Session 7 Overview: *Imagers and Range Sensors*

IMAGERS, MEDICAL, MEMS AND DISPLAYS SUBCOMMITTEE

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This session covers a wide variety of imagers and range sensors for different applications. For imagers, innovations are reported achieving smaller pixel pitch, higher frame rate or increased on-board intelligence. For ranging, improved SPAD and MEMS based LIDAR are presented and improved depth sensing is achieved. The first paper describes a photodiode-based indirect Time-of-Flight (iToF) depth sensor, followed by three Single Photon Avalanche Diodes (SPAD) based range sensors: a direct Time-of-Flight (dToF) flash LiDAR, a LiDAR system using MEMS mirrors for scanning, and a flash LiDAR with smaller pitch and advanced process node. The next paper presents a SPAD-based photon-counting imager to eliminate the SNR dip problem in photodiode-based high-dynamic-range imagers, followed by a conventional color imager with high resolution, larger pixels, and low noise for digital cameras. The last three papers describe a programmable convolutional imager with near-sensor processing for embedded computer vision applications, a large-format imager for computational imaging with adaptive dynamic range control, and a conventional color imager with high resolution and smaller pixels for smartphone and mobile applications.

8:30 AM

7.1 A 4-tap 3.5μm 1.2Mpixel Indirect Time-of-Flight CMOS Image Sensor with Peak Current Mitigation and Multi-User Interference Cancellation

Min-Sun Keel, Samsung Electronics, Hwaseong, Korea

In Paper 7.1, Samsung presents a 1.2Mpixel stacked iToF depth sensor with 4-tap 3.5μm pixels. It uses multiple interleaving to reduce peak current with minimal demodulation contrast (DC) degradation and multi-user interference cancellation by pseudo-random modulation. The design achieves QE of 38% at 940nm, DC of 96% at 100MHz and 80% at 200MHz modulation with a depth noise less than 0.35% at the 2×2 binning.

8:38 AM

7.2 A 48×40 13.5mm Depth Resolution Flash LiDAR Sensor with In-Pixel Zoom Histogramming Time-to-Digital Converter

Bumjun Kim, Ulsan National Institute of Science and Technology, Ulsan, Korea

In Paper 7.2, Ulsan National Institute of Science and Technology presents a 48×40 SPAD-based flash LiDAR achieving 45m detectable range and 13.5mm depth resolution. The zoom histogramming TDC incorporates a coarse SAR TDC in a long distance with a fine phase-domain depth extraction in a short distance.

8:46 AM

7.3 A 189×600 Back-Illuminated Stacked SPAD Direct Time-of-Flight Depth Sensor for Automotive LiDAR Systems

Oichi Kumagai, Sony Semiconductor Solutions, Atsugi, Japan

In Paper 7.3, Sony demonstrates a MEMS-based LiDAR system for autonomous driving, using a 189×600 back-illuminated, stacked SPAD sensor to measure up to 150m with 0.1% accuracy for a 10%-reflectivity and 200m with 0.1% accuracy for a 95%-reflectivity target. The sensor employs passive quenching and recharge front-end circuitry, time-correlated single-photon counting, and digital signal processing.

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8:54 AM

7.4 A 256×128 3D-Stacked (45nm) SPAD FLASH LiDAR with 7-Level Coincidence Detection and Progressive Gating for 100m Range and 10klux Background Light

Preethi Padmanabhan, EPFL, Neuchâtel, Switzerland

In Paper 7.4, EPFL uses multi-level coincidence detection and progressive gating techniques to design a flash LiDAR with a 256×128, 7µm-pitch SPAD array stacked on a circuit layer in an advanced technology node. The sensor features a shared 14b TDC with 60ps resolution, reaching 7cm depth accuracy at 100m range under 10klux background light.

9:02 AM

7.5 A 250fps 124dB Dynamic-Range SPAD Image Sensor Stacked with Pixel-Parallel Photon Counter Employing Sub-Frame Extrapolating Architecture for Motion Artifact Suppression

Jun Ogi, Sony Semiconductor Solutions, Kanagawa, Japan

In Paper 7.5, Sony introduces a 250fps and 124dB dynamic-range, 160×264 12.24µm-pitch SPAD photon-counting image sensor with motion artifact suppression, no SNR dip, and efficient power reduction under high-light conditions. The sub-frame extrapolating architecture sufficiently decreases the number of counter bits and reduces the power consumption by a factor of 100 under high-light conditions.

9:10 AM

7.6 A High-Speed Back-Illuminated Stacked CMOS Image Sensor with Column-Parallel kT/C-Cancelling S&H and Delta-Sigma ADC

Chihiro Okada, Sony Semiconductor Solutions, Kanagawa, Japan

In Paper 7.6, Sony presents a 50.1Mpixel, 4.16µm-pitch, back-illuminated stacked CIS with a pipelined column-parallel kT/C noise-cancelling sample-and-hold circuit and a 14b delta-sigma ADC achieving 1.18e-rms random noise at 250fps. The design splits the pixel signal line to lower the wiring load and increase the operation speed.

9:18 AM

7.7 A 0.2-to-3.6TOPS/W Programmable Convolutional Imager SoC with In-Sensor Current-Domain Ternary-Weighted MAC Operations for Feature Extraction and Region-of-Interest Detection

Martin Lefebvre, Université catholique de Louvain, Louvain-la-Neuve, Belgium

In Paper 7.7, the Université catholique de Louvain presents a 160×128 imager using in-sensor current-domain ternary-weighted MAC operations and reaching a minimum energy of 2.5pJ/pixel·frame·filter and a peak efficiency of 3.6TOPS/W. The chip can produce 8b outputs or thresholded 1b outputs for feature extraction and region-of-interest detection. It features a pixel-level current gain tunable between 40 and 100dB, which yields an inter-scene input dynamic range >73.4dB.

9:26 AM

7.8 A 1-inch 17Mpixel 1000fps Block-Controlled Coded-Exposure Back-Illuminated Stacked CMOS Image Sensor for Computational Imaging and Adaptive Dynamic Range Control

Tomoki Hirata, Nikon, Tokyo, Japan

In Paper 7.8, Nikon demonstrates a 4k×4k, 2.7µm pixel, back-illuminated stacked CIS with controllable integration time for each pixel block for coded exposure applications. This design achieves a dynamic range of 110dB at 1000fps and higher than 134dB at 60fps, when block-coded exposure is performed over a period of multiple frames.

9:30 AM

7.9 1/2.74-inch 32Mpixel-Prototype CMOS Image Sensor with 0.64µm Unit Pixels Separated by Full-Depth Deep-Trench Isolation

Sungbong Park, Samsung Electronics, Hwaseong, Korea

In Paper 7.9, Samsung continues going down the pixel-scaling path and presents a back-illuminated, stacked 32Mpixel CIS with a 0.64µm pixel, isolated by full-depth deep trench isolation. Various pixel design and fabrication process improvements are developed such that the 0.64µm pixels show equivalent or even better performance comparable to the 10% larger pixels despite a 25% reduction in photodiode volume.