A 270-mA Self-Calibrating-Clocked Output-Capacitor-Free LDO With 0.15–1.15V Output Range and 0.183-fs FoM

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***Abstract*— This article proposes a fully integrated output-capacitor-free low-dropout regulator (LDO) for mobile applications. To overcome the limited output voltage range of typical analog LDOs, our design uses a rail-to-rail voltage-difference-to-time-converter (VDTC) and a charge pump (CP) to achieve a wide output range. Using a self-calibrating clock generator (SCCG) removes the need for an external clock source and adaptively tunes the clock frequency, enabling fast transient responses while minimizing quiescent current. A tunable undershoot compensator (TUC) mitigates voltage droop by detecting the drop in the output voltage due to a sharp increase in load current and compensating the output voltage immediately. The proposed LDO is fabricated in a 65-nm low power (LP) CMOS process and demonstrates a maximum load current capacity of 270 mA. The input and output voltage ranges of the LDO are 0.5–1.2 and 0.15–1.15 V, respectively, with 12.7-μA quiescent current and 99.99% peak current efficiency. The measured undershoot and settling time are 150 mV and 100 ns at a slew rate of 200 mA/3 ns, respectively, achieving a figure of merit (FoM) of 0.183 fs.**

***Index Terms*— Charge pump (CP), low-dropout regulator (LDO), output-capacitor-free LDO, voltage difference to time converter, voltage regulator.**

I. Introduction

INDIVIDUAL power management of hardware blocks in system-on-chip (SoC) is crucial for maximizing battery life. Recently released SoCs for mobile systems have multiple power domains and utilize different types of voltage regulators to drive them efficiently. Due to its small area and high power density, low-dropout regulators (LDOs) are widely used as voltage regulators for hardware blocks in SoCs.

Analog LDOs are commonly found in those systems due to their good regulation performance, fast transient response, and small area. However, they require an output capacitor on the order of microfarads that incurs a large area overhead, which motivated output-capacitor-less designs [1]–[6]. Besides, mobile SoCs often rely on deep voltage scaling to maximize power efficiency, but analog LDOs are not suitable for low-voltage operations due to limited voltage headroom, and frequency compensation must be accompanied for stable operation.

Contrarily, digital LDOs offer a wide operating range and maintain good transient responses without an analog amplifier and a frequency compensation network. These benefits motivated an array of recent studies on digital LDOs as an integrated voltage regulator [7]–[9]. They typically require a high-frequency clock to minimize latency to achieve a fast transient response, but this results in a large switching power overhead. Therefore, event-driven digital LDOs were proposed to overcome the correlation between the clock frequency and the switching power consumption [10]–[12].

Nevertheless, the LDO output may experience a voltage ripple due to the nature of digital LDOs having limited output resolution. Using an analog-assisted loop [13] or a hybrid structure [14] resolves these issues by combining the advantages of analog and digital LDOs. However, in analog-assisted LDO [13], the input clock frequency should be carefully determined since it dictates the regulation characteristics. In addition, it has a limited operating voltage range due to the CP that supplies power to the circuit driving the NMOS power transistor. The hybrid LDO [14] requires an output capacitor on the order of nanofarads and also has a limited operating range.

Another approach, a class-D LDO, achieves good regulation performances and small area without requiring a high-frequency clock [15]. However, a large output capacitor is needed in the design, and the LDO exhibits a large quiescent current and limited operating range. Recently, it was reported that using a voltage-difference-to-time converter (VDTC) in an LDO could significantly improve regulation efficiency and reduce power consumption without using an output capacitor [16]. However, this design suffers limited operating voltage range and a tradeoff between transient response, power consumption, and settling time, which is determined by the operating frequency.

In this article, we present an output-capacitor-free LDO with a wide output range and fast transient responses. The design uses a rail-to-rail VDTC circuit with a CP and a self-calibrating clock generator (SCCG), along with a tunable undershoot compensator (TUC). The remainder of this article is organized as follows. The overall architecture of the proposed LDO is described in Section II. Section III presents the implementation details and explains the benefits of the

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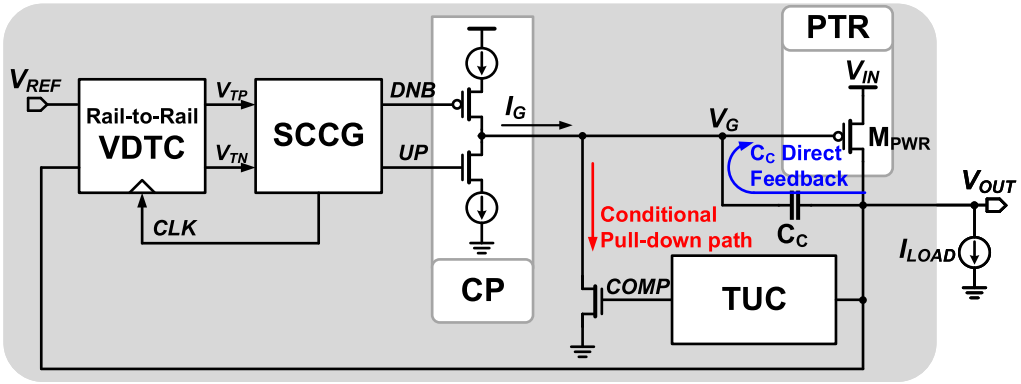

Fig. 1. Overall architecture of the proposed LDO.

proposed techniques. We analyze the stability of the LDO with the focus on SCCG in Section IV. Section V discusses the chip measurement results, and Section VI concludes this article.

II. Proposed LDO Architecture

Fig. 1 shows the overall architecture of the proposed LDO. The LDO consists of a rail-to-rail VDTC combined with an SCCG, a CP, a TUC with a pull-down transistor, a power transistor M_{PWR}, and a coupling capacitor C_C. VDTC with SCCG converts V_{OUT}–V_{REF} into digital pulses (DNB and UP) with the widths proportional to the magnitude of the voltage difference. This adjusts the power transistor's gate voltage (V_{G}) by controlling the current of CP (I_{G}) to regulate V_{OUT}. C_C directly feeds back the change in V_{OUT} to V_{G} for fast transient responses [16]. TUC detects a drop in V_{OUT} due to an abrupt load current increase and generates a pulse (COMP) to pull down V_{G} conditionally for suppressing undershoot. SCCG generates a clock for the main loop, where the clock frequency is optimized depending on V_{OUT}, V_{DD}, and process, voltage, and temperature (PVT) variations to maximize transient responses and energy efficiency.

Fig. 2 shows LDO operations with timing diagram examples. In the case of normal operation when a load current changes relatively slowly [Fig. 2(a)], V_{OUT} is regulated through the main loop consisting of VDTC, SCCG, and CP. When V_{OUT} falls due to an increase in load current, VDTC with SCCG generates a UP pulse in every clock cycle to make CP generate pull-down current, which lowers V_{G} to recover V_{OUT}. Simultaneously, SCCG slows down the clock frequency so that V_{OUT} can be stabilized more quickly. After V_{OUT} is regulated, UP pulses are no longer generated, and SCCG maximizes the clock frequency to minimize quiescent current and speed up the loop reaction against the next load current change. On the other hand, when V_{OUT} increases due to load current reduction, V_{G} is raised through the DNB pulses to lower V_{OUT}. Likewise, SCCG slows down the clock frequency to reduce the V_{OUT} recovery time. After V_{OUT} is regulated, the clock frequency returns to its maximum value. During these operations, the direct feedback capacitor C_C immediately reflects the change in V_{OUT} in V_{G}, improving the transient response.

If the load current increases quickly with a high slew rate [Fig. 2(b)], TUC detects a voltage drop larger than $V_{\mathrm{TH\_TUC}}$

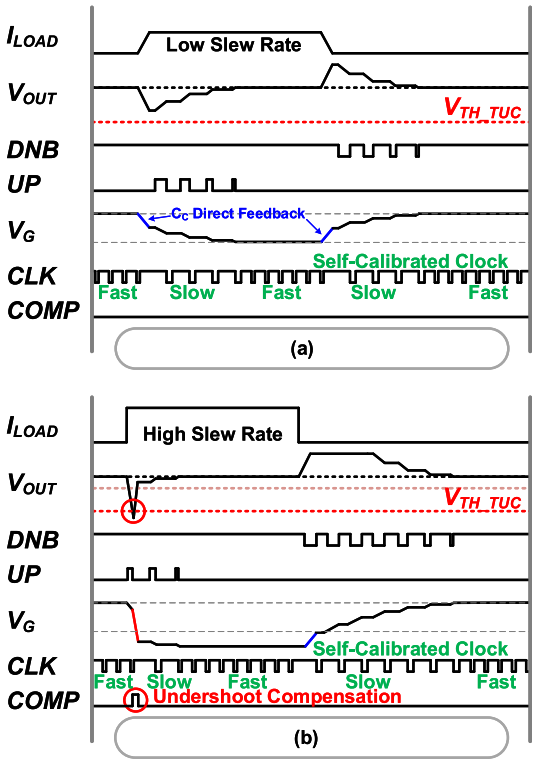

Fig. 2. Timing diagrams of the proposed LDO for (a) normal and (b) fast transient operations.

and generates a COMP pulse, which directly pulls down V_{G} to compensate V_{OUT} in addition to the main regulation loop described above. While TUC does not detect voltage overshoot, a voltage drop is usually considered a more severe issue in voltage-scaled microprocessors [17], [18]. If needed, we could also implement a similar overshoot compensator to detect an overshoot in the output voltage and mitigate the issue by pulling up V_{G}.

III. Circuit Implementation

A. Rail-to-Rail VDTC Circuit

Fig. 3 shows the rail-to-rail VDTC circuit, and Fig. 4 shows its timing diagram. The VDTC circuit operates with a small bias current (I_{SS}) that limits its current consumption. VDTC has two operation phases. If CLK = 0 (reset phase), V_{TN} and V_{TP} are reset to V_{DD}. If CLK = 1 (conversion phase), V_{TN} and V_{TP} are discharged with the currents proportional to

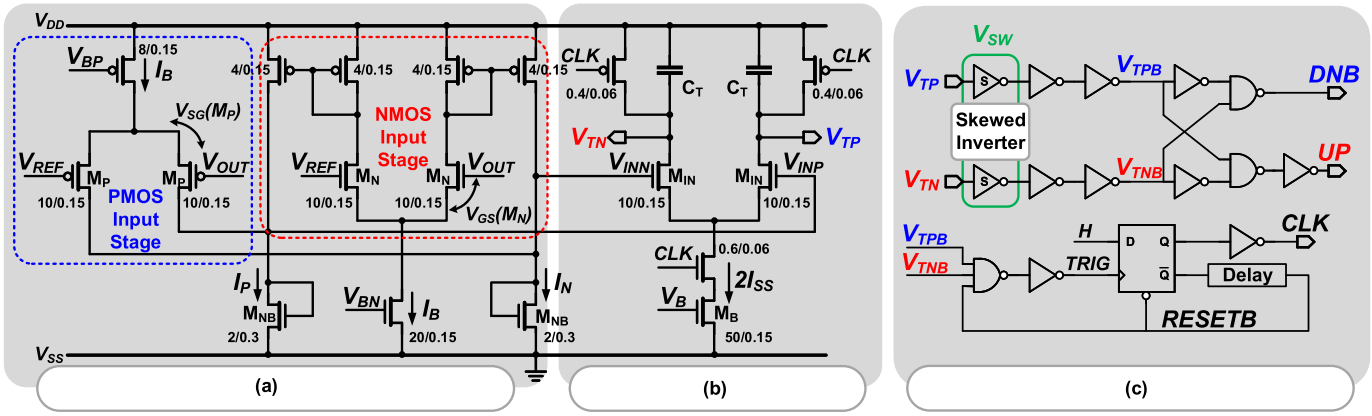

Fig. 3. (a) Rail-to-rail input preprocessing stage. (b) VDTC circuit. (c) SCCG circuit.

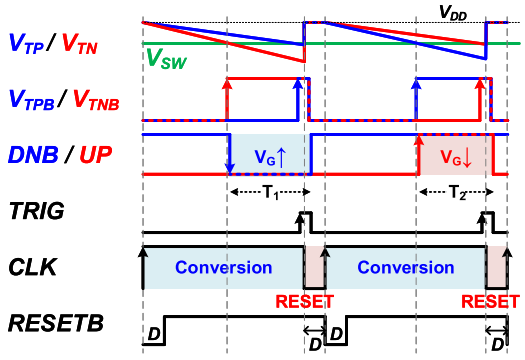

Fig. 4. Timing diagram of VDTC.

the two input voltages V_{INN} and V_{INP}, respectively. A down pulse (DNB) or an up pulse (UP) is initiated when V_{TN} or V_{TP} crosses the switching voltage of the skewed inverters (V_{SW}) and is disabled when the other signal (V_{TP} or V_{TN}) also crosses V_{SW}, rendering the input difference ($\triangle V$) into the pulsewidth (T). More precisely, the pulsewidth of UP or DNB pulse follows the following equation:

$$T = \frac{-2C_{\mathrm{T}}(V_{\mathrm{DD}} - V_{\mathrm{SW}})g_{m,M_{\mathrm{IN}}}}{{I_{\mathrm{SS}}}^2} \cdot \triangle V \tag{1}$$

where $g_{m,M_{\mathrm{IN}}}$ is the transconductance of the input transistor. After encoding $\triangle V$ into a DNB or UP pulse, CLK goes to low, and VDTC is reset during the time window whose width (D) is determined by the delay unit inside SCCG.

In LDOs, the output voltage may oscillate near the desired value at a steady state due to limited resolution, which mainly occurs in digital LDOs. However, our design does not suffer this issue because of the nature of its analog operation. VDTC converts $\triangle V$ into the time domain by generating a pulse whose width is determined by (1). The pulsewidth is directly proportional to the value of $\triangle V$, suggesting that VDTC could be regarded as an analog amplifier or voltage-time converter with infinite resolution. Therefore, our system does not exhibit limit cycle oscillation. In addition, in the actual circuit, VDTC is unable to generate a pulse with an arbitrarily small duration. If $\triangle V$ is very small, an output pulse is not generated due to the transition delay of the pulse generation circuit. In other words, when V_{OUT} is very close to V_{REF}, no output pulse is generated, further removing the possibility of limit cycle oscillation.

The input range of VDTC in Fig. 3(b) is limited by V_{GS} of the input NMOS transistors (M_{IN}). The gate voltage of M_{IN} must be large enough to secure the voltage headroom of M_{B} operating as a current source and V_{GS} of M_{IN}, making VDTC fail to operate with input voltages smaller than $V_{\mathrm{GS},M_{\mathrm{IN}}}+V_{\mathrm{DS},M_{\mathrm{B}}}$. This also directly limits the output voltage range of the LDO. In addition, the values of V_{REF} and V_{OUT} are determined by the target application. As a result, the performance of VDTC can significantly vary since the gain of VDTC depends on the dc level of inputs. To address these issues, we propose a rail-to-rail preprocessing stage shown in Fig. 3(a). The preprocessing circuit translates rail-to-rail input voltages into the voltage range in which VDTC can properly operate, and hence, the gain of VDTC remains nearly the same for a wide range of V_{REF} and V_{OUT}. This effectively expands the operation range of the LDO.

Fig. 5 shows the detailed operations of the rail-to-rail input preprocessing stage. The circuit converts the input (V_{REF} and V_{OUT}) into the voltages (V_{INN} and V_{INP}) that VDTC can process. For low-voltage inputs (when $(V_{\mathrm{REF}}, V_{\mathrm{OUT}}) - V_{\mathrm{SS}} < V_{\mathrm{GS,M_N}}$), only PMOS stage operates as shown in Fig. 5(a) and the voltage difference of the two preprocessing stage outputs ($\triangle V_M$) is given by

$$\triangle V_M = V_{\mathrm{INP}} - V_{\mathrm{INN}} = \frac{g_{m,M_{\mathrm{P}}}}{g_{m,M_{\mathrm{NB}}}}(V_{\mathrm{REF}} - V_{\mathrm{OUT}}). \tag{2}$$

For high-voltage inputs (when $V_{\mathrm{DD}} - (V_{\mathrm{REF}}, V_{\mathrm{OUT}}) < V_{\mathrm{SG,M_P}}$), only NMOS stage operates as shown in Fig. 5(b) and $\triangle V_M$ is

$$\triangle V_M = \frac{g_{m,M_{\mathrm{N}}}}{g_{m,M_{\mathrm{NB}}}}(V_{\mathrm{REF}} - V_{\mathrm{OUT}}) \tag{3}$$

which is identical to (2) if we design the circuit in a way that $g_{m,M_{\mathrm{P}}}$ and $g_{m,M_{\mathrm{N}}}$ have the same value. For intermediate input voltage ranges, both stages are activated, as shown in Fig. 5(c). In this case, $\triangle V_M$ is

$$\triangle V_M = \frac{g_{m,M_{\mathrm{P}}} + g_{m,M_{\mathrm{N}}}}{g_{m,M_{\mathrm{NB}}}}(V_{\mathrm{REF}} - V_{\mathrm{OUT}}) \tag{4}$$

which is twice as large as (2) and (3) if $g_{m,M_{\mathrm{P}}} = g_{m,M_{\mathrm{N}}}$. While the gain of the preprocessing stage could vary between 1 and 2, the LDO is designed to exhibit stable operation with any preprocessing stage gain in this range. The detailed stability analysis follows in Section III-B.

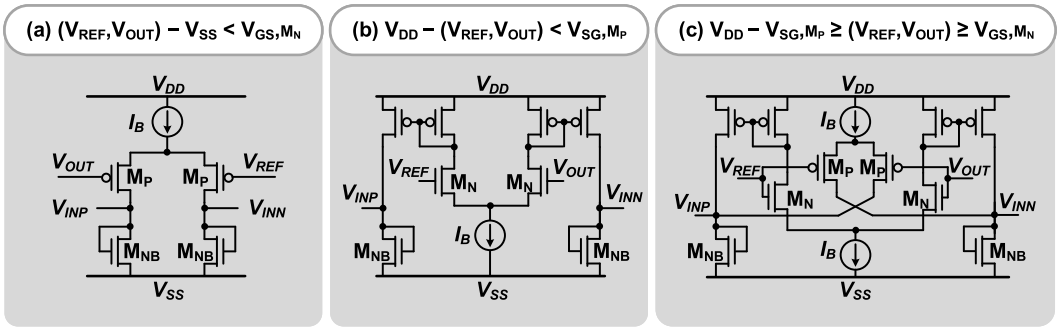

Fig. 5. Operations of rail-to-rail input preprocessing stage for (a) low-voltage inputs, (b) high-voltage inputs, and (c) intermediate-voltage inputs.

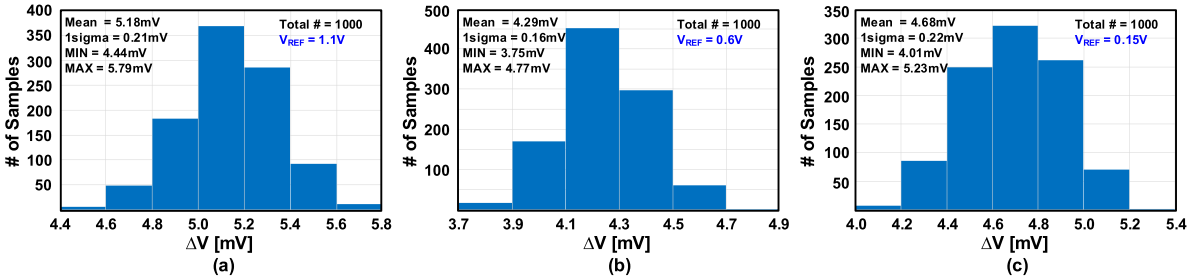

Fig. 6. Monte Carlo simulation results of input offset of the rail-to-rail VDTC for (a) V_{REF} = 1.1 V, (b) V_{REF} = 0.6 V, and (c) V_{REF} = 0.15 V.

In all three cases, the minimum voltage level of V_{INN} and V_{INP} is determined by the size of the diode-connected transistors (M_{NB}) and the current flowing through them (I_{P} and I_{N}). For proper operation of VDTC, the input voltages should be higher than $V_{\mathrm{th},M_{\mathrm{IN}}}$. When $V_{\mathrm{REF}} = V_{\mathrm{OUT}}$, I_{P} and I_{N} are identical to the bias current I_{B}, resulting in the design constraint shown in the following:

$$\sqrt{\frac{I_B}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{,M_{\mathrm{NB}}}}} + V_{th,M_{\mathrm{NB}}} = V_{GS,M_{\mathrm{NB}}} > V_{th,M_{\mathrm{IN}}}. \quad (5)$$

We need to appropriately size the transistor M_{NB} to meet the constraint above. When V_{OUT} raises or drops due to load current change, one of the input voltages (V_{INN} and V_{INP}) will increase, while the other decreases, and hence, at least one of the input transistors stays turned on, guaranteeing that the main loop still operates normally and V_{OUT} is regulated. As a result, with the preprocessing stage, VDTC is no longer limited by the voltage level of the inputs V_{REF} and V_{OUT}.

It is important to minimize an offset in the rail-to-rail VDTC, as it directly introduces an offset in the output. The offset is mainly incurred by the transistor mismatch of a differential input pair. We minimize the offset by carefully drawing the layout. Specifically, transistors share the active region to minimize the shallow trench isolation (STI) effect that affects the effective length of the transistors. We also add a dummy transistor to the boundary to eliminate the well-proximity effect. Finally, the input pair is laid out as a common-centroid pattern to minimize mismatch. Fig. 6 shows the Monte Carlo simulation results of the input offset of the rail-to-rail VDTC. Fig. 7 shows the minimum voltage difference between V_{REF} and V_{OUT} that VDTC can detect in simulation. It is 0.13 mV in the typical condition (TT, V_{IN} = 0.8 V, 25 °C) and 1.54 mV in the worst condition (SF, V_{IN}=0.5 V, 85 °C).

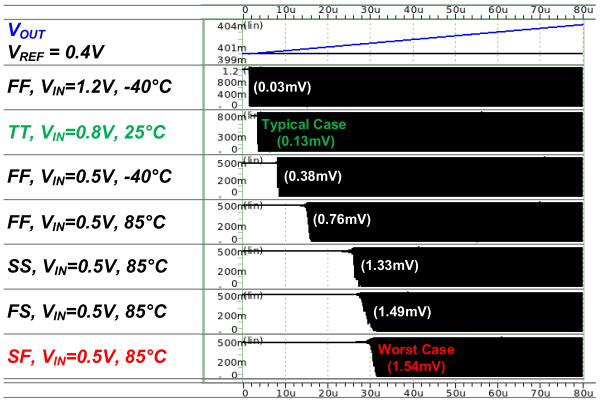

Fig. 7. Minimum voltage difference that can be detected by VDTC in simulation.

B. Self-Calibrating Clock Generator

It is crucial to choose an optimal operating frequency of VDTC, as it dictates the regulation performance and energy efficiency of the LDO. Ideally, if both V_{TN} and V_{TP} of VDTC cross V_{SW}, the output pulse is disabled and VDTC becomes ready for the next conversion. However, it is impossible to take advantage of this property with a fixed clock frequency as the pulse duration continuously changes depending on the regulation error. Hence, using an external clock with a fixed frequency would unavoidably incur a tradeoff between regulation speed and quiescent current. Fig. 8(a) shows the issue related to the clock frequency selection. Using a slow clock not only slows down settling due to fewer pulses generated but also makes it harder to detect fast load changes. In addition, it increases quiescent current due to the short-circuit current in the skewed inverters since they are kept turned on even after the output pulse is disabled. Contrarily, using a fast clock stops conversion too early before both signals reach V_{SW} and reduces the output pulsewidth, also increasing settling time. The optimal clock frequency depends on many factors,

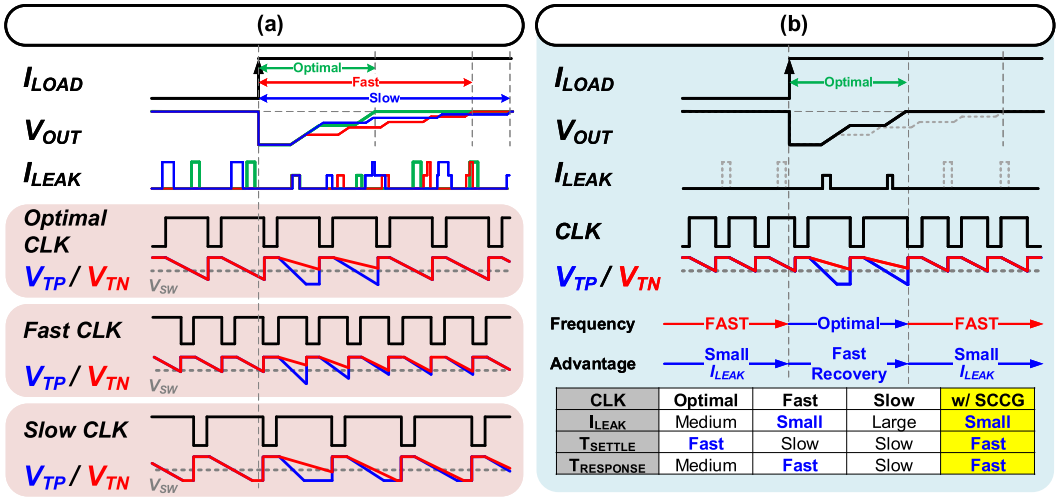

Fig. 8. Timing diagram examples of SCCG showing its advantages: (a) without SCCG and (b) with SCCG.

including V_{REF}, V_{OUT}, and PVT variations; hence, it is nearly impossible to tune the clock frequency for each case.

Instead, our design employs an SCCG circuit that automatically generates a clock with the optimal frequency. SCCG detects when both V_{TP} and V_{TN} cross V_{SW} and starts the next clock cycle immediately, guaranteeing optimal clock frequency at any operating point and under PVT variations. Fig. 8(b) shows an example timing diagram of the proposed LDO operating at a frequency calibrated by SCCG in real time. In a static load state where V_{OUT} is the same as V_{REF}, V_{TP} and V_{TN} are discharged at the same speed. In this case, the VDTC returns to the reset phase right after both V_{TP} and V_{TN} cross V_{SW}. As a result, the short-circuit current of the skewed inverters is minimized. In addition, due to the fast clock frequency, the load regulation characteristic of V_{OUT} in a static load condition is improved and the main loop bandwidth is maximized, enabling fast load change detection and response. When V_{OUT} deviates from V_{REF} due to a load current change, the time required for V_{TP} and V_{TN} to reach V_{SW} varies with the difference between V_{REF} and V_{OUT}, and the clock frequency decreases as necessary for optimal operation. In detail, the clock frequency becomes slow enough to wait until both V_{TP} and V_{TN} reach V_{SW} to maximize the output pulsewidth for the given voltage difference $V_{REF}-V_{OUT}$. As a result, CP could be turned on for long enough to regulate V_G. In addition, the next cycle immediately follows after a short reset period, adaptively tuning the clock frequency to its optimal value. This effect minimizes the settling time of V_{OUT}, and the LDO achieves optimal load transient responses. Simultaneously, since the clock frequency does not slow down more than necessary, the short-circuit current incurred by the skewed inverter is minimized while not sacrificing transient performance. Furthermore, it has the advantage of removing the cost of an external clock input.

Fig. 9 shows a timing diagram example showing how the clock frequency varies with V_{OUT} due to SCCG shown in Fig. 3(c). The gain of the rail-to-rail input preprocessing stage is assumed to be 1 in this case. First, in the steady state in which V_{OUT} is regulated to be equal to V_{REF}, V_{TP} and V_{TN} in VDTC reach V_{SW} simultaneously. Hence, neither DNB nor UP pulse is not generated, making V_{OUT} unchanged. When they cross V_{SW}, SCCG detects the end of voltage-to-time conversion and starts the next cycle immediately, maximizing the clock frequency f_S. The maximum clock frequency in the steady state is $1/(T_{MIN}+D)$, where T_{MIN} is the time it takes for both V_{TP} and V_{TN} to reach V_{SW} and D is the reset delay of SCCG. If a sudden increase or decrease in load current causes a change in V_{OUT}, the larger the difference between V_{REF} and V_{OUT}, which is the input of VDTC, the longer the time difference between when V_{TP} and V_{TN} reach V_{SW}. This renders DNB or UP pulse longer, and thus, the frequency becomes slower. Consequently, CP recovers V_{OUT} by charging or discharging V_G for a longer period of time. In Fig. 9, these additional times are denoted by T_1–T_3, and their duration follows $T_1>T_2>T_3$ in the order of $|V_{OUT}-V_{REF}|$. Accordingly, the clock frequency is the slowest when a load transient occurs, and then, it gradually increases toward the maximum clock frequency $1/(T_{MIN}+D)$ as V_{OUT} recovers.

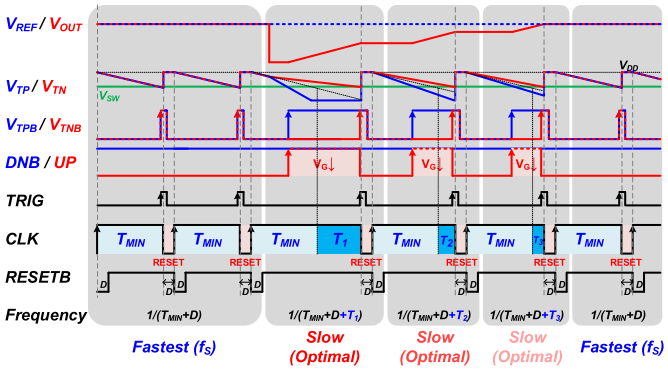

Fig. 9. Detailed timing diagram of SCCG with output voltage changes.

Fig. 10 shows the simulated load transient responses. In a steady state with 0.85-V V_{OUT}, the clock generator generates a fast clock with 41.3-MHz frequency regardless of the load current. If a load current changes, the clock generated by SCCG slows down as much as V_{OUT} changes (i.e., $|V_{REF}-V_{OUT}|$). When TUC is OFF, the clock frequency reduces to 11.5 MHz under a load transient of 200 mA at the TT corner, and then,

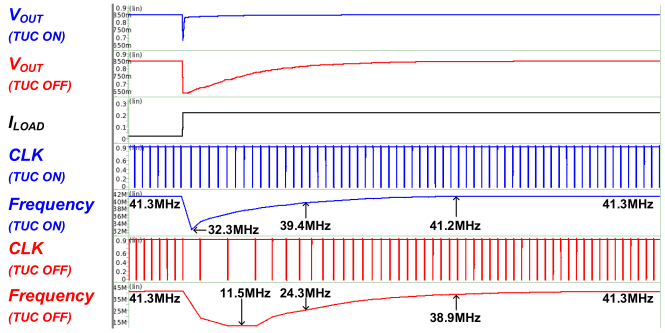

Fig. 10. Simulated load transient responses of SCCG.

it gradually returns to 41.3 MHz as V_{OUT} approaches V_{REF}. When TUC is ON, the clock frequency initially slows down to 32.3 MHz.

Fig. 11 shows the simulated and measured start-up operations of the proposed LDO at the lowest operating voltage (V_{IN}=0.5 V and V_{OUT}=0.15 V). When the LDO is enabled, V_{TP} drops and the UP pulse is enabled. This continues until V_{OUT} rises enough so that V_{TN}, the other output of VDTC, reaches V_{SW}. When V_{TN} crosses V_{SW}, SCCG starts resetting and generating the clock signal, enabling normal LDO operations. The start-up time is 2.5 μs in both simulation and measurement.

Nasir *et al.* [8] proposed a reduced dynamic stability technique that detects an abrupt change in the output voltage and temporarily adopts a fast clock to accelerate output recovery. The SCCG in our design achieves a similar effect by automatically changing the clock frequency based on the error in the output voltage, but with distinct differences. First, our design slows down the clock to increase the amount of charge delivered to CP when V_{OUT} departs from V_{REF}, instead of raising the clock frequency. Second, in the prior design [8], the clock frequency returns to a nominal value when the output voltage is within a predefined range set by two comparators. Contrarily, our design continues to tune the clock frequency until V_{OUT} becomes identical to V_{REF}, which improves transient responses. Finally, our design does not need an additional external clock with a higher frequency since the clock is generated internally, reducing implementation overhead.

C. Tunable Undershoot Compensator

While the output-capacitor-free structure reduces the design cost by removing the need for a large output capacitor, it is vulnerable to fast load transient. We address this issue by employing TUC circuit in the design. Fig. 12 shows the circuit diagram of TUC. The circuit detects an abrupt change that exceeds a threshold and conditionally pulls down V_{G} to quickly increase the load current. A similar circuit for undershoot detection using a high-pass filter (HPF) demonstrated performance improvements [9], but process variations may undermine its benefit. Specifically, the dc level of V_{M} and the switching voltage of the skewed inverter are directly affected by the process variation. This translates to variations in the delay for generating the COMP pulse, which is the output of the TUC, and the undershoot may not be mitigated

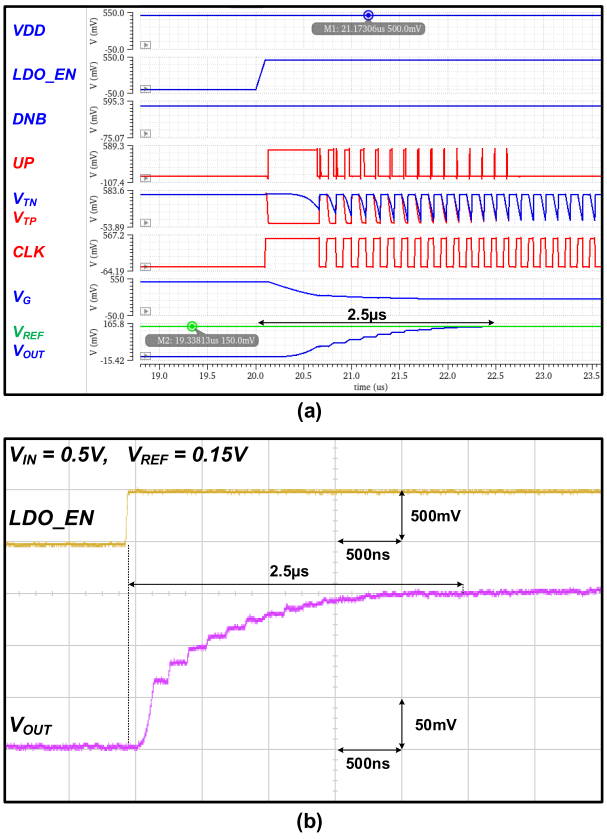

Fig. 11. (a) Simulated and (b) measured start-up operations at V_{IN} = 0.5 V and V_{OUT} = 0.15 V.

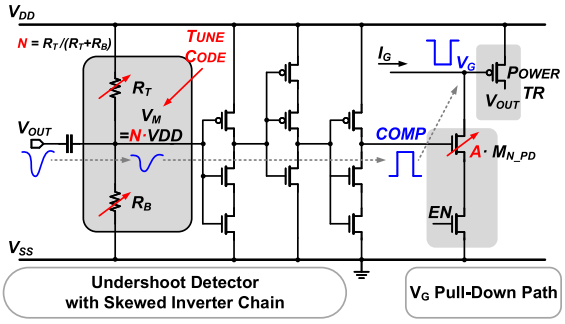

Fig. 12. TUC.

fast enough or an overcompensation may occur. Therefore, we employ an additional circuitry to fine-tune the circuit, as shown in Fig. 12. By tuning the ratio of resistances (N) and the number of NMOS devices to pull down V_{G} (A), the undershoot detection-level deviation due to process variation can be effectively suppressed. The total width of $M_{\mathrm{N\_PD}}$ is determined by the tuning code A. We used minimum-length transistors, and the total width can be tuned between 16 and 40 μm.

There are several design considerations when implementing a TUC. First, it should not affect the operational stability of the main loop. Since the change in the output voltage goes to the TUC circuit through HPF, the cutoff frequency of the HPF must be set so as not to affect the operation of the main loop. We need to design the HPF to have a sufficient margin outside the operating bandwidth of the main loop. In the final design, the cutoff frequency of the HPF was set to 2.2 MHz, which is significantly higher than the main loop bandwidth on the order

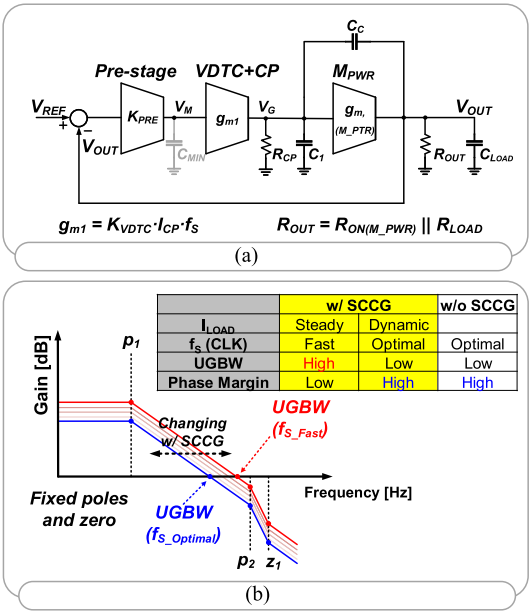

Fig. 13. (a) Small-signal modeling of the proposed LDO and (b) frequency analysis with SCCG.

of 100 kHz. Next, we need to ensure that overcompensation does not occur. To prevent overcompensation and properly operate the TUC, the following two elements of circuit design are important: 1) the size of M_{N_PD} that determines the amount of compensation and 2) the resolution of the resistor ratio that determines the timing of compensation by adjusting the dc level V_M for the following skewed inverter. The tuning circuit needs to be designed to sufficiently cover the load transient that occurs depending on the application of the load device to be driven by the LDO. The size of M_{N_PD} is chosen considering the capacitance at the gate node of the power transistor. If the size of M_{N_PD} is set too large, overcompensation may occur. Therefore, it is necessary to tune the size of M_{N_PD} by changing the number of NMOS transistors (A) so that overcompensation does not occur for the maximum V_{IN}/V_{OUT} value. The amount of compensation is proportional to the steady-state level of V_G, which determines the V_{DS} of M_{N_PD}, and hence, the circuit would not suffer overcompensation for smaller V_{IN}/V_{OUT} values for the same load current. In addition, the smaller the resolution of the resistor ratio, the finer the timing of compensation. Therefore, it is advantageous to subdivide the resistor ratio as much as the hardware allows.

IV. Stability Analysis With Self-Calibrated Clock

The small-signal model of the proposed LDO is shown in Fig. 13(a). The model consists of the preprocessing stage, VDTC+CP, the coupling capacitor C_C, and the power transistor. The discrete-time operation of VDTC and CP can be approximated as a linear model. VDTC converts the preprocessing stage output $\triangle V_M$ into a pulse. If the gain of VDTC is K_{VDTC}, the pulsewidth is $K_{VDTC} \cdot \triangle V_M$ following (1). Since the output of CP is I_{CP}, we can replace the combination of VDTC and CP with a voltage-dependent current source with a gain of $g_{m1} = K_{VDTC} \cdot I_{CP} \cdot f_S$.

The gain of the preprocessing stage is represented by (2)–(4). The function of the preprocessing stage is treated as a constant term in the small-signal model. In our design, we designed g_{m,M_P}, g_{m,M_N}, and $g_{m,M_{NB}}$ to have the same value. Therefore, the gain stays in the range between 1 and 2, depending on the input voltages, suggesting that the preprocessing stage gain does not significantly vary over the entire input voltage range. Since the gate capacitance of M_{IN} ($C_{M_{IN}}$) and the resistance at the node V_M ($1/g_m$ of M_{NB}) are both small, the pole at V_M is located out-of-band over 100 MHz and is negligible. Consequently, the loop gain function of the LDO is similar to a Miller compensation network [19]. The term K_{PRE} represents the preprocessing stage gain and is expressed by

$$K_{PRE} = \begin{cases} \dfrac{g_{m,M_P}}{g_{m,M_{NB}}} \approx 1, & (V_{REF},\ V_{OUT}) - V_{SS} < V_{GS,M_N} \\ \dfrac{g_{m,M_N}}{g_{m,M_{NB}}} \approx 1, & V_{DD} - (V_{REF},\ V_{OUT}) < V_{SG,M_P} \\ \dfrac{g_{m,M_P} + g_{m,M_N}}{g_{m,M_{NB}}} \approx 2, & \text{otherwise.} \end{cases} \tag{6}$$

Other components in the small-signal model are defined as follows. C_1 is the parasitic capacitance at the gate of the power transistor, R_{CP} is the output resistance of CP, $g_{m,M_{PWR}}$ and $R_{ON,M_{PWR}}$ are the transconductance and output resistance of the power transistor, respectively, and C_C is the coupling capacitor. The output load resistance and load capacitance are represented by R_{LOAD} and C_{LOAD}, respectively. Based on this, the loop gain function simplifies to

$$A_v(s) = \frac{A_{OL} \cdot \left(1 - \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)} \tag{7}$$

where

$$A_{OL} = K_{PRE} \cdot g_{m1} R_{CP} \cdot g_{m,M_{PWR}} R_{OUT} \tag{8}$$

$$g_{m1} = K_{VDTC} \cdot I_{CP} \cdot f_S \tag{9}$$

$$R_{OUT} = R_{ON,M_{PWR}} \parallel R_{LOAD} \tag{10}$$

and f_S is the clock frequency generated by SCCG. Assuming that $C_{LOAD} \gg C_C \gg C_1 \gg C_{MIN}$ and $g_{m,M_{PWR}} R_{OUT} \gg 1$ for the sake of simplicity, the following equations for poles, zeros, and the unity-gain bandwidth (UGBW) are obtained:

$$p_1 = \frac{1}{g_{m,M_{PWR}} R_{OUT} R_{CP} C_C} \tag{11}$$

$$p_2 = \frac{g_{m,M_{PWR}}}{C_{LOAD}} \tag{12}$$

$$z_1 = \frac{g_{m,M_{PWR}}}{C_C} \tag{13}$$

$$\text{UGBW} = \frac{K_{PRE} \cdot K_{VDTC} \cdot I_{CP} \cdot f_S}{C_C}. \tag{14}$$

The clock frequency f_S continues to change depending on the load current. However, since f_S does not appear in the expression of poles and zeros, the change in f_S does not affect the locations of poles and zeros. It only affects A_{OL}, and, as a result, the loop gain and UGBW of the LDO are proportional to f_S. Fig. 13(b) shows the frequency response plot of the design. f_S is higher for a static load current, which

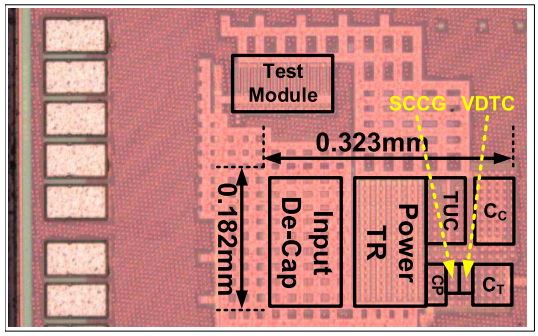

Fig. 14. Die micrograph.

results in a wider UGBW of the LDO and makes the LDO quickly react to a load current change. On the other hand, if the load current changes abruptly, the clock signal slows down temporarily until the output voltage V_{OUT} follows V_{REF} again. In this case, the phase margin is enlarged, improving the stability of the LDO during V_{OUT} recovery.

V. Measurement Results

The proposed LDO was fabricated in a 65-nm low power (LP) CMOS process. For direct output feedback, we used a 7.2-pF MIM capacitor as C_C and a 0.2-pF MIM capacitor as C_T in VDTC. If the gate capacitance of the power transistor is included, the effective value of C_C increases to 10 pF. We used low-Vt transistors in most circuits, including power transistors, while high-Vt transistors are used in skewed inverter circuits. The die micrograph is shown in Fig. 14. The LDO occupies an area of 0.059 mm^2, including decoupling capacitor of V_{DD} and excluding I/O pads and test circuits. Excluding power transistors and input decap, the area of the controller and C_C in our design is 0.0195 mm^2. When estimated using the chip micrograph in [6], which presents an analog LDO in a 180-nm CMOS process, the area excluding the power transistor is approximately 0.208 mm^2. The LDO design in [20] is implemented in a 65-nm CMOS process, and the controller area, including C_C, is 0.035 mm^2. Compared with these studies, the proposed LDO design requires a smaller area to implement the controller.

When testing an on-chip LDO using an external load current source, it is very difficult to guarantee that the LDO actually sees an output load change with the desired slew rate due to line resistance, inductance, and parasitic capacitance in I/O cells, wirebonds, packages, and printed circuit board (PCB) traces [21]. This is a critical issue when testing on-chip LDOs since these parasitic components do not contribute when the LDO drives another block on the same die. Therefore, we implemented an on-chip test circuitry to obtain the actual transient characteristics of the LDO accurately.

To verify the performance of a voltage regulator in terms of fast transient responses, we employ the test circuit shown in Fig. 15. The test circuit is designed in a way that the load current can have a slew rate of over 100 mA/ns, which is the target value, even in the worst case considering process variations. The test circuit consists of four load switches, which can be turned on and off using the LOAD_SEL signal. V_{LOAD} is the power supply of the logic driving the load switch

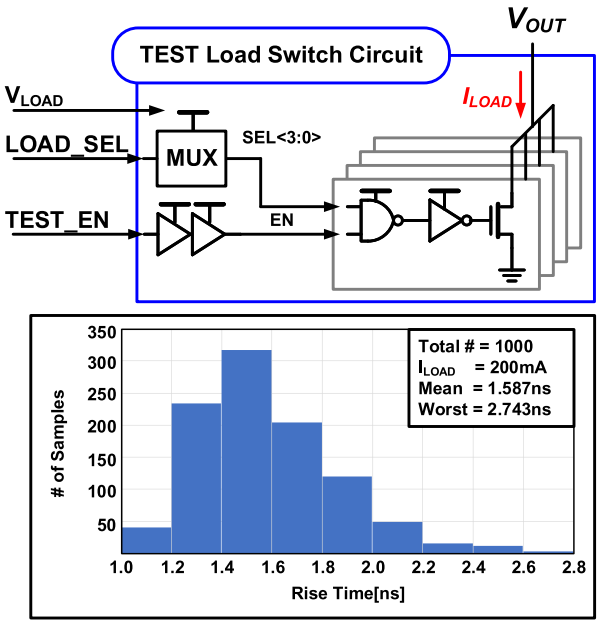

Fig. 15. Test circuit structure and Monte Carlo simulation results.

as well as the gate voltage of the load switch. TEST_EN is a signal that turns on the NMOS load circuits. We can control the load current by turning on and off TEST_EN after setting LOAD_SEL and V_{LOAD} in advance. It is designed to have a slew rate of 100 mA/ns or more in the worst case for V_{LOAD} of 1.2 V, and the slew rate can be lowered by adjusting V_{LOAD}. Since each load switch has a dedicated driver, the slew rate is guaranteed even if the load current increases or decreases by adjusting the number of switches through LOAD_SEL. Fig. 15 shows the results of Monte Carlo simulations using a postlayout netlist with extracted parasitics and the estimated I/O cell and wirebonding parasitics, confirming that the circuit reliably generates 200 mA/3 ns or higher slew rate, which is required for testing our design.

Fig. 16 shows the measurement results with SCCG turned on and off, which demonstrates the effectiveness of adaptive clocking using SCCG. It optimizes both clock frequency and duty cycle; hence, it shows significantly better responses than external clocks with the clock frequency ranging from 10 to 50 MHz and a 50% duty cycle. Our design also outperforms the optimal clock setting obtained by exhaustive search (45 MHz, 25% duty cycle). With SCCG, the settling time T_{SETTLE} is 1.5 μs when operating with V_{IN} of 1.0 V, V_{OUT} of 0.85 V, and a load current change of 200 mA/3 ns. Fig. 17 shows the measured load transient responses with both SCCG and TUC turned on. Compared to when TUC is turned off, the undershoot is reduced by 120 mV, confirming the effectiveness of TUC circuit. T_{SETTLE} is also significantly decreased from 1.5 μs to 20 ns.

Fig. 18 shows the measured load transient responses with 50-mV dropout voltage and both SCCG and TUC turned on. With 0.9-V V_{IN}, 0.85-V V_{OUT}, and a load current change of 75 mA/1 ns, the undershoot of V_{OUT} is measured at 135 mV [Fig. 18(a)]. With 0.5-V V_{IN}, 0.45-V V_{OUT}, and a load current change of 20 mA/1 ns, the undershoot of V_{OUT} is measured at 75 mV [Fig. 18(b)]. Fig. 19 shows an example

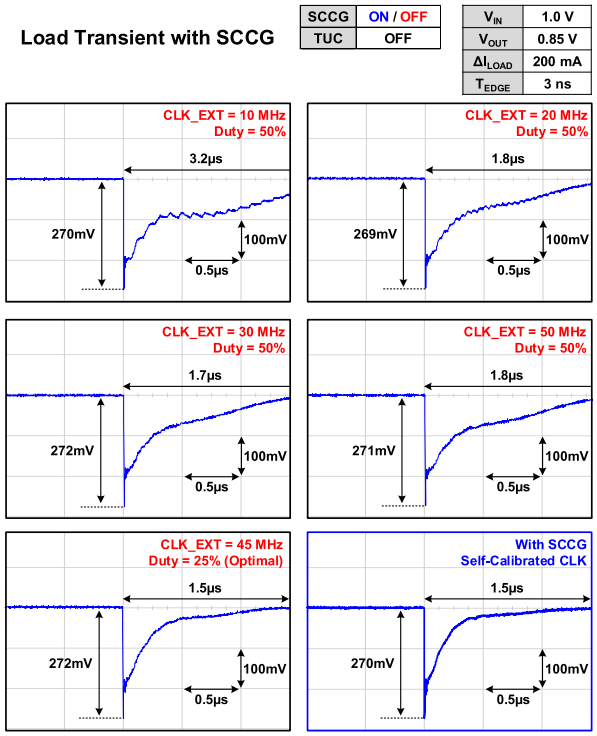

Fig. 16. Measured load transient responses with SCCG.

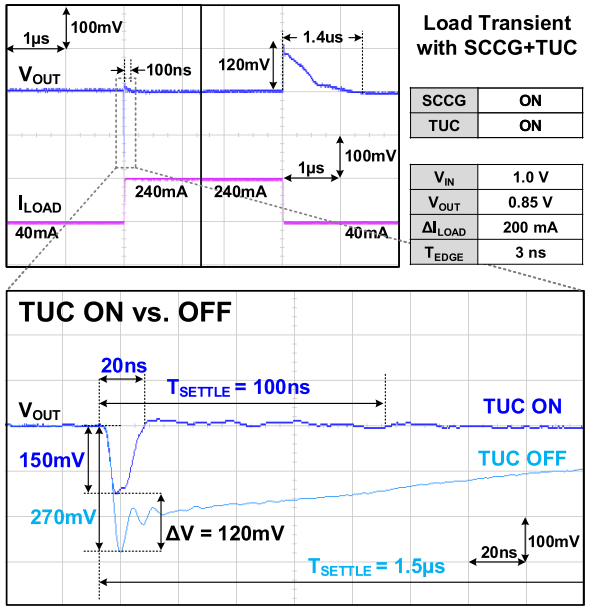

Fig. 17. Measured load transient responses with SCCG and TUC.

of measured transient responses with different TUC tuning codes. In Fig. 19(a), the output was measured while changing N to adjust the undershoot detection point, and optimal compensation was achieved with the code 011. In addition, the amount of TUC compensation can be selected by adjusting A, and the undershoot is effectively compensated with the code 000 [Fig. 19(b)]. Fig. 20(a) shows the measurement results with different load current changes while maintaining the slew rate. The amount of undershoot is nearly identical in all experiments, suggesting that TUC properly operates. On the other hand, Fig. 20(b) shows the measurement results when the slew rate is altered. It can be seen that TUC is not activated

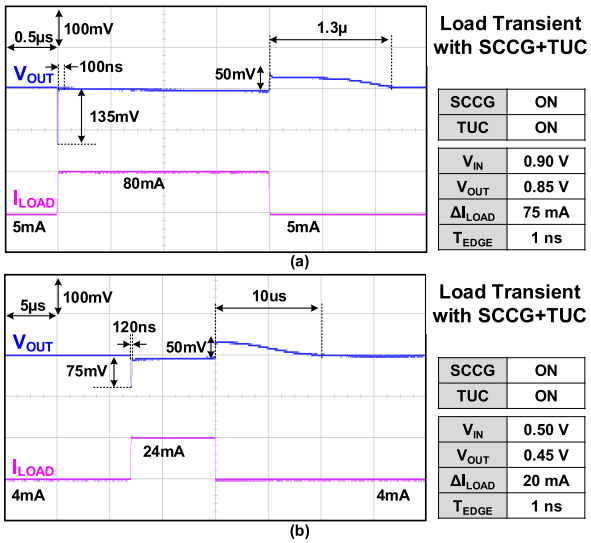

Fig. 18. Measured load transient responses with 50-mV dropout: (a) V_{IN} = 0.9 V and V_{OUT} = 0.85 V and (b) V_{IN} = 0.5 V and V_{OUT} = 0.45 V.

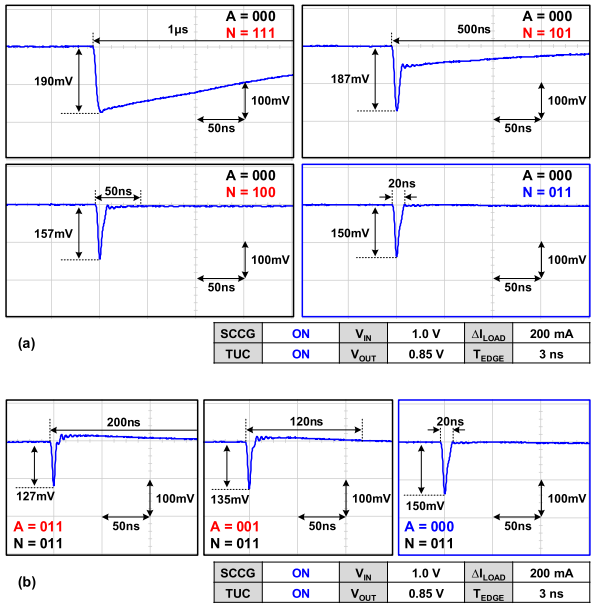

Fig. 19. Measured transient responses with different TUC tuning codes. (a) Resistor ratio N. (b) Pull-down Strength A.

for a low slew rate of 60 mA /10 ns. These results demonstrate that TUC effectively compensates for undershoot as intended.

The measured load regulation is shown in Fig. 21(a). The maximum load current that satisfies 0.5% load regulation error is 270 mA. The measurement results in Fig. 21(a) are obtained when the dropout voltage (V_{IN}–V_{OUT}) is fixed at 100 mV. Since V_{GS} of the PMOS power transistor determines the load current and the minimum value of V_G is zero (i.e., ground), the maximum load current would be proportional to V_{IN} (and hence V_{OUT}) when the dropout voltage is fixed. Fig. 21(b) shows the measured line regulation, where V_{IN} is lowered until V_{OUT} reduces by 0.5%. The input and output voltage ranges are 0.5–1.2 and 0.15–1.15 V, respectively. The quiescent current is measured at 1.05–12.7 μA, as shown in Fig. 21(c). Using SCCG noticeably reduces quiescent current compared to when SCCG is turned off and an external clock is applied. The measured current efficiency with respect to V_{IN}

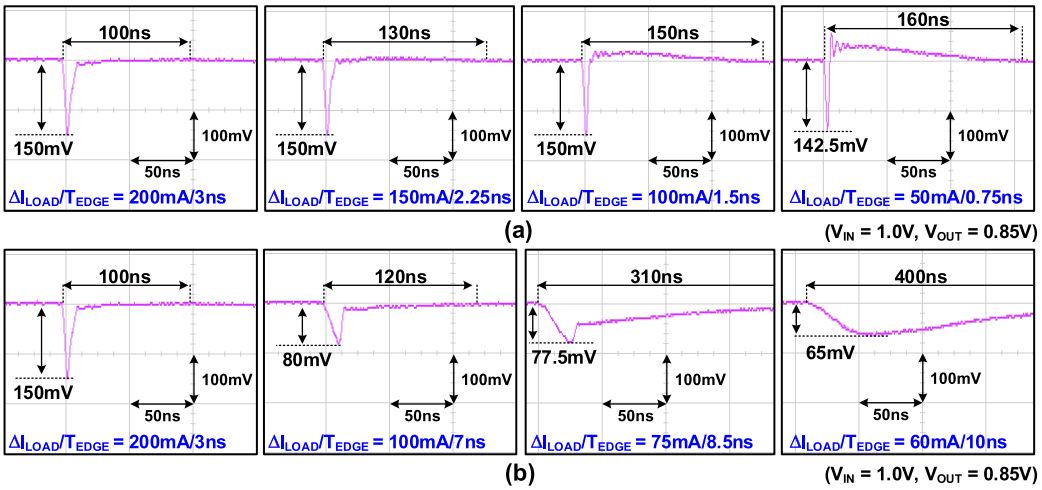

Fig. 20. Measured transient responses with various load current step conditions: (a) fixed slew rate and (b) varying slew rate.

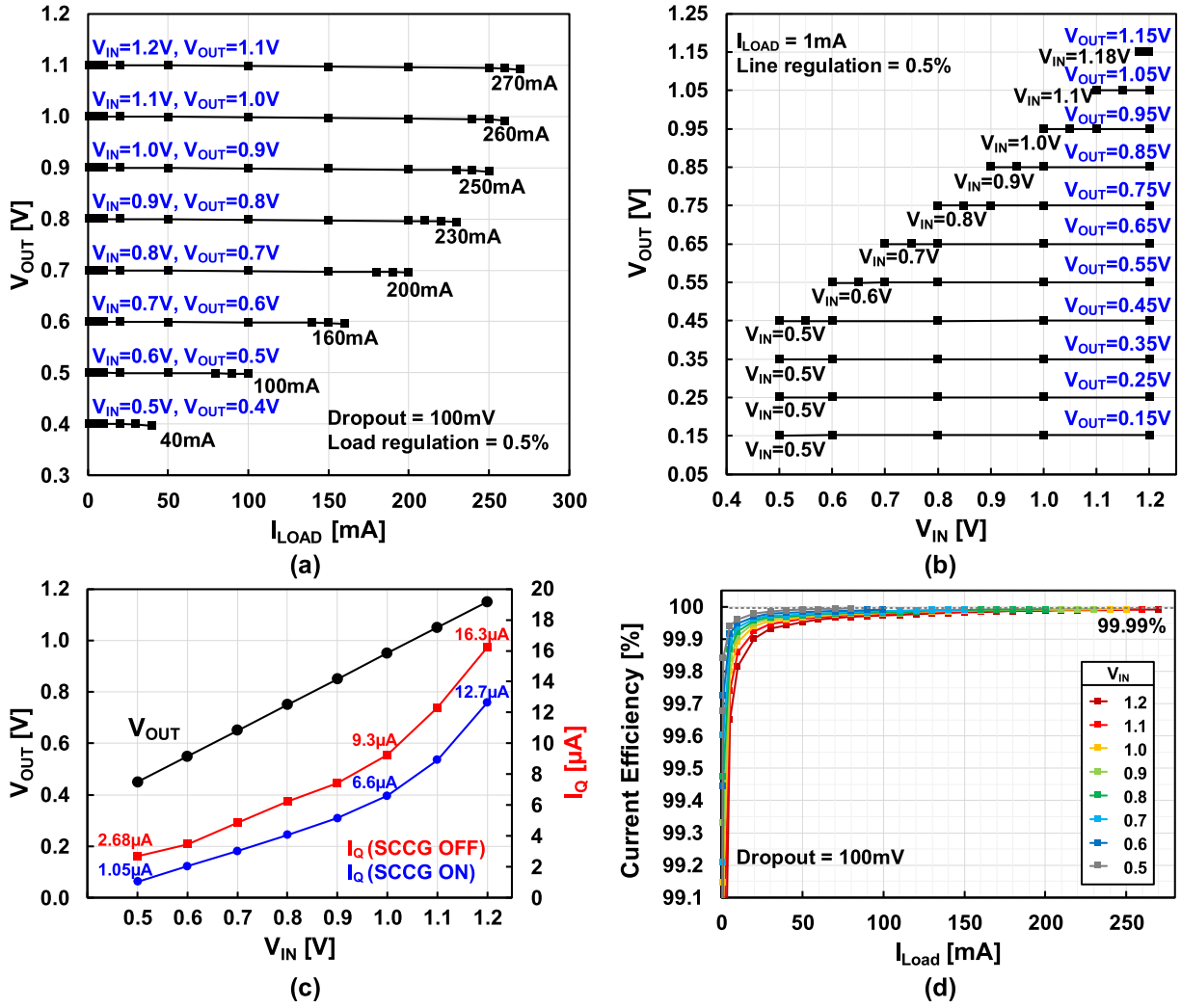

Fig. 21. Measurement results: (a) load regulation, (b) line regulation, (c) quiescent current, and (d) current efficiency.

is shown in Fig. 21(d), demonstrating the peak efficiency of 99.99%.

Fig. 22 shows the measured line transient response at 0.8-V V_{OUT}. When V_{IN} changes from 0.9 to 1.1 V with 100-mV/10-μs slew rate, there is no undershoot or overshoot observed in V_{OUT}. The measured power supply rejection ratio (PSRR) is shown in Fig. 23. When V_{OUT} is 0.5 V and the load current is 10 and 100 mA, the measured PSRR is below -30 dB up to 1 kHz and below -15 dB up to 100 kHz. For all V_{IN} values with a 10-mA load, the measured PSRR is below -28 dB up to 1 kHz and below -15 dB up to 100 kHz. Fig. 24 shows the measured output spectral noise density with

TABLE I

PERFORMANCE SUMMARY AND COMPARISONS WITH PRIOR WORKS

	[11] JSSC '17	[9] ISSCC '20	[13] ISSCC '18	[14] ISSCC '19	[15] ISSCC '17	[20] JSSC '20	[16] TCAS-II '21	**This Work**	
Process (nm)	65	28	28	14	28	65	65	**65**	
Type	Digital	Digital	AA−Digital	Hybrid	Class−D	CP+DCHZ	VDTC+CP	**VDTC+CP**	
V_{IN} (V)	0.5−1.0	0.5−1.0	0.4−0.55	1.0−1.2	1.2−1.8	0.5−1.0	0.6−1.2	**0.5−1.2**	
V_{OUT} (V)	0.45−0.95	0.45−0.95	0.35−0.50	0.7−0.85	1.05	0.45−0.95	0.5−1.15	**0.15−1.15**	
Maximum I_{OUT} (mA)	3.511	480	20.5**	530	1000	105	60	**270**	
I_Q (μA)	12.5−216	7.7−241	>0.81	31.1−53.5	152	4.9	0.1−10	**1.05−12.7**	
C_{OUT} (pF)	400	Cap-free	Cap-free	4000	1000000	Cap-free	Cap-free	**Cap-free**	
C_{TOTAL} (pF)	-	4.11	24	-	-	42	10	**7.4**	
Peak Current Efficiency (%)	96.3	99.99	-	99.99	-	99.99	99.99	**99.99**	
Total Area (mm^2)	0.029	0.049	0.0055	0.262	0.058	0.04	0.083	**0.059**	
Current Density (A/mm^2)	0.121	9.8	3.73	2.023	17.24	2.625	0.723	**4.75**	
Tested V_{IN} / V_{OUT} (V)	0.5 / 0.45	0.9 / 0.85	0.5 / 0.45	1.1 / -	1.35 / 1.05	0.6 / 0.5	1.2 / 1.1	**1.0 / 0.85**	**0.9 / 0.85**
T_{EDGE} (ns)	0.1	2	3	<0.5	500	1	1	**3**	**1**
$\triangle I_{LOAD}$ (mA)	0.4	430	20	508	1000	100	50	**200**	**75**
$T_{SETTLE(Undershoot)}$ (ns)	80000	310	9000	400	-	62	100	**100**	**100**
V_{DROOP} (mV)	40	112	117	133	40	185	100	**150**	**135**
FoM_1 (fs)	1250000	0.41	5.7	67	6080	3.8	4.04	**0.183**	**0.915**
FoM_2 (fs)	125000**	0.82	17.1	83	3040000	3.8	4.04	**0.549**	**0.915**

$$FoM_1 = C_{TOTAL} \cdot \left(\frac{I_Q}{\triangle I_{LOAD}}\right) \cdot \left(\frac{V_{DROOP}}{\triangle I_{LOAD}}\right)$$

$$FoM_2 = C_{TOTAL} \cdot \left(\frac{I_Q}{\triangle I_{LOAD}}\right) \cdot \left(\frac{V_{DROOP}}{\triangle I_{LOAD}}\right) \cdot \left(\frac{T_{EDGE}}{1ns}\right)$$

**Estimated from figure

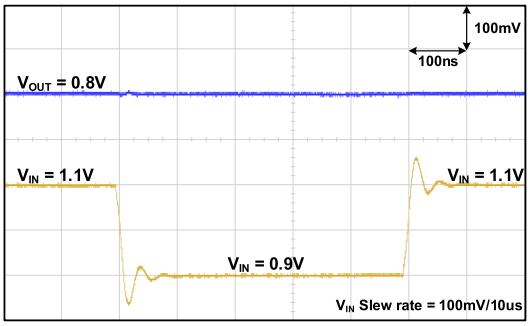

Fig. 22. Measured line transient responses.

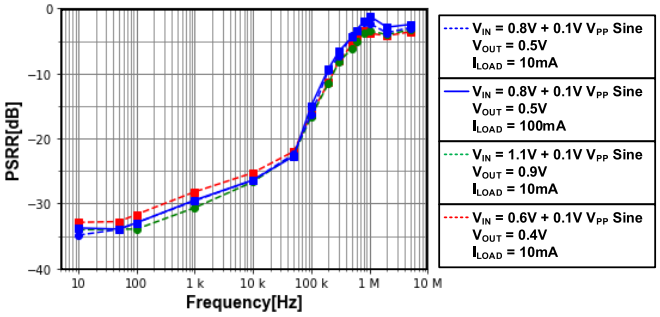

Fig. 23. Measured PSRR.

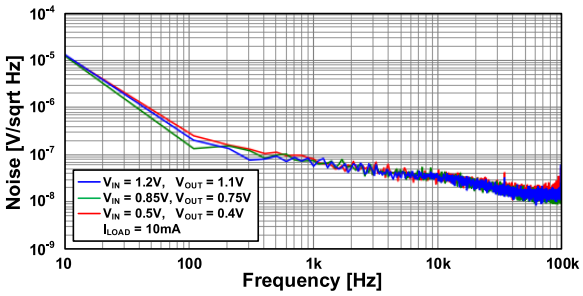

Fig. 24. Measured output spectral noise density.

a 10-mA load current at different V_{IN} levels. The noise is measured less than 10^{-6} V/$\sqrt{\text{Hz}}$ at 100 Hz and higher, and it does not significantly vary with V_{IN}.

Table I summarizes the performance of the proposed LDO and compares the design with prior works. Due to the rail-to-rail VDTC structure, our design exhibits the widest output voltage range. The LDO also achieves a very small quiescent current due to the energy-efficient VDTC and adaptive clocking, even compared to digital LDOs [9], [11]. Moreover, our design achieves fast settling speed and the lowest figure of merit (FoM). Note that FoM_1 used in Table I is calculated using the total capacitance, the quiescent current divided by the load current change, and the voltage droop divided by the load current change. FoM_2 additionally includes the slew rate of the load current change. FoM_1 represents the absolute transient response performance, whereas FoM_2 allows for accurate comparison of transient response performance regardless of the magnitude of the driving load current by additionally considering slew rate. Comparisons show that our design achieves the lowest FoM_1 and FoM_2. Our design was measured to have the current density of 4.75 A/mm^2, which is the third best value after the designs in [9] and [15]. These results confirm the effectiveness of the proposed LDO design. Note that our design exhibits inferior FoMs at 50-mV dropout voltage, but this is due to the fact that our design is optimized for higher dropout voltage of 100–150 mV. If we were to design the LDO for 50-mV dropout voltage, we could double the size of the power transistor so that our design exhibits a better FoM in the same condition, at the

expense of area increase. In postlayout simulations including the estimated I/O cell and wirebonding parasitics, the modified design with a double-size power transistor exhibits FoM_1 of 0.0678 fs and FoM_2 of 0.203 fs for $V_{\text{IN}} = 0.9$ V and $V_{\text{OUT}} = 0.85$ V, $\triangle I_{\text{LOAD}} = 300$ mA, and $T_{\text{EDGE}} = 3$ ns, outperforming prior designs. This modification increases the area by 28.5% and results in the maximum load current of 400 mA, which translates to the current density of 5.296 A/mm^2.

VI. Conclusion

In this article, we presented a wide-range energy-efficient LDO that does not require external capacitors and clocks. The rail-to-rail VDTC circuit enables a wide output voltage range, and the adaptive clocking scheme using SCCG optimizes the clock frequency in real time, effectively mitigating PVT variation and load current change. As a result, our design maximizes energy efficiency while securing optimal transient responses in not only the steady state but also the in the dynamic state. The TUC circuit further improves the transient response under a sharp load current increase by detecting a voltage droop in the output, also mitigating the effect of process variation through additional tuning circuitry. Combining all the design techniques described above, the design achieves 0.183-fs FoM_1 and 0.549-fs FoM_2, which outperforms prior arts.

Acknowledgment

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