An All-Standard-Cell-Based Synthesizable SAR ADC With Nonlinearity-Compensated RDAC

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***Abstract*— We propose an all-standard-cell-based synthesizable successive-approximation-register analog-to-digital converter (SAR ADC) which is automatically placed and routed (P&R) using a commercial digital implementation tool. For higher feasibility and wider input range, a differential architecture is proposed with an inverter-based resistive digital-to-analog converter (RDAC) and a four-input comparator. MOSFET gate capacitance is employed for the sampling capacitor. To mitigate its capacitance variation due to input voltage and the leakage between gate and diffusion, we leave the diffusion of the standard cell floating and only use the capacitance between gate and bulk. Two prototypes have been designed in 65-nm bulk CMOS. Prototype I has been fabricated and achieves 10 MS/s, 14.3 mW, and 28.1-dB SNDR in a 6-bit architecture. The performance is improved in Prototype II by proposing a lookup table (LUT)-compensating transistor-configurable inverter-based RDAC and an OR-AND-Inverter (OAI)-based comparator and by employing a thick-oxide diffusion-floating decoupling cell for the sampling capacitor. The default LUT is created during the design phase by a script-controlled automatic simulation routine. The power consumption is significantly reduced as well through improved timing control. Layout-parasitic-extraction (LPE) simulations of Prototype II suggest 35.7- and 47.2-dB SNDRs in 6- and 8-bit versions, respectively. The power consumptions are reduced to 0.91 and 2.52 mW, respectively.**

***Index Terms*— Resistive DAC (RDAC), standard cell, synthesizable, synthesizable successive-approximation-register analog-to-digital converter (SAR ADC).**

I. Introduction

GROWING industries increasingly demand a tremendous number of microchips which nowadays are involving with more and more digital and digitally assisted analog circuits. Digital circuits are typically described in register transfer level (RTL) netlist and placed and routed (P&R) in an automatic flow. They can be fast realized and modified to adapt to different specifications and process technologies. This feature, however, is rarely found in analog circuits. Despite a small portion in a system, analog or mixed-signal circuits often take long time to design. Moreover, to suit the existing design to another specification or process technology, the required redesign time is typically as long as the previous one.

To reduce the design or redesign time of analog circuits, synthesizable solutions using standard cells have been proposed. In these solutions, generally, analog circuits are described in RTL netlists and automatically laid out in digital P&R flows. Recent works have succeeded in time-to-digital converters (TDCs) [1]–[3], phase-locked loops (PLLs) [4]–[11], low-dropout (LDO) regulators [12]–[14], and analog-to-digital converters (ADCs) [15]–[24]. As the interface between the real world and digital signal processing, ADCs are widely needed in sensor and radio frequency systems. In most development scenarios, they should be specifically designed according to system requirements, inevitably requiring long design time. Their design automation—unlike TDCs, PLLs, and LDOs that are mainly in a manner of time-domain circuits—can be more challenging due to the necessity to deal with voltage-domain signals by manipulating standard cells.

A standard-cell library lacks available components to realize two-port resistors and operational amplifiers. Thus, conventional flash, pipeline, and $\Delta\Sigma$ architectures are less possible to be implemented. To circumvent this issue, stochastic ADCs were proposed, but the thousands of NAND comparators result in large area and high power [15], [16], [25]. Prior to them, a domino-logic-based ADC with custom-designed cells and manual layout was presented in [26]. In another work on a voltage-controlled oscillator-based (VCO-based) ADC [27], only standard cells were employed, but the circuit layout was done manually. By registering custom-designed cells to a physical library, automatic P&R flows for analog circuits were introduced [17], [19], [23], [24], [28]. Also, hybrid methods for successive-approximation-register (SAR) ADCs were proposed with SKILL language for capacitive digital-to-analog converter (CDAC) generation [29], [30]. The two works have achieved high performance at the cost of more implementation complexity.

An SAR ADC can be suitable for synthesis owing to its simple and digital-intensive architecture. A single-ended all-standard-cell-based SAR ADC with an OR-AND-Inverter (OAI)-based DAC was proposed in [21]. However, its signal

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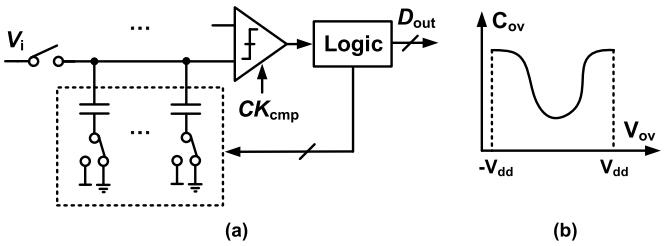


Fig. 1. (a) Conventional custom-designed SAR ADC. (b) Voltage dependence of MOSFET capacitance.

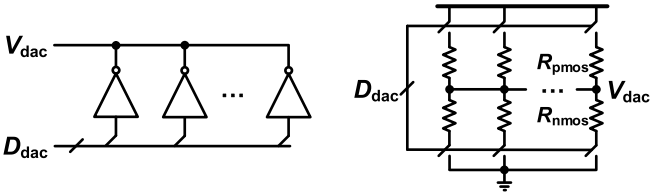


Fig. 2. Proposed inverter-based RDAC for synthesizable SAR ADC.

bandwidth is limited since the sample-and-hold (S/H) circuit is not implemented. Dyadic-digital-pulse-modulation (DDPM) DACs are proposed for synthesizable SAR ADCs in [22]. Still, they suffer from limited speed because the DACs require exponentially more cycles for output generation. In [20], we proposed a differential all-standard-cell-based SAR ADC using a floating-diffusion S/H circuit, an inverter-based resistive DAC (RDAC), and a four-input comparator. In this article, we detail the design in Prototype I and propose the improving techniques for higher performance in Prototype II. Prototype I is evaluated on silicon, and Prototype II is verified through simulations in layout-parasitic-extraction (LPE) comprising resistors and capacitors.

II. Synthesizable SAR ADC

An SAR ADC in a custom design typically consists of an S/H circuit which also operates as a CDAC, a dynamic comparator, and SAR logic, as shown in Fig. 1(a). Since the comparator and the logic can be realized using standard cells, one may naturally consider replacing the CDAC with MOSFET capacitors seen from the gate nodes of logic or decoupling cells. The following issues, however, cause the replacement less feasible: 1) MOSFET capacitance varies with gate-diffusion voltage, as shown in Fig. 1(b), which may lead to unpredictable errors during binary searching based on charge redistribution; 2) two-port capacitor and especially its array are uneasy to implement using a digital P&R tool; and 3) even though 2) is available, the parasitic capacitance of routing wires cannot be controlled as in custom layout, which undermines the linearity.

Due to these issues, we separate the S/H and DAC and let the capacitor work only for sampling. The binary searching is carried out via a resistive DAC, as shown in Fig. 2. Compared with the OAI-based DAC in [21], the inverter-based one features simple architecture with a similar level of performance. PMOS or NMOS transistors are turned on according to the input codes and form a voltage divider.

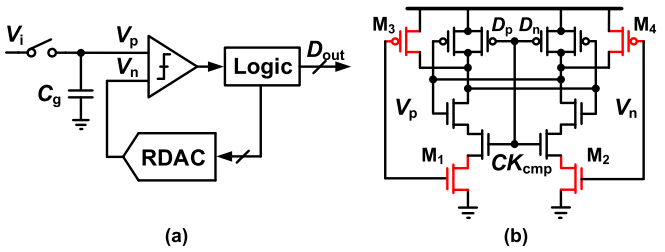


Fig. 3. (a) Possible single-ended solution, where the comparator's input common mode changes during conversion. (b) Conventional standard-cell comparator and its limited input range issue.

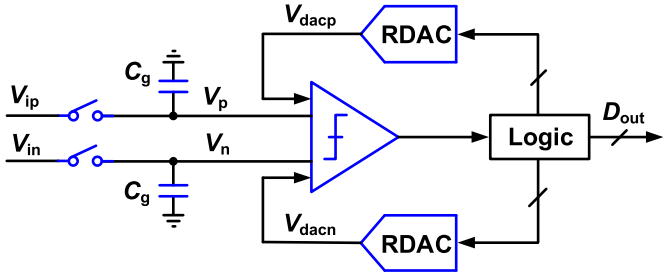


Fig. 4. Proposed differential all-standard-cell synthesizable SAR ADC.

The output voltage is calculated as

$$V_{\rm dac} = \frac{2^N - 1 - D_{\rm dac}}{2^N - 1 + (\alpha - 1)D_{\rm dac}} \tag{1}$$

where $\alpha = (R_{\rm pmos}/R_{\rm nmos})$. If the resistance of PMOS and NMOS transistors is equivalent, i.e., $\alpha = 1$, then

$$V_{\rm dac} = \frac{2^N - 1 - D_{\rm dac}}{2^N - 1} \tag{2}$$

which suggests a linear relation between $D_{\rm dac}$ and $V_{\rm dac}$. In practice, $\alpha \neq 1$ and varies with $V_{\rm dac}$ that determines transistors' drain–source voltage. Consequently, this inverter-based RDAC exhibits high nonlinearity. The proposed methods to compensate the nonlinearity for moderate resolution will be described in Sections III and V.

Employing this RDAC, one can possibly derive a single-ended architecture, as shown in Fig. 3(a). Since the MOSFET gate capacitor is only used for S/H, the issue of the voltage-dependent capacitance during binary searching is avoided. Although the capacitance still varies with input voltage that affects the bandwidth of the sampler, this effect can be mitigated with sufficient design margin and the floating-diffusion capacitor, which will be introduced in Sections III-C and V-C. The major issue of this architecture is the limited input range because the input common-mode voltage ($V_{\rm cm}$) of the conventional NAND-based comparator changes during conversion. As shown in Fig. 3(b), when $V_{\rm cm}$ becomes too low, M_1 and M_2 are turned off. Thus, the currents flowing through two paths are cut off, and the upper transistors are disabled, resulting in uncertain output. If $V_{\rm cm}$ is too high, transistors M_3 and M_4 go to the subthreshold region, and the effect of their mismatch can drastically increase.

Different from the NAND+ NOR comparator in [21], to solve this issue, we propose a differential architecture, as shown in Fig. 4. Here, $V_{\rm p} - V_{\rm n}$ and $V_{\rm dacp} - V_{\rm dacn}$ are differential pairs,

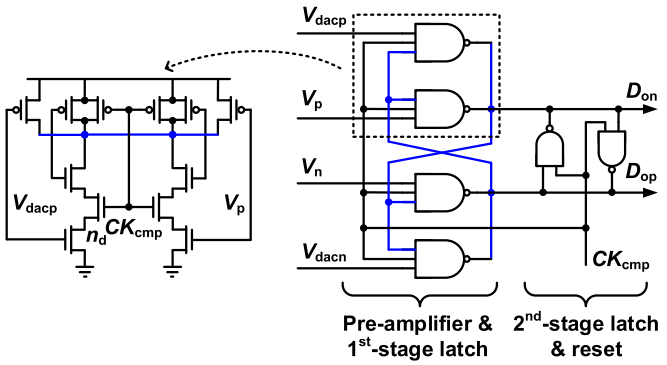


Fig. 5. Proposed four-input NAND-based comparator for Prototype I.

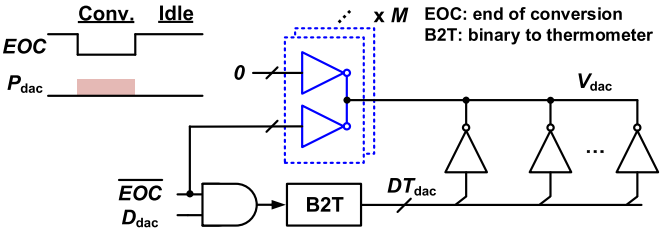


Fig. 6. RDAC in Prototype I with attenuating inverters and gating control.

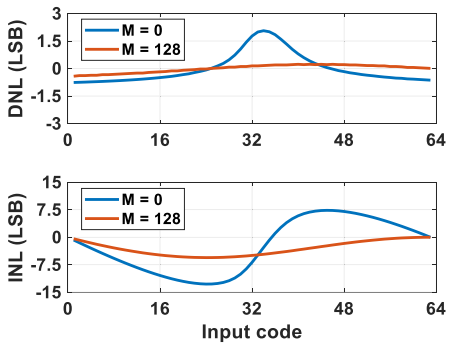


Fig. 7. Simulated DNLs and INLs of 6-bit RDAC in Prototype I without and with 128 attenuating inverters.

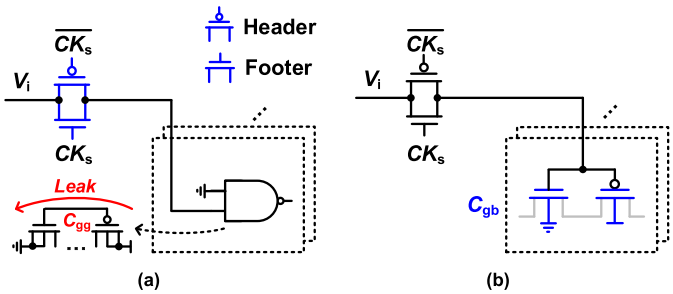


Fig. 8. (a) Leakage issue of MOSFET gate capacitor. (b) Sample-and-hold circuit in Prototype I with floating diffusion against leakage.

respectively, and their V_{cm} is fixed at $V_{dd}/2$. The comparator is extended to a four-input structure which will be described in Sections III-A and V-A. The differential architecture is also beneficial to the suppression of common-mode noise. The design and evaluation of building blocks will be described in Sections III–VI. In brief, Prototype I evaluated on silicon achieves 10 MS/s, 14.3 mW, and 28.1-dB SNDR in a 6-bit architecture; Prototype II verified with LPE netlists suggests 10 MS/s, 0.9 mW, and 35.5-dB SNDR in a 6-bit version, and 10 MS/s, 2.5 mW, and 46.5-dB SNDR in an 8-bit version. Thanks to the synthesizable design methodology, it is agile and straightforward to modify the architecture from 6 to 8 bit.

III. Circuit Design of Prototype I

A. Four-Input nand-Based Comparator

A NAND-based comparator can be interpreted as a preamplifier, a latch, and clock switches. To create a four-input comparator, we feed back the shorted output of one pair of the preamplifiers to the input of the other pair, similarly as in a custom design, as shown in Fig. 5. Here, $V_p + V_{dacp}$ and $V_n + V_{dacn}$ are compared. Two NAND2 cells at the output operate as a 2nd-stage latch to enhance the gain during comparison. Before and after comparison, they help reset the outputs.

B. Inverter-Based RDAC

As previously discussed, the inverter-based RDAC shown in Fig. 2 suffers from nonlinearity because α varies with V_{dac}. To attenuate this effect, in Prototype I, auxiliary inverters are introduced, as shown in Fig. 6. Half of the inverters are fed with 0 and the other half are with 1 to turn on their PMOS and NMOS transistors, respectively. In this way, the variation of α is suppressed. To lower the power consumption, the RDAC is only active during conversion when the end-of-conversion (EOC) signal is low. After that, logic 0 is sent to all the inverters to cut off the static current. Fig. 7 shows simulated DNLs and INLs of a 6-bit RDAC. It can be seen from the figure that the peak INL is reduced from 8.2/−12.6 LSB to 1.0/−5.0 LSB when 28 attenuating inverters (with the same unit size as in the DAC) are added.

C. Sample-and-Hold (S/H) Circuit

While it is possible to implement metal-oxide-metal (MOM) sampling capacitors using SKILL language [29], [30] or p-cell initialization by the script in a digital P&R flow [22], to mitigate implementation complexity, and to explore the possibility of an all-standard-cell-based ADC, we implement the sampling capacitor using MOSFET gate capacitance in this work. As shown in Fig. 8, in Prototype I, we use header and footer power-gating cells to make a transmission gate as the sampling switch. As for the capacitor, a conventional method is the employment of a NAND gate with one input connecting to 0 to cut off the short-circuit current, as shown in Fig. 8(a). This capacitor, however, cannot steadily hold the sampled voltage because of the leakage between the gate and diffusion. To solve this issue, we leave the power and ground ports (i.e., the diffusion) of the cell floating but retain the connections of the substrate and well. Thereby, only the gate-bulk capacitance is utilized without suffering from the leakage. Since the power and ground nodes are floating, we can replace the NAND gates with inverters for smaller area, as shown in Fig. 8(b).

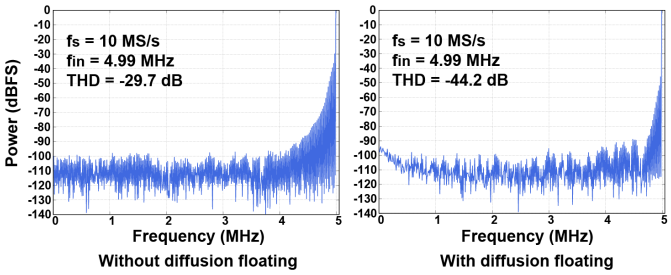


Fig. 9. Simulated THDs of Prototype I where S/H is in LPE and other building blocks are in ideal Verilog-A/HDL.

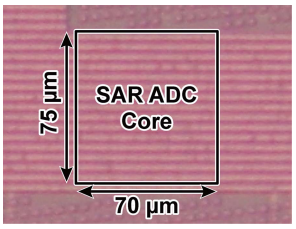


Fig. 10. Chip micrograph of Prototype I.

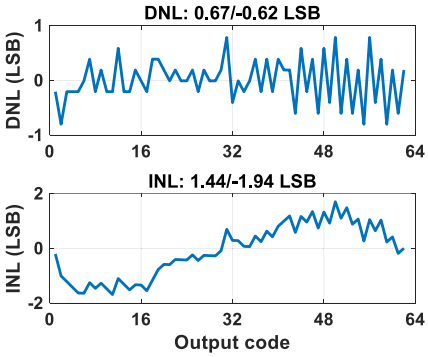


Fig. 11. Measured DNL and INL of Prototype I.

Fig. 9 shows simulated total harmonic distortions (THDs) of Prototype I where the S/H is in LPE and other building blocks are in ideal Verilog-A/HDL. With diffusion floating, the result suggests −44.2-dB THD, adequate to 6-bit resolution, whereas without diffusion floating, the THD degrades to −29.7 dB.

IV. Experimental Results of Prototype I

Prototype I is designed in a typical synthesizable mixed-signal circuit flow, where the digital part is synthesized, and the analog part is described in gate-level RTL. The P&R is carried out with a commercial digital automatic implementation tool. Fabricated in 65-nm bulk CMOS, the core area of Prototype I is 0.0051 μm^2. Fig. 10 shows the chip micrograph. Fig. 11 shows measured DNL and INL. The peak DNL and INL are 0.67/−0.62 LSB and 1.44/−1.94 LSB, respectively, consistent with the simulated RDAC linearity shown in Fig. 7. At 10-MS/s sampling rate and 1.0-V power supply, the measured power consumption is 14.3 mW. The power consumption can be lowered by improving the gating timing of

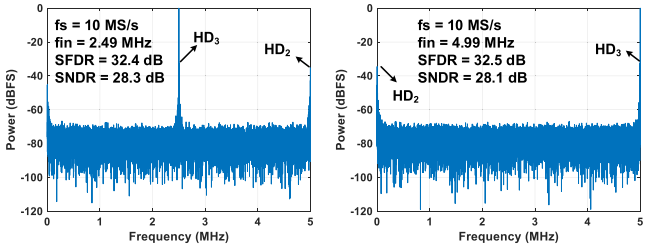


Fig. 12. Measured spectra of Prototype I.

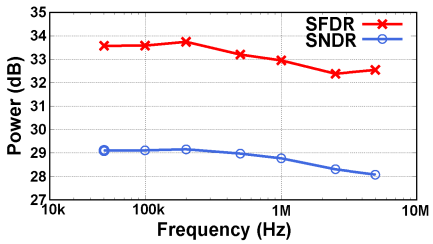


Fig. 13. Measured SFDR and SNDR with different input frequencies of Prototype I.

the RDAC, which will be described in Section V. Fig. 12 shows measured spectra with Nyquist-frequency (4.99 MHz) and half-Nyquist-frequency (2.49 MHz) inputs. Their measured SNDRs are 28.1 and 28.3 dB, respectively, and the former one translates to 4.4-bit ENOB and 67.73-pJ/step FoM. Fig. 13 shows the measured SNDR and SFDR versus input frequency. The performance comparison will be shown together with the results of Prototype II in Table I.

In summary, we designed and measured a 6-bit all-standard-cell-based synthesizable SAR ADC as Prototype I. Its power consumption and nonlinearity due to the nonidealities of analog building blocks need to be improved. With the architecture same as the one in Fig. 4, we improved the overall performance by proposing new solutions to these building blocks. This will be described in Sections V and VI.

V. Circuit Improvement in Prototype II

A. OAI-Based Four-Input Comparator

As previously mentioned, a NAND comparator can be interpreted as a complementary preamplifier connected to a latch in series. If the input voltage is lower than V_{th}, the NMOS transistors of the preamplifier are turned off. Although the proposed comparator shown in Fig. 5 receives fixed common-mode input, each input can still experience low voltage. In this case, when CK_{cmp} becomes low, the reset path of a preamplifier's NMOS transistor is cut off. Thus, residue charges at the drain node (n_d in Fig. 5) remain and are uncertain. Consequently, the resulting drain voltage difference can be amplified by the latch unexpectedly during the next comparison, leading to error output. This undermines ADC's linearity especially when the input amplitude is large.

To solve this issue, we replace NAND with OAI cells in order to add a reset path for the NMOS drain nodes of

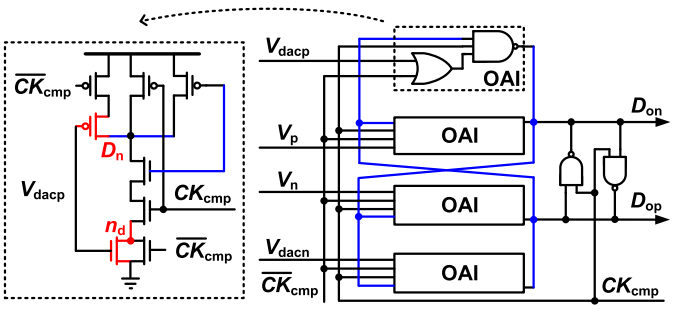


Fig. 14. Proposed OAI-based comparator where node n_d is reset by the adjacent transistor after comparison to eliminate residue charges.

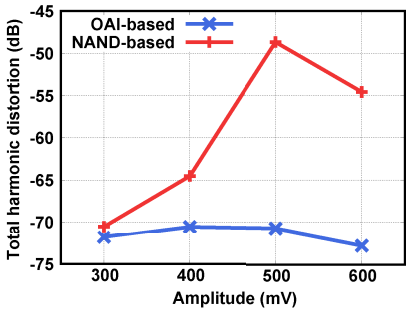


Fig. 15. Simulated ADC's THDs where comparators are in LPE and other building blocks are in ideal Verilog-A/HDL.

the preamplifier. As shown in Fig. 14, when a comparison is complete, node n_d is reset to V_{ss} by its adjacent turned-on transistor. Since the drain nodes of both PMOS and NMOS transistors of the preamplifier are reset before the next comparison, the probability of error output is greatly reduced. Fig. 15 shows simulated THDs of the SAR ADCs with NAND- and OAI-based comparators in LPE and other building blocks in ideal Verilog-A/HDL. When the input amplitude grows, the THD is kept below -70 dB with an OAI-based comparator, while it degrades to -50 dB with an NAND-based one.

B. Transistor-Configurable Inverter-Based RDAC With Automated Default Lookup Table (LUT) Creation in Design Phase

The feedback DAC dominates the overall ADC nonlinearity. Although we employed attenuating inverters to suppress the variation of the resistance, the linearity is still insufficient to realize moderate resolution. A natural consideration for the compensation is predistorting the input code using an LUT. Furthermore, it is demanded to separately turn on PMOS and NMOS transistors for higher compensation resolution. Based on these considerations, we proposed the improved RDAC, as shown in Fig. 16. We use two inverters for a unit, one with floating V_{dd} and the other one with floating V_{ss}. In this way, PMOS and NMOS transistors can be independently turned on. Hence, the resistors connecting to V_{dd} and V_{ss} become configurable, leading to higher compensation resolution. To realize the flowing V_{dd} and V_{ss}, two power-ground domains are defined for the macro during P&R. One domain is kept floating during the final P&R for the SAR ADC.

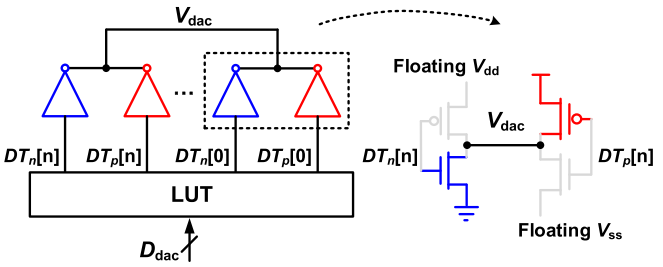


Fig. 16. Proposed transistor-configurable inverter-based RDAC, where PMOS and NMOS transistors can be independently turned on.

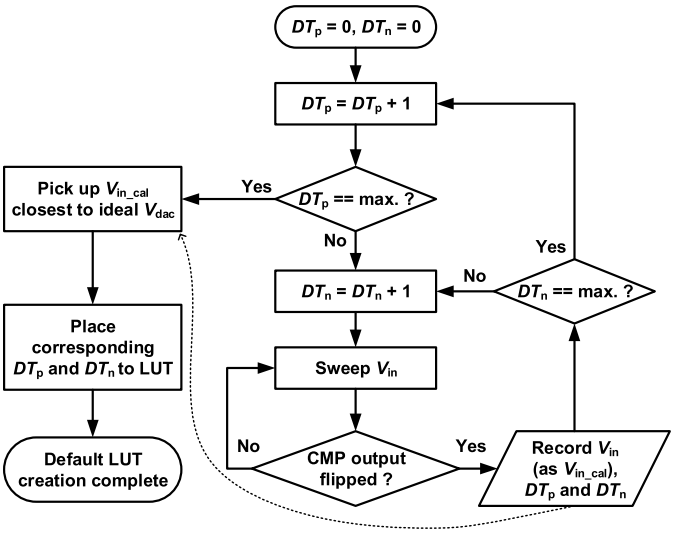


Fig. 17. Flowchart of script-controlled simulation-based default LUT creation.

The LUT as an encoder translates binary input code D_{dac} to predistorted thermometer codes DT_p and DT_n. A default LUT needs to be created during the design phase as a baseline of the nominal linearity performance. Since the SAR ADC is fully realized with standard cells, the design by transistor-level analysis and sizing should be avoided. However, it is also impractical to determine the LUT values one by one by a significant number of manual simulations. To fully leverage the power of computer-aided design automation, we developed a Python script to control the simulation-based determination routine automatically. As shown in Fig. 17, we sweep RDAC's input and tune the input reference ramp signal to track RDAC's output voltage according to their comparison result. Once the two voltages are close enough to flip the comparator's output, the input voltage is recorded as V_{in_cal} as well as DT_p and DT_n in one dataset. When the sweeping is completed, from the recorded datasets, we pick up V_{in_cal} that is closest to the expected ideal DAC's output voltage, and place DT_p and DT_n of that dataset into the default LUT. This sweeping and tuning process requires 2^{2N} times of simulations, where N is the DAC's nominal resolution. Thanks to the developed automatic routine, no tedious manual operation is required.

Fig. 18 shows 100-run Monte Carlo LPE simulation results of DNLs and INLs of 6- and 8-bit RDACs with their default LUTs, respectively. The mean values of peak DNL and INL

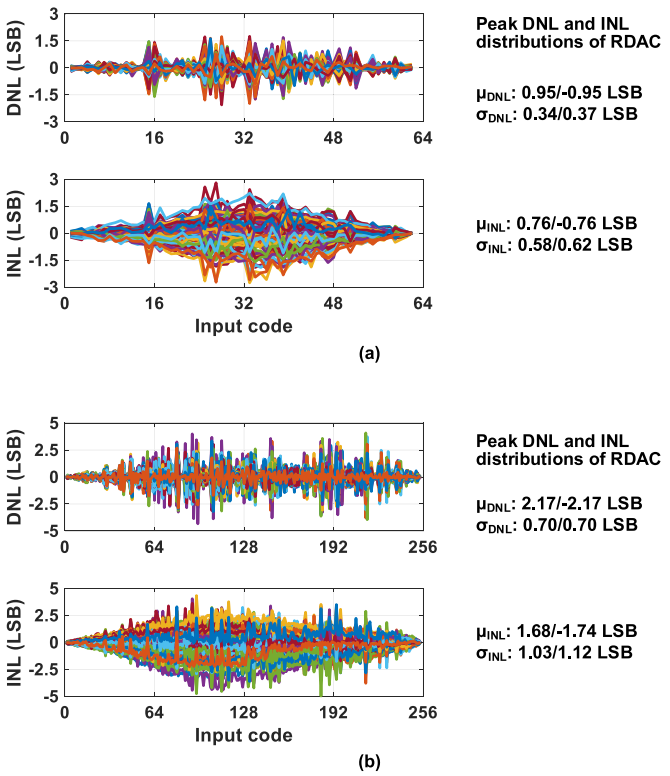


Fig. 18. 100-Run Monte Carlo LPE simulation results of (a) 6-bit and (b) 8-bit RDACs' DNLs and INLs with their default LUTs.

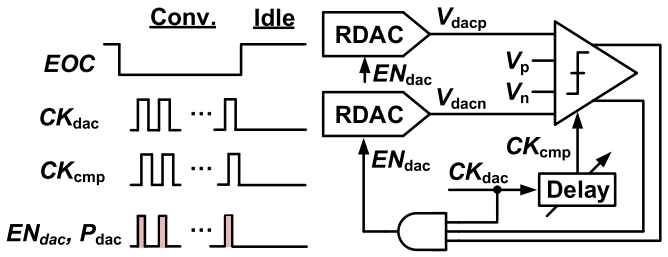


Fig. 19. Intermittent RDAC enabling control in Prototype II.

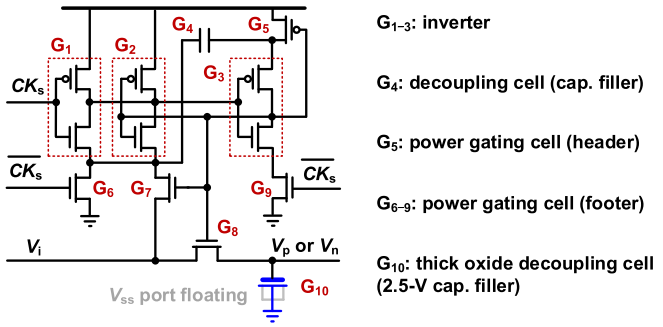


Fig. 20. Bootstrap S/H circuit [21] using thick-oxide decoupling cell with floating V_{ss}.

of the 6-bit RDAC are 0.95/−0.95 LSB and 0.76/−0.76 LSB, respectively. Their standard deviations are 0.34/0.37 LSB and 0.58/0.62 LSB, respectively. In the 8-bit one, the mean values of peak DNL and INL are 2.17/−2.17 LSB and 1.68/−1.74 LSB, respectively, and the standard deviations are 0.70/0.70 LSB and 1.03/1.02 LSB, respectively. It should be noted that the DNL exceeding −1 LSB in a DAC does not mean "missing code." From the peak INL distributions, we roughly estimate that, among 34% fabricated chips, the ENOB loss due to the RDAC nonlinearity and mismatch of the 6-bit ADC is less than 0.5 bit, while that of the 8-bit one is less than 1.5 bit. Of course, the performance can be improved by using larger size cells trading off with power consumption. It should also be noted that the LUT is possible to be configured externally for an actual chip by implementing a memory block like the all-standard-cell-based one in [31]. Then, similar automatic routine can be carried out on-chip or on-board to update the LUT values. A reconfigurable memory-based LUT also helps alleviate other process–voltage–temperature (PVT) variations at the cost of memory size and complexity. For example, an implemented 1024 × 1024 memory-based LUT following [31] occupies about 0.255 mm^2 additional area. Alternatively, if a memory library were provided, the synthesized SRAM would be much smaller. Also, if this ADC were incorporated in an SoC, sharing its memory would be a possible choice.

The 6- and 8-bit RDACs output root-mean-square (rms) thermal noises are also simulated in LPE. The peak rms noises are 0.51 and 0.36 mV, respectively, sufficiently low for their resolutions.

C. RDAC Enabling Control and Bootstrapped S/H Circuit With Floating Thick-Oxide Decoupling Cell

The power consumption of the RDAC in Prototype II is lowered with the improved enabling control scheme, as shown in Fig. 19. The RDAC is only enabled for bit comparison and is disabled when each comparison ends. The enable time is about 2 ns to cover the worst case RDAC settling time. Supposing a 5-ns-period CK_{dac} shown in the figure, the duty cycle of EN_{dac} is 40%. The average power can be saved by approximately 40% as well, compared with an RDAC activated during the whole conversion period.

The S/H circuit is modified to the bootstrapped structure [30], as shown in Fig. 20. The type of each cell is also shown in the figure. The difference from [30] is that the sampling capacitor is changed to a thick-oxide decoupling cell for less leakage. By keeping V_{ss} port floating, the leakage is further suppressed, and the voltage-dependent capacitance variation is mitigated as well. To implement the floating V_{ss} as well as the routing of G_4–G_9, we defined several power/ground domains during P&R, following the method in [30]. In an upper-level P&R, the dedicated V_{ss} domain for the sampling capacitor is kept floating, while the power/ground domains of G_4–G_9 are automatically routed by a P&R tool.

The simulated capacitance variations (with the input voltage) of the sampling capacitor are shown in Fig. 21(a). Without V_{ss} floating, the capacitance varies by ±23.5%; with V_{ss} floating, the variation is suppressed to ±5.2%. Fig. 21(b) shows the simulated THD of the SAR ADC with S/H circuit in LPE and other building blocks in Verilog-A/HDL. The result

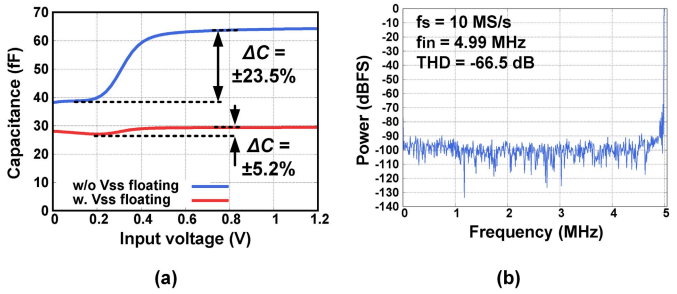
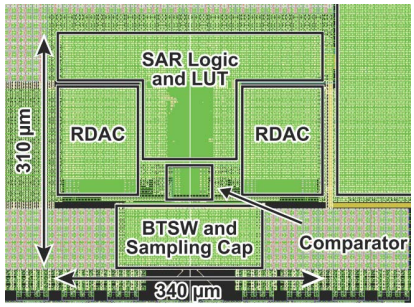


Fig. 21. (a) Simulated voltage-dependent capacitance variation of the sampling capacitor. (b) Simulated THD of the SAR ADC with S/H circuit in LPE and other building blocks in Verilog-A/HDL.



	Power (mW)	
	6-bit	8-bit
Comparator	0.16	0.16
BTSW	0.01	0.01
RDAC	0.45	1.76
Logic	0.31	0.6
Total	0.93	2.53

Fig. 22. Layout of Prototype II in 6-bit and 8-bit topologies and power breakdowns. They have same area because of unchanged floor plan.

of −66.5 dB suggests the capability of sustaining 10.75-bit ENOB thanks to these techniques.

Although one may suspect that sampling capacitor G_{10} with floating source and drain can be more sensitive to substrate noise coupling, yet simulated output spectra of the sampling circuit suggest almost no difference between the cases of floating and connected V_{ss}, when adding a 100-mV_{pp} Gaussian random noise to the substrate of G_{10}. Nevertheless, to alleviate the substrate noise coupling when incorporating the ADC to an SoC, a guard ring is often preferred (though with some manual layout work).

D. Discussion of Speed and Resolution

The speed of the proposed SAR ADC is mainly limited by the settling time of RDAC and the latency of LUT. LPE simulations of current designs suggest about 0.5- and 1-ns settling times of the 6- and 8-bit RDACs, respectively. Since the results are mainly limited by parasitic capacitance during P&R, they can be reduced with larger gate size and optimized wiring. Also, similar to a conventional custom SAR ADC, settling time is degraded by wire bonding, which requires sufficient decoupling capacitors. The LUT latencies of current designs are about 1 ns of both versions. Giving about 0.5 ps for sampling and about 0.7 ps for the comparator and the logic, the estimated highest conversion speeds of 6- and 8-bit SAR ADCs can be 45 and 73 MS/s, respectively. Nevertheless, since we mainly focus on the linearity improvement in Prototype II, we still designed the two ADCs with 10-MS/s sampling frequency.

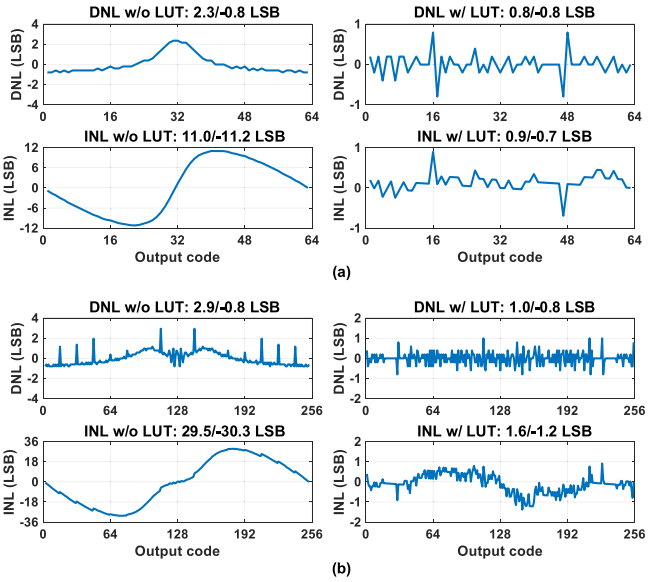


Fig. 23. Simulated DNLs and INLs of (a) 6-bit and (b) 8-bit Prototype II ADCs in LPE with and without LUTs.

As for resolution, the one higher than 8-bit may be less practical because resolution is limited by the nonidealities of the RDAC, and the size of LUT increases exponentially resulting in more power consumption and area.

VI. Post-Layout Simulation Results of Prototype II

The improved SAR ADC as Prototype II is designed and implemented in 65-nm bulk CMOS. The layout covering 0.1-mm^2 area and the simulated power breakdowns in LPE are shown in Fig. 22. Each building block is automatically P&R, and RDACs are placed symmetrically in the macro level. Although we laid out the macro manually, it is possible to place and route it automatically using the P&R tool because the positions of building blocks and their pins are specifically known. Also, for simplicity, the floor plans for building blocks of both 6- and 8-bit versions are the same; thus, two ADCs occupy the same area. The floor plans can be, of course, optimized if the area is a concern. Verified by LPE simulations at 10-MS/s, with 1.2-V power supply, the power consumptions of the 6- and 8-bit SAR ADCs are 0.9 and 2.5 mW, respectively, thanks to the improved RDAC enabling control.

Fig. 23 shows the simulated DNLs and INLs of the two ADCs in LPE without and with their default LUTs. Without LUTs, the peak DNL and INL of the 6-bit version are 2.3/−0.8 LSB and 11.0/−11.2 LSB, respectively. Those of the 8-bit version are 2.9/−0.8 LSB and 29.5/−30.3 LSB, respectively. Thanks to the LUT-based compensation, the linearity is significantly improved. With LUT, the peak DNL and INL of the 6-bit version are 0.8/−0.8 LSB and 0.9/−0.7 LSB, respectively. Those of the 8-bit version are 1.0/−0.8 LSB and 1.6/−1.2 LSB, respectively.

Fig. 24 shows simulated spectra of the two ADCs with Nyquist and half-Nyquist input frequencies. Transient noise is turned on for the simulations. The number of FFT points

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART SYNTHESIZABLE ADCS

	Prototype I	[1]Prototype II		Access'19 [21]	Access'20 [22]	TCAS-I'14 [16]	TCAS-II'15 [25]	CICC'19 [19]	[3]TCAS-I'14 [27]
		6-bit	8-bit						
Type	SAR	SAR		SAR	SAR	Stochastic	Stochastic	VCO-based	VCO-based
Custom cells involved?	No	No	No	No	Poly res. & MOM cap.	No	No	Poly resister	No
CMOS (nm)	65	65		28	40	90	130	40	65
Active area (mm^2)	0.0053	[2]0.1		0.002	0.005	0.18	0.51	0.01	0.026
Input range (mV_{pp})	600 (differential)	2200 (differential)		800 (single)	1000 (single)	280 (differential)	800 (differential)	NA	600 (single)
F_s (MHz)	10	10		0.5	0.0028	21	140	600	205
BW (MHz)	5	5		0.25	0.0014	10.5	70	4	25.6
SNDR (dB)	28.1	35.7	47.2	34.2	40.4	34.6	28.5	68.8	50.3
SFDR (dB)	32.5	45.7	62.1	44	49.7	41.5	37.0	75	55.3
ENOB (bit)	4.4	5.6	7.5	5.4	6.4	5.5	4.4	11.1	8.1
Power (mW)	14.3	0.9	2.5	0.092	0.0073	1.1	2.3	1.1	3.3
[4]FoM (pJ/step)	67.73	1.86	1.38	4.36	30.87	1.16	0.78	0.06	0.23

[1]Verified with LPE simulation.
[2]Same floor plan for the 6-bit and 8-bit versions.
[3]Not automatically laid out.
[4]FoM = Power / (2ENOB×2×BW).

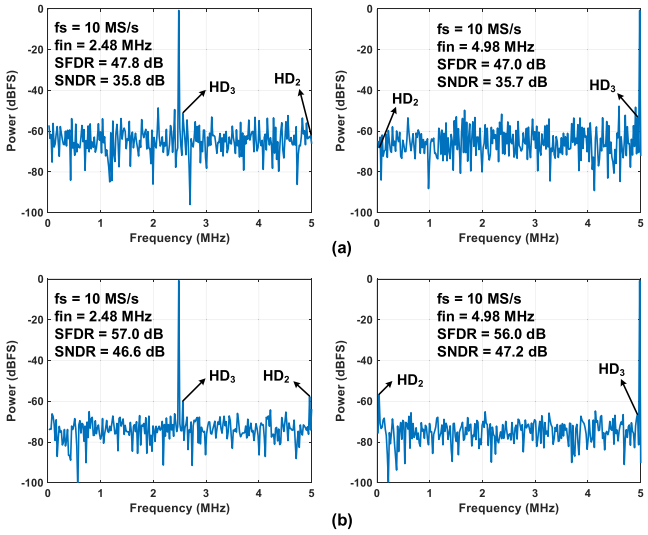


Fig. 24. Simulated spectra of (a) 6-bit and (b) 8-bit Prototype II in LPE with transient noise turned on.

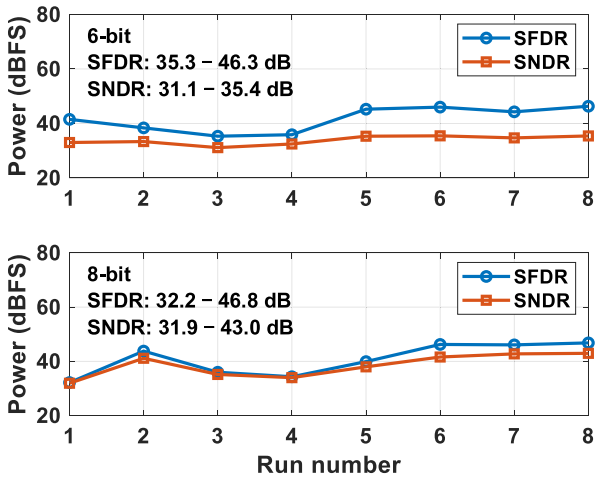


Fig. 25. Monte Carlo simulated SFDRs and SNDRs of 6-bit and 8-bit Prototype II in LPE.

is 512. With Nyquist input frequency, the SNDRs are 35.7 and 47.2 dB, respectively, translating to 5.6- and 7.5-bit ENOBs, and 1.86- and 1.38-pJ/step FoMs, respectively. Fig. 25 shows Monte Carlo simulated SFDRs and SNDRs. Although the SNDR of the 8-bit ADC can degrade to the same level of the 6-bit one, as previously mentioned, the issue is possible to be overcome with a reconfigurable memory-based LUT.

The performance of Prototype-I and Prototype-II is compared with the state-of-the-art synthesizable ADCs in Table I. Compared with Prototype I, Prototype II is expected to have better performance in terms of input range, SNDR, and power consumption. Compared with the SAR ADCs of [21], [22], this work features higher signal bandwidth, better SNDR, and better FoM (expected from LPE simulation). The SNDR and FoM are also comparable with [16], [25] though the latter two works feature higher sampling rates. The sampling rate and the signal bandwidth of this work can be further increased by improving the internal clocking and logic latency. Although the FoMs are less comparable with [19], [27], this work is implemented using only standard cells and laid out automatically. Furthermore, the proposed SAR ADC can generally handle a larger amplitude of the input signal among the other works.

VII. CONCLUSION

We have presented a fully synthesizable all-standard-cell-based SAR ADC using an inverter-based RDAC, a four-input comparator, and a floating-diffusion S/H circuit. Prototype I in 6-bit architecture is measured on silicon. The performance is improved in Prototype II with proposed techniques enhancing linearity and lowering power consumption. The performance of Prototype II is verified through LPE simulations in 6- and 8-bit versions. The ADCs are described in RTL and laid out using a commercial digital automatic P&R tool. The circuits and the methodology enable fast implementation still with moderate resolution. This merit is highly demanded in the scenario of incorporating this ADC into a digital signal processing system.

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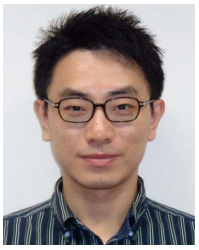

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