Opening of the 2021 Editorial Year—Overture for a New Year of Change

THE year 2021 is expected to be a turning point, after a challenging year that has unexpectedly impacted our lives and interactions. In 2020, technological and scientific progress in the area of VLSI design has been relentless despite the difficulties that the year has brought. This has been made possible by the ability to adapt to the temporary "new normal" of our community of researchers, designers, and innovators in the area of VLSI systems.

The year starts with a renewed enthusiasm on the wave of a remarkable growth of our IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI), both in quantity and quality [item 1) in the Appendix]. From a quantity viewpoint, the energetic sentiment of our community has reflected very positively on submissions, which have fully recovered compared to the previous year. From a quality standpoint, the acceptance rate has been progressively reduced, with a decisive 5.1% decrease in the year 2020 that has brought it to a healthy 31.1%. The expansion of the Editorial Board and the streamlined review process have led to a reduction in the turnaround time to first decision down to about seven weeks. The impact factor has exceeded the value of two for the first time. Keynote papers have now become a tradition in our journal, with contributions from Giovanni De Micheli (EPFL), Jan Rabaey (University of California at Berkeley), Vivek De (Intel), and Kaushik Roy (Purdue University), among the many others. The keynote papers are indeed becoming a venue to challenge common thinking and stimulate further discussion on the upcoming opportunities to innovate and change the world.

We are very excited to open this first TVLSI issue of the year 2021 with the keynote paper by Prof. Boris Murmann (Stanford University), which provides a compelling vision on mixed-signal computing for inference in deep neural networks (DNNs). Memory-like and in-memory compute fabrics are discussed to narrow the gap between recently achieved energy efficiency targets and asymptotic limits. Energy efficiency improvements enabled by analog computing are explored in the low-SNR regime, leveraging on the error resilience of DNNs. Energy per operation down to the fJ/op range is shown at the processing array level. Design challenges and opportunities are also discussed for the analog–digital interface and complete DNN accelerators. The keynote paper describes an intriguing vision on domain-specific hardware for on-chip integration of DNNs. Our community is called to act and solve the fundamental challenges related to data movement, layer reconfigurability, and integration with emerging memory technologies for on-chip weight storage. Overall, across-layer insights and innovation from algorithm to circuit are shown to be instrumental for the pursuit of further advances in this exciting field. We trust this article will trigger deeper reflections and collaborations across our community, and encourage the adoption of more comprehensive approaches to accelerate technology advancements in this field.

Being the beginning of the year, it is natural to wonder about "what's next" and lay out a clear path that continues the upward trajectory that our journal is having. Several initiatives will be rolled out this year, continuing the implementation of the long-term plan that was described in a previous editorial [item 1) in the Appendix]. Social media will be used as an additional channel to enable two-way and tighter interaction between the TVLSI editorial board and its readership. We trust that this will establish new bridges among the three IEEE Societies that sponsor it, and the related communities (Circuits and Systems, Computers, and Solid-State Circuits). Opportunities for across-journal special issues will also be explored to encourage collaboration and synergy of multiple communities on common scope and goals. Such expertise integration effort is indeed crucial to the advancement of our field and of our society at large.

The content of TVLSI publications will be enriched through the broader inclusion of supplemental materials extending the traditional paper format beyond its solely textual and graphical form. Graphical abstracts, software code (e.g., RTL and testbenches), benchmarks, data sets, design scripts, and demo multimedia files are expected to make TVLSI publications more interesting, informative, verifiable, and replicable. We believe that such added value will nicely complement the ongoing initiatives to relentlessly raise the quality and the impact of our journal. Other initiatives are also being prepared to sustain the growth of TVLSI in terms of its impact. Please stay tuned to discover more in the months to come!

This exciting journey is ultimately enabled by the passion and the effort of many dedicated people. First of all, we really appreciate and value the continued support from the TVLSI Steering Committee. At the center stage of the journal operations, the members of the Editorial Board have really brought the above vision to life, generating tangible improvements and impact while keeping authors and readers well connected. I deeply thank each and every one of them. Furthermore, I am very excited to announce the top five Associate Editors who have exceptionally contributed to the speedup of the turnaround time of the submission process in 2020: Prof. Mingoo Seok (Columbia University), Prof. Chirn Chye Boon (NTU), Dr. Rajiv Joshi (IBM), Prof. Yong Chen (UMacau), and Prof. Paolo Crovetti (PoliTO). Their exceptionally high

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standards are a testimony to the commitment of the entire Editorial Board to serve the members of our society and make a difference.

Last and certainly not least, the Associate Editors-in-Chief Prof. Mircea Stan and Prof. Pasquale Corsonello as well as the Editorial Assistant Stacey Weber are irreplaceable and generous travel companions. Their leadership and tireless support are essential to make TVLSI what it is, and have been even more so while navigating through this challenging year.

Thank you all for your effort and contribution, they really make a difference. Now, let us go back to work. Another remarkable year is getting started!

Massimo Alioto, Editor-in-Chief
Department of Electrical and Computer Engineering, National University of Singapore
Singapore 117583

APPENDIX
RELATED WORK

1) M. Alioto, "Editorial TVLSI positioning–continuing and accelerating an upward trajectory," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 2, pp. 253–280, Feb. 2019.

Massimo Alioto (Fellow, IEEE) is a Professor with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore, where he leads the Green IC Group, and is the Director of the Integrated Circuits and Embedded Systems Area, and the FD-FAbrICS Research Center. Previously, he held positions at the University of Siena, Siena, Italy; Intel Labs, Hillsboro, OR, USA; University of Michigan, Ann Arbor, MI, USA; University of California at Berkeley, Berkeley, CA, USA; and École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland.

He has authored or coauthored more than 300 publications in journals and conference proceedings. He is a coauthor of four books printed by Springer, including *Enabling the Internet of Things—From Circuits to Systems* (Springer, 2017), and the recent *Adaptive Digital Circuits for Power-Performance Range Beyond Wide Voltage Scaling*. His primary research interests include self-powered wireless integrated systems, near-threshold circuits for green computing, widely energy-scalable integrated systems, data-driven integrated systems, hardware-level security, and emerging technologies.

Prof. Alioto is the Editor-in-Chief of IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and was the Deputy Editor-in-Chief of IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS. He is a Distinguished Lecturer of the IEEE Solid-State Circuits Society and previously had the same appointment in the IEEE Circuits and Systems Society, for which he is/was also a member of the Board of Governors. In the last five years, he has given 50+ invited talks at top conferences, universities, and leading semiconductor companies. He served as a Guest Editor for several IEEE journal special issues [e.g., IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS (TCAS-I), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS (TCAS-II), and IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS (JETCAS)] and an Associate Editor for a number of IEEE and ACM journals. He is/was Technical Program Chair (e.g., ISCAS 2023, SOCC, ICECS, and NEWCAS) in numerous conferences and is currently in the IEEE "Digital Architectures and Systems" ISSCC subcommittee, and the IEEE ASSCC technical program committee.