

# Analysis of Passive Charge Sharing-Based Segmented SAR ADCs

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**Abstract**—This article presents the theoretical analysis of passive charge sharing-based segmented successive-approximation-register (SAR) analog-to-digital converter (ADC), where the precise reference source in a capacitive digital-to-analog converter (CDAC) is replaced by a capacitor that is  $\beta$  times larger than its bit capacitor and precharged to the reference level, known as a reference charge reservoir (RCR). A segmented SAR-ADC uses a coarse SAR-ADC to compute some most significant bits (MSBs). Four methods, namely aligned switching (AS) with bitwise RCRs, AS with a subsample-wise RCR, detect-and-skip aligned switching (DAS-AS) with bitwise RCRs, and DAS-AS with a subsample-wise RCR are introduced for setting fine MSBs. Closed-form analytic expressions of the reference error due to the finite reference capacitance are derived and validated by behavioral modeling and circuit simulation of an 11-bit 50 MS/s segmented SAR ADC in 65-nm CMOS technology. The error expressions can be used to select one of the four methods for setting the fine MSBs and to determine  $\beta$  for the required linearity or for implementing digital circuitry for precise error correction.

**Index Terms**—Bitwise reference charge reservoirs (RCRs), reference-buffer free, segmented architecture, subsample-wise reference charge reservoir (RCR), successive-approximation-register (SAR) ADC.

## I. INTRODUCTION

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) are the most energy-efficient data conversion solutions for 10–100-MHz sampling rates with 10–12 bit resolution [1]–[4]. Combined with pipeline [5], [6], time interleaving [6], and noise shaping [7], SAR ADCs are being extended to applications with even higher speed up to GHz [8] or higher resolution up to 18 bits [9].

One major reason why the SAR-ADC architecture is increasingly popular is its scalability with the process technology and its amenability to a digital-centric design methodology. To remove power-hungry buffers associated with precise capacitive digital-to-analog converter (CDAC) references, various forms of passive charge sharing have been

introduced [10]–[16]. In particular, a Sample-wise Switched Reference Charge Reservoir (SS-RCR) technique was introduced [12], where a sufficiently large capacitor (reservoir),  $\beta$  times larger than the total bit capacitors, precharged to the reference voltage level during the sample phase acts as the reference for all bit switchings during the entire ADC. Very recently, a Bitwise Switched Reference Charge Reservoir (BS-RCR) technique was proposed [13], where the charge reservoir capacitor is split into the corresponding bit, and before each bit switching, the corresponding bit charge reservoir capacitor is precharged to the reference levels and used as the reference during each bit decision. With BS-RCRs, a 16-bit 1 MS/s SAR-ADC in 55 nm CMOS with 6.95 mW with a FoM of 738 fJ/conversion-step [14] and a 16-bit 16 MS/s SAR in 55 nm CMOS with FoM 157.4 fJ/conversion-step [15] have been demonstrated. It has been approved theoretically [16] that the BS-RCR technique yields better linearity than the SS-RCR technique, a seemingly counterintuitive fact. Furthermore, the reference error due to finite BS-RCRs appears in the form of digitally correctable *bit weight error*, where the  $i$ th bit weight is attenuated by  $1 + 2^{i+1-N}\beta$  for an  $N$ -bit SAR-ADC.

To reduce the energy associated with most significant bit (MSB) switching, a dominating factor in affecting SAR-ADC switching energy efficiency, a segmented architecture has been developed, where a coarse SAR-ADC computes the MSBs for a fine SAR-ADC [17]. This article extends reference charge reservoirs (RCRs) to segmented SAR-ADC design. Since BS-RCR has better linearity, we use it for the coarse ADC, as well as fine ADC LSB switching. For copying the results from coarse ADC to the MSBs of the fine ADC, there are two switching methods: aligned switching (AS), all bits are switched together; detect-and-skip AS (DAS-AS) [17], where only some bits are switched. For the fine MSBs reference, it can be bitwise RCRs and subsample-wise RCR. This leads to four switching methods for setting fine MSBs, known as AS with bitwise RCRs, AS with a subsample-wise RCR, DAS-AS with bitwise RCRs, and DAS-AS with a subsample-wise RCR.

Theoretically, we have derived the analytical formula of the reference error for various RCR-based segmented SAR-ADC switching schemes. From these formulae, we have proved that successive decisions using bitwise RCRs and fine MSB switching using DAS-AS subsample-wise RCR yields the near the smallest reference error while saving most switching energy.

This article is organized as follows. Section II describes the operations of charge-redistribution and charge-sharing SAR

Manuscript received November 21, 2019; revised February 6, 2020; accepted February 27, 2020. Date of publication April 1, 2020; date of current version April 24, 2020. This work was supported in part by the Air Force Research Laboratory (AFRL) and in part by Defense Advanced Research Projects Agency (DARPA) Posh Open Source Hardware (POSH) Program under Grant FA8650-18-2-7857. (Corresponding author: Aili Wang.)

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Digital Object Identifier 10.1109/TVLSI.2020.2979500

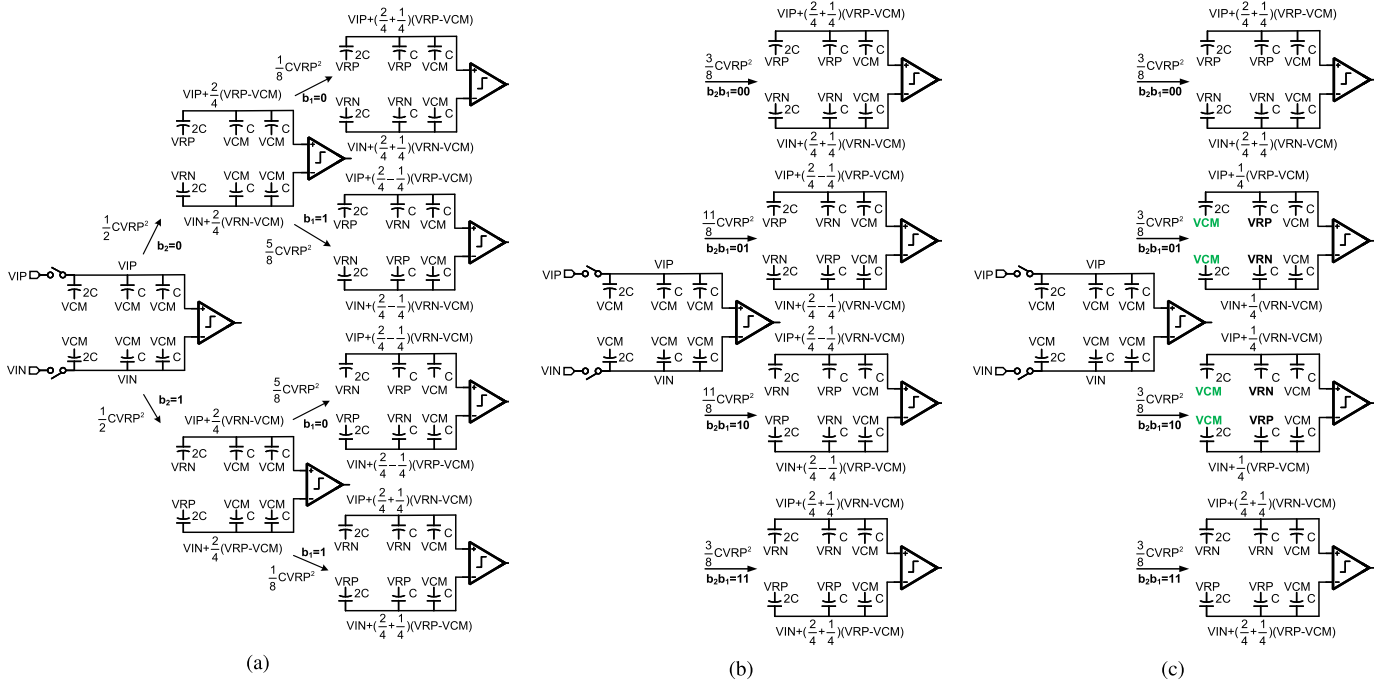


Fig. 1. Three bit charge redistribution CDAC switching examples. (a) MCS. (b) AS. (c) DAS-AS.

ADCs. Section III presents the theoretical analysis of the RCR-based segmented SAR-ADCs. Simulation validation and discussion are described in Section IV. Section V concludes this article.

## II. CHARGE REDISTRIBUTION AND CHARGE SHARING-BASED SAR ADCS

In this section, a 3-bit SAR ADC is used to illustrate three switching methods: VCM-based merged capacitor switching (MCS), AS, and DAS-AS, and their switching energy consumption. First, reference sources are used for CDAC; this is the *charge-redistribution* SAR ADC. We then replace reference sources with precharged capacitors, known as RCRs; this leads to the *passive charge-sharing* SAR ADC.

### A. Charge-Redistribution SAR-ADC Switchings

Fig. 1(a) illustrates the operation of a 3-bit binary-weighted differential charge-redistribution SAR ADC using MCS [18]. Two reference levels are VRP (high, often VDD) and VRN (low, often GND) with the common mode voltage  $V_{CM} = (VRP + VRN)/2$ . Bit capacitors are binary weighted with  $2C$ ,  $C$ , and  $C$  where  $C$  is the unit capacitance. Initially, differential inputs VIP and VIN are sampled onto the top plates of the CDAC, and all bottom plates are connected to VCM. Then, the comparator compares the two top-plate voltages and determines the MSB  $b_2$ . The bottom plate of the p-side CDAC MSB bit capacitor is switched to VRN if  $b_2 = 1$  otherwise to VRP, whereas the bottom plate of the N-side MSB bit capacitor switches oppositely to VRP and VRN. The resulting top plate voltages are shown in the figure. This process continues by comparing the two resulting top-plate voltages to obtain the second MSB and switches the

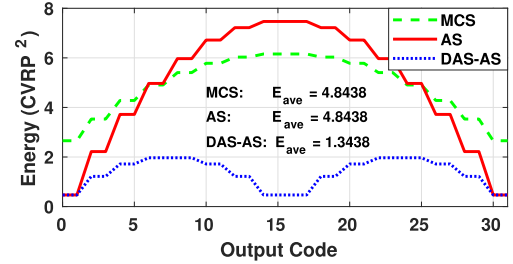


Fig. 2. Calculated switching energy of a 5-bit SAR ADC using MCS, AS, and DAS-AS.

bottom plates to VRP or VRN accordingly. The LSB is finally obtained by comparing the resulting top-plate voltages.

Hence, a total of four cases of MCS are shown in Fig. 1(a), where for each switching, the resulting top-plate voltage and the energy consumed are marked. Now consider that all digital bits are known, and all the bottom plates of the 3-bit CDAC are switched simultaneously in one step. This is referred to as AS [17]. The four cases are illustrated in Fig. 1(b). If we are interested only in the final top-plate voltages with AS, opposite switching can be avoided. This was developed like the DAS-AS operation [17]. Fig. 1(c) shows all DAS-AS four cases.

We observe that all the three switching methods yield the same top-plate voltage but different energy consumption values. The average energy consumed by AS is the same as that of MCS. DAS-AS consumes the least energy. Fig. 2 shows the switching energy for each code of a 5-bit SAR ADC uses these three different switching methods.

### B. Charge-Sharing SAR ADC Switchings

Fig. 3(a)–(c) shows, respectively, the decision process of a 3-bit charge-sharing SAR ADC using MCS, AS, and

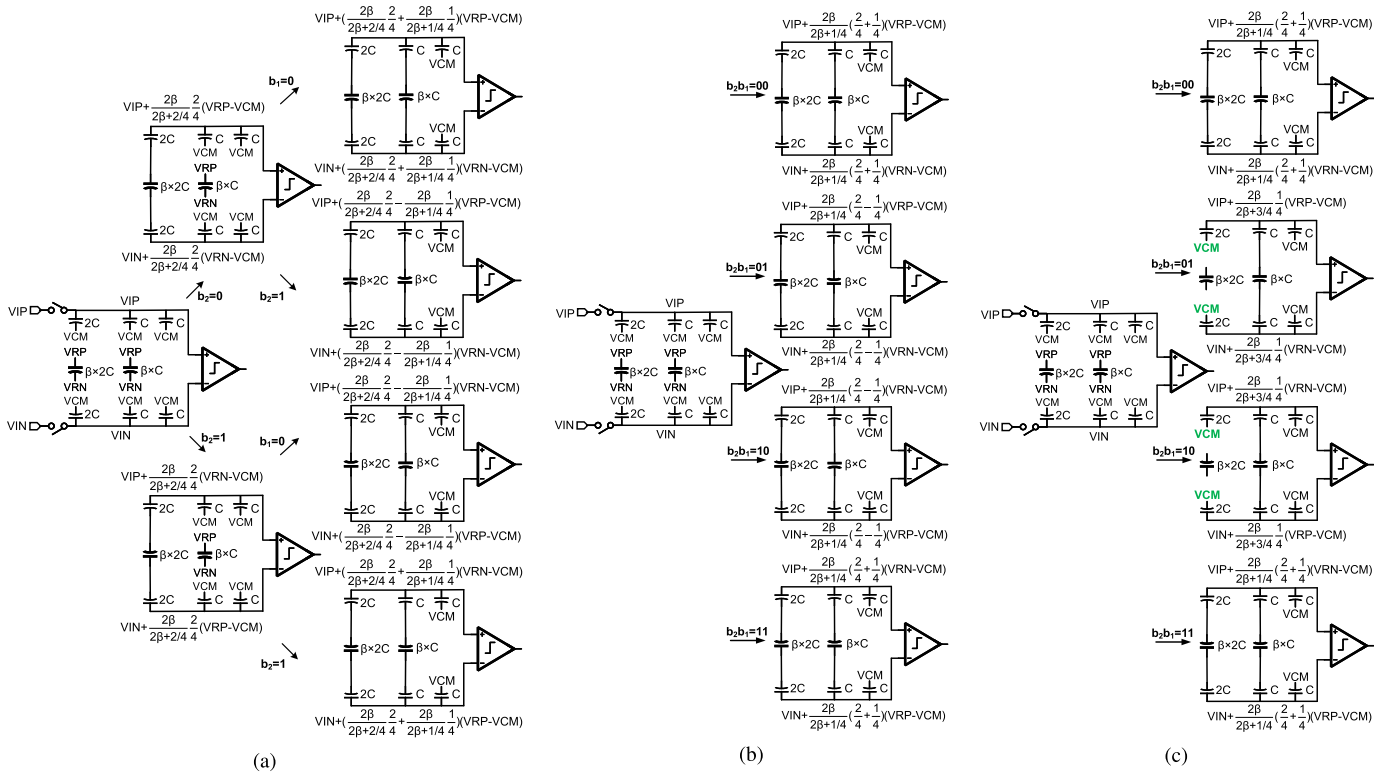


Fig. 3. Three-bit bitwise charge-sharing CDAC switching examples. (a) MCS. (b) AS. (c) DAS-AS.

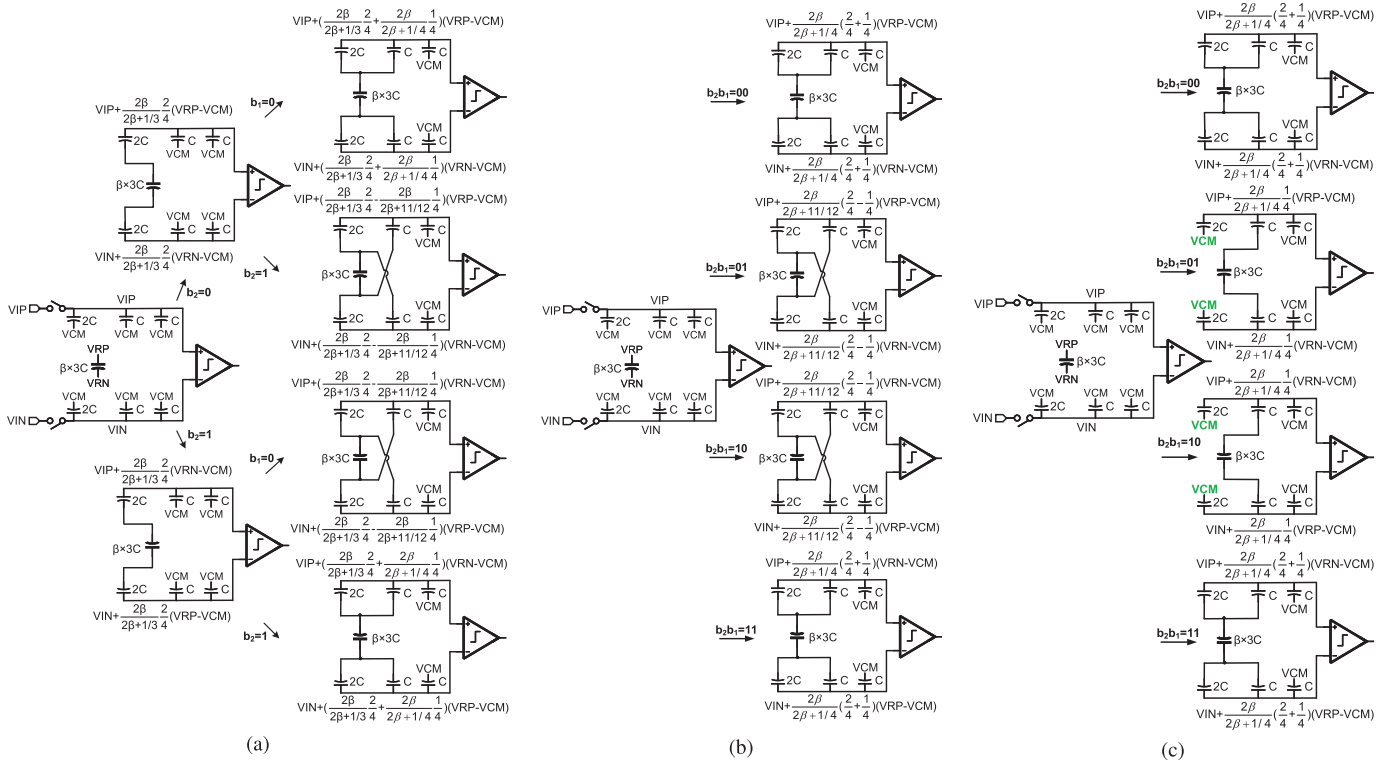


Fig. 4. Three-bit sample-wise charge-sharing CDAC switching examples. (a) MCS. (b) AS. (c) DAS-AS.

DAS-AS methods. For each bit decision, the reference sources VRP and VRN are replaced by charge reservoir capacitors  $\beta$ -times larger than the corresponding bit capacitances, precharged to VRP and VRN. This is known as *bitwise*

RCR. Fig. 4 shows the decision process of another structure of a 3-bit charge-sharing SAR-ADC where all reference capacitors connected in parallel to form a *sample-wise* charge reservoir.

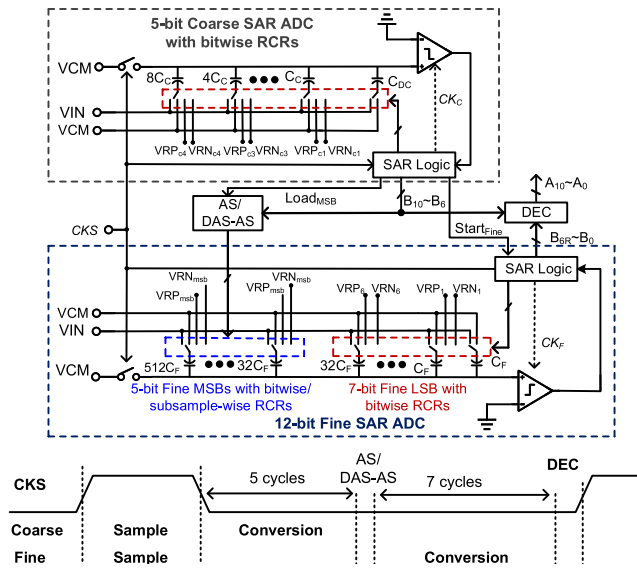


Fig. 5. Prototype segmented SAR-ADC architecture.

For all the three methods, for each bit switching, the resultant top plate voltages are labeled in the figures. We can see that there is a  $\beta$ -dependent term, referred to as  $\alpha$ ,  $0 < \alpha < 1$ , reflecting the reference error due to finite  $\beta$ . When  $\beta = \infty$  and  $\alpha = 1$ . We observe that with bit-wise RCRs, for term  $\alpha$  in AS is not less than that in MCS, which is not less than that in DAS-AS. Thus, for bit-wise RCR, AS has better linearity than MCS, and MCS has better linearity than DAS-AS. With sample-wise RCR, the term  $\alpha$  in AS is not greater than that in MCS, which is not greater than that in DAS-AS. Hence, for sample-wise RCR, DAS-AS has better linearity than MCS, and MCS has better linearity than AS.

### III. ANALYSIS OF SEGMENTED SAR SWITCHING WITH RCRs

This section presents the theoretical analysis of the SAR-ADC linearity for various switching methods for a segmented charge-sharing ( $N + M$ )-bit SAR ADC where a coarse SAR-ADC computes the  $N$  MSBs, and a fine SAR ADC computes the  $M$  LSBs. Whenever possible, the analysis is based on the equivalent circuit model introduced in [16] since it provides more circuit intuition. Nevertheless, all the results in this section have been derived directly using the principle of charge conservation following the same procedure as in the Appendices of [16].

#### A. Segmented SAR-ADC Architecture

Fig. 5 shows the architecture of the proposed RCR-based segmented SAR ADC. For simplicity, it shows only the single-ended architecture, but the implementation is differential. It consists of a 5-bit coarse SAR ADC, a 12-bit fine SAR ADC including one redundant bit, an AS or DAS-AS logic block for setting fine MSBs, and a digital error correction (DEC) block. The coarse or fine SAR ADC contains a bootstrapped sampling switch, an RCR-based CDAC, a voltage comparator [17], and an SAR logic block.

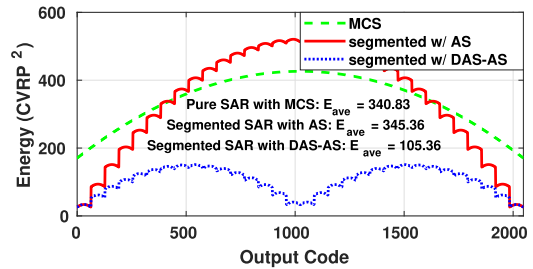


Fig. 6. Calculated switching energy of an 11-bit SAR ADC with MCS, a segmented SAR ADC shown in Fig. 5 with AS and with DAS-AS.

Differential inputs VIP and VIN are sampled on the CDAC bottom plates in both coarse and fine ADCs, whereas the top plates are connected to VCM during the sampling phase. Simultaneously, the bit reservoir capacitor sample references VRP and VRN. After sampling, the 5-bit coarse SAR ADC computes the 5 MSBs bit by bit using VCM-based MCS [18]. For RCR-based CDAC switching, the reservoir capacitor precharged to voltage level VRP or VRN is used instead of the reference source VRP or VRN. Then, the AS or DAS-AS logic block loads digits from the coarse ADC to the 5-bit fine MSBs in one step. Since the fine 5 MSBs are set at one step, one of the four switching methods: AS with bit-wise RCRs, AS with a subsample-wise RCR, DAS-AS with bit-wise RCRs, and DAS-AS with a subsample-wise RCR can be used. Finally, the remaining seven fine LSBs are determined successively using MCS with bit-wise RCRs. The five MSBs from the coarse ADC and the seven LSBs from the fine ADC are combined into the DEC block to derive the final 11-bit output.

Fig. 6 compares the switching energy of each code of a 11-bit charge-redistribution segmented SAR-ADC and that of a conventional 11-bit charge-redistribution SAR-ADC. The conventional 11-bit SAR-ADC uses MCS. The segmented ADC uses MCS for the coarse ADC, uses AS or DAS-AS to copy the MSBs for the fine ADC, and MCS for resolving the remaining LSBs. We can see that the segmented SAR-ADC with DAS-AS reduces switching energy by 69.1% compared with a conventional SAR with MCS. Here, the coarse unit capacitance is twice the fine unit capacitance in the segmented architecture.

#### B. Bit-wise RCR-Based Coarse SAR ADC Successive Switching

The  $N$ -bit coarse SAR ADC decides each bit successively using VCM-based MCS [18] with bit-wise RCRs. We use a bracketed superscript  $(k)$  to indicate the  $k$ th bit decision, and a subscript  $i$  to represent the  $i$ th bit. The equivalent half-circuit model [16] for charge-sharing from  $(k+1)$ th to  $k$ th bit decision is shown in Fig. 7. The bottom plate of the  $k$ th bit weight capacitor  $C_k$  is switched from connecting to VCM to either VRP or VRN dependent upon  $b_k$ . Without loss of generality, we assume VRP. Voltage  $VRP_k^{(k)}$  can be obtained from the following charge-sharing equation:

$$\begin{aligned} & (VRP - VCM)(2\beta C_k) \\ &= \left( VRP_k^{(k)} - VCM \right) \times [2\beta C_k + (C_a + C_b)C_k / (C_a + C_b + C_k)]. \end{aligned} \quad (1)$$



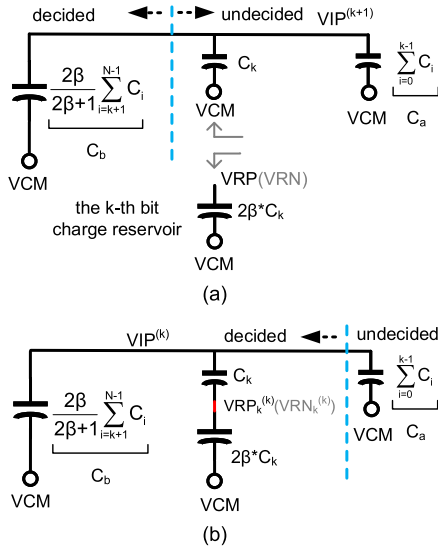


Fig. 7. Half-circuit model and derivation of bitwise reference switching in the coarse SAR ADC. (a)  $(k+1)$ th decision. (b)  $(k)$ th decision.

Then the p-side top-plate voltage change due to this charge sharing is obtained by capacitive division as

$$VIP^{(k)} - VIP^{(k+1)} = \frac{C_k(1-2b_k)}{C_a + C_b + C_k} (VRP_k^{(k)} - VCM). \quad (2)$$

Substituting (1) to (2) with  $C_T = C_a + C_b(2\beta+1)/2\beta + C_k$ , we obtain the following:

$$VIP^{(k)} - VIP^{(k+1)} = \alpha^{(k)} \frac{(1-2b_k)C_k}{C_T} (VRP - VCM) \quad (3)$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + \sum_{j=0}^{k-1} \frac{C_j}{C_T}} = \frac{2\beta}{2\beta + (1/2)^{N-k}} \quad (4)$$

where  $N$  is the number of bits in the coarse ADC,  $C_T$  is the sum of the coarse CDAC capacitance from  $C_0$  to  $C_{N-1}$ , and  $b_k$  is the  $k$ th bit value being either 1 or 0. The last equality in (4) holds if bit capacitances are binary weighted.

Note that  $0 < \alpha^{(k)} < 1$ ,  $\alpha^{(k)}$  increases from the MSB ( $k = N-1$ ) to the LSB ( $k = 1$ ) and  $\alpha^{(k)} = 1$  when  $\beta = \infty$ . Fig. 8 shows  $\alpha^{(k)}$  at each bit decision of a 5-bit BS-RCR-based coarse SAR ADC with  $\beta = 16$ . The term  $\alpha^{(k)} \neq 1$  in (3) is caused by the reference error due to charge-sharing between the reference capacitor and the bit capacitor. The elegance of bitwise RCR-based SAR ADCs is that the reference error is the form of linear bit weight error as shown in (4) and in Fig. 8 [16]. Bit weight error factor  $(1 - \alpha^{(k)})$  depends only on  $\beta$ ,  $k$  and  $N$ , irrespective of the input.

### C. Fine MSB AS and DAS AS: Bitwise and Subsample Wise

Let  $C_F$  denote the fine ADC unit capacitance,  $C_{TM}$  the  $N$ -bit MSB capacitance,  $C_{TL}$  the  $M$ -bit LSB capacitance, and  $C_{TF}$  the total capacitance in the fine ADC.

1) *Fine MSB AS: Bitwise and Subsample Wise:* When loading the coarse digits directly to the fine MSBs in one step, the fine CDAC top-plate voltages after AS can be expressed

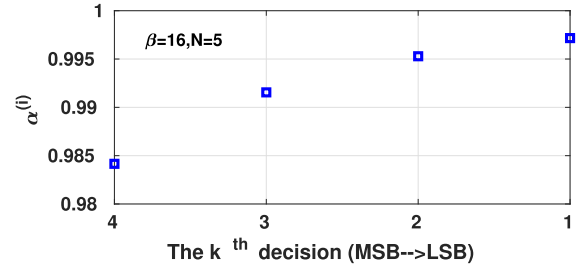


Fig. 8.  $\alpha^{(k)}$  at each bit decision for the coarse SAR ADC in a segmented architecture.

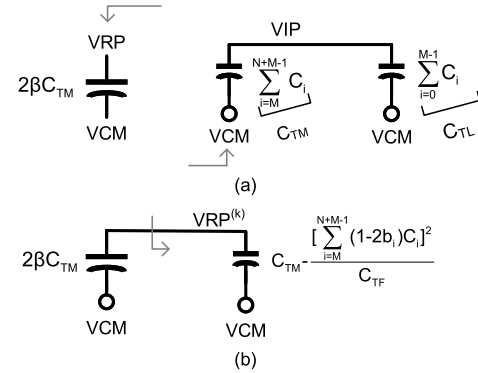


Fig. 9. Half-circuit model and derivation of sample-wise reference switching in fine MSB. (a) Sampling phase. (b) AS decision phase.

in the following equation:

$$VIP^{(M)} = VIP + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i}{C_{TF}} (1-2b_i) (VRP - VCM) \quad (5)$$

$$VIN^{(M)} = VIN + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i}{C_{TF}} (1-2b_i) (VRN - VCM) \quad (6)$$

where  $b_i$  are the digits of the  $N$ -bit fine MSBs, which are equal to coarse bits. For AS, the coefficient  $\alpha^{(M)}$  is extracted to the outside of the sum symbol. This is because AS is an one-step operation involving  $N$ -bits.

For bitwise referenced,  $\alpha^{(M)}$  can be expressed as follows:

$$\alpha^{(M)} = \frac{2\beta}{2\beta + 1 - \sum_{i=M}^{N+M-1} \frac{C_i}{C_{TF}}} = \frac{2\beta}{2\beta + 1 - \frac{C_{TM}}{C_{TF}}}. \quad (7)$$

The derivation is in Appendix A based on charge conservation.

For subsample-wise referenced, the equivalent half-circuit model from the sampling phase to the AS phase is shown in Fig. 9 [16]. Charge is conserved before and after AS; that is

$$\begin{aligned} & (VRP - VCM)(2\beta C_{TM}) \\ &= (VRP^{(M)} - VCM) \\ & \times \left[ 2\beta C_{TM} + C_{TM} - \frac{\left[ \sum_{i=M}^{N+M-1} C_i (2b_i - 1) \right]^2}{C_T} \right]. \quad (8) \end{aligned}$$

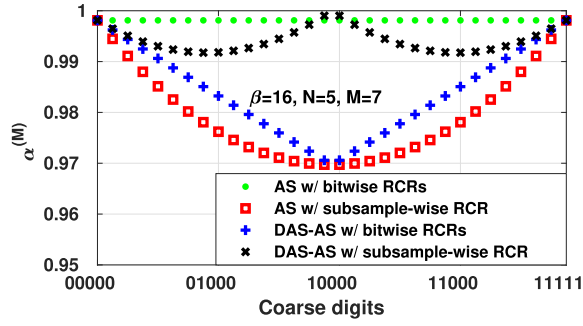


Fig. 10.  $\alpha^{(M)}$  versus coarse codes for the fine MSBs with four different switching methods in a segmented architecture.

Then the p-side top-plate voltage change can be obtained based on capacitive division

$$\text{VIP}^{(M)} = \text{VIP} + (\text{VRP}^{(M)} - \text{VCM}) \sum_{i=M}^{N+M-1} \frac{C_i}{C_{\text{TF}}} (1 - 2b_i). \quad (9)$$

Substituting (8) to (9) with  $C_{\text{TF}} = C_{\text{TM}} + C_{\text{TL}}$ , we obtain the same result as (5) with  $\alpha^{(k)}$  defined by the following equation:

$$\alpha^{(M)} = \frac{2\beta}{2\beta + 1 - \frac{\left[ \sum_{i=M}^{N+M-1} C_i (2b_i - 1) \right]^2}{C_{\text{TF}} C_{\text{TM}}}}. \quad (10)$$

We note that coefficient  $\alpha^{(M)}$  in (7) is input-independent because both bitwise RCRs and AS are input-independent.  $\alpha^{(M)}$  is shown in Fig. 10 by the dot · marker. The last term in the denominator of (7) represents the ratio of the  $N$ -bit fine MSB capacitance to the total fine capacitance. The subsample-wise reference coefficient  $\alpha^{(M)}$  in (10) is input-dependent because of the subsample-wise RCR. In this case,  $\alpha^{(M)}$  has  $2^N$  possible values based on the  $N$ -bit MSBs, which is shown in Fig. 10 by the square □ marker. We further observe that the square term in (10) is less than or equal to  $C_{\text{TM}}$ . Thus,  $\alpha^{(M)}$  in (7)  $\geq$   $\alpha^{(M)}$  in (10). Therefore, AS with bit-wise charge reservoirs always has better linearity than AS with a subsample-wise charge reservoir.

2) *Fine MSB DAS AS: Bitwise and Subsample Wise*: Now, we consider that the fine MSBs use DAS-AS based on the computed coarse MSBs. If the coarse MSB is 1, then the p-side (n-side) CDAC bottom plates either connect to VCM or switch to VRN (VRP). The switched bit capacitance in the fine MSBs is

$$C_{\text{sw}} = \sum_{i=M}^{N+M-1} C_i b_i \quad (11)$$

where  $b_i$  are the digits of the  $N$ -bit fine MSBs, which are obtained by left rotating coarse bits. The differential fine CDAC top-plate voltages after DAS-AS operation are given in the following equation:

$$\text{VIP}^{(M)} = \text{VIP} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i b_i}{C_{\text{TF}}} (\text{VRN} - \text{VCM}) \quad (12)$$

$$\text{VIN}^{(M)} = \text{VIN} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i b_i}{C_{\text{TF}}} (\text{VRP} - \text{VCM}). \quad (13)$$

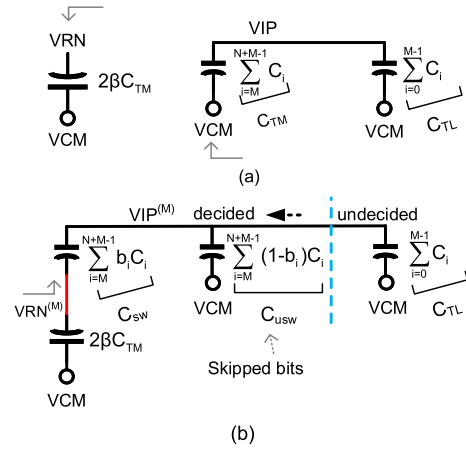


Fig. 11. Half-circuit model and derivation of subsample-wise reference switching when coarse MSB is 1 in fine MSB. (a) Sampling phase. (b) DAS-AS decision phase.

If the coarse MSB is 0, the total switched bit capacitance in the fine MSBs is

$$C_{\text{sw}} = \sum_{i=M}^{N+M-1} C_i (1 - b_i). \quad (14)$$

The CDAC top-plate voltages can be expressed by

$$\text{VIP}^{(M)} = \text{VIP} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i (1 - b_i)}{C_{\text{TF}}} (\text{VRP} - \text{VCM}) \quad (15)$$

$$\text{VIN}^{(M)} = \text{VIN} + \alpha^{(M)} \sum_{i=M}^{N+M-1} \frac{C_i (1 - b_i)}{C_{\text{TF}}} (\text{VRN} - \text{VCM}). \quad (16)$$

For bitwise-referenced DAS-AS,  $\alpha^{(M)}$  is given in (17)

$$\alpha^{(M)} = \frac{2\beta}{2\beta + 1 - \frac{C_{\text{sw}}}{C_{\text{TF}}}} \quad (17)$$

as shown in Appendix B based on the principle of charge sharing.

For subsample-wise referenced DAS-AS, there is no cross-coupling between the p-side and the n-side CDACs, so the equivalent half-circuit model can be used to derive the final results directly. Fig. 11 shows the equivalent half-circuit model from the sampling phase to the DAS-AS phase. The charge is conserved before and after AS; that is

$$\begin{aligned} & (\text{VRN} - \text{VCM})(2\beta C_{\text{TM}}) \\ &= (\text{VRN}^{(M)} - \text{VCM}) \\ & \quad \times [2\beta C_{\text{TM}} + (C_{\text{TL}} + C_{\text{usw}})C_{\text{sw}} / (C_{\text{TL}} + C_{\text{usw}} + C_{\text{sw}})]. \end{aligned} \quad (18)$$

Then the p-side top-plate voltage change can be obtained based on capacitive division

$$\text{VIP}^{(M)} = \text{VIP} + (\text{VRN}^{(M)} - \text{VCM}) \sum_{i=M}^{N+M-1} \frac{C_i b_i}{C_{\text{TF}}}. \quad (19)$$

Substituting (18) to (19) with  $C_{\text{TM}} = C_{\text{sw}} + C_{\text{usw}}$  and  $C_{\text{TF}} = C_{\text{TM}} + C_{\text{TL}}$ , we can obtain the same result as (12) with  $\alpha^{(M)}$  defined by the following equation:

$$\alpha^{(M)} = \frac{2\beta}{2\beta + \frac{C_{\text{sw}}}{C_{\text{TM}}} \left(1 - \frac{C_{\text{sw}}}{C_{\text{TF}}}\right)}. \quad (20)$$

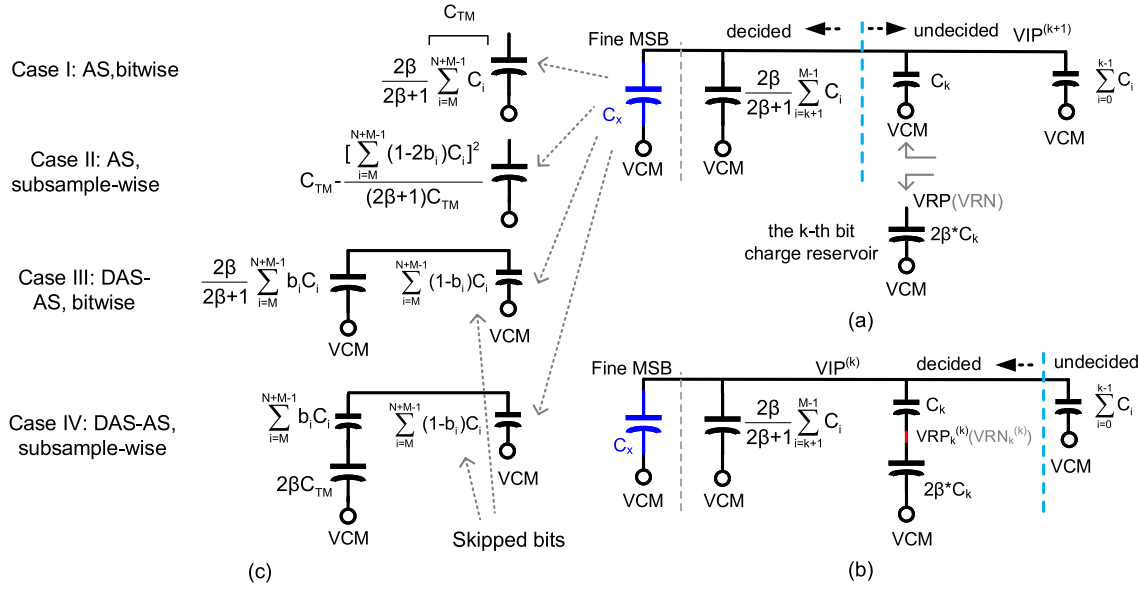


Fig. 12. Half-circuit model and derivation of bitwise reference switching in fine LSBs. (a)  $(k+1)$ th decision. (b)  $(k)$ th decision. (c)  $C_x$  in four different switching methods.

We have  $\alpha^{(M)}$  in (20)  $\geq \alpha^{(M)}$  in (17) by comparing (20) with (17). This is because, in the DAS-AS operation, the ratio of the reservoir capacitance to the switched bit capacitance is  $\beta C_{TM}/C_{sw}$  for subsample-wise RCR, greater than or equal to  $\beta$  for bitwise RCRs. Thus, subsample-wise referenced DAS-AS always has better linearity than bitwise referenced DAS-AS.  $\alpha^{(M)}$  in (17) and (20) versus coarse digits are shown in Fig. 10 with the plus '+' marker and cross 'x' marker.

3) *Comparison of Four MSB Switching Methods*: Now, we compare  $\alpha^{(M)}$  in (7), (10), (17), and (20) by examining the last two terms in the denominator of  $\alpha^{(M)}$ . Consider the DAS-AS method, the total switched capacitance  $C_{sw}$  expressed in (11) and (14) is mathematically equal to the term  $|\sum_{i=M}^{N+M-1} C_i(2b_i - 1)|$  in AS shown in the last term in the denominator of (10). We rewrite (10) as

$$\alpha^{(M)} = \frac{2\beta}{2\beta + 1 - \frac{C_{sw}^2}{C_{TF}C_{TM}}}. \quad (21)$$

Thus,  $\alpha^{(M)}$  in (10)  $\leq \alpha^{(M)}$  in (17). Up until now, we have  $\alpha^{(M)}$  in (7)  $\geq \alpha^{(M)}$  in (10), and  $\alpha^{(M)}$  in (20)  $\geq \alpha^{(M)}$  in (17)  $\geq \alpha^{(M)}$  in (10). Finally, we compare  $\alpha^{(M)}$  in (7) with the one in (20) by comparing  $1 - C_{TM}/C_{TF}$  with  $(C_{sw}/C_{TM})(1 - (C_{sw}/C_{TF}))$ . As shown in Appendix B, we have  $\alpha^{(M)}$  in (7)  $\geq \alpha^{(M)}$  in (20)  $\geq \alpha^{(M)}$  in (17)  $\geq \alpha^{(M)}$  in (10) except at the middle codes. Therefore, in terms of linearity, bitwise AS is better than subsample-wise DAS-AS, which is better than bitwise DAS-AS, which is better than subsample-wise AS.

#### D. Bitwise RCR-Based Fine LSB Successive Switching

Once the  $N$  MSBs in the fine SAR-ADC are set based on the coarse ADC bits using one of the four methods, the remaining  $M$ -bit LSBs in the fine SAR-ADC can be decided by bitwise RCR-based MCS with  $k = M - 1, \dots, 1$ . The top-plate voltages at step  $k$  can be analyzed using the equivalent half-circuit models shown in Fig. 12, where  $C_x$  is the equivalent

capacitance for the MSBs that have been set using one of these four methods. This is exactly similar to the analysis for the bitwise switched coarse ADC in Section III-B except with an extra  $C_x$ . Hence, the top-plate voltages at step  $k$  can be obtained in the same form as (1), which is rewritten as follows:

$$VIP^{(k)} = VIP^{(k+1)} + \frac{\alpha^{(k)} C_k}{C_{TF}} (1 - 2b_k) (VRP - VCM) \quad (22)$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{(C_{TM} - C_x)(2\beta + 1)}{C_{TF}}}. \quad (23)$$

Substituting  $C_x$  in Fig. 12(c) into (23), we have  $\alpha^{(k)}$  for the case of  $N$  MSBs set by AS with bitwise RCRs, aligned switching with a subsample-wise RCR, DAS-AS with bitwise RCRs and DAS-AS with a subsample-wise RCR shown in the following equation, respectively:

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{C_{TM}}{C_{TF}}} \quad (24)$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{[\sum_{i=M}^{N+M-1} C_i(2b_i - 1)]^2}{C_{TF}C_{TM}}} \quad (25)$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{C_{sw}}{C_{TF}}} \quad (26)$$

$$\alpha^{(k)} = \frac{2\beta}{2\beta + 1 - \sum_{j=i}^{M-1} \frac{C_j}{C_{TF}} - \frac{C_{sw}}{C_{TF}} \frac{2\beta + 1}{2\beta \frac{C_{TM}}{C_{sw}} + 1}}. \quad (27)$$

We see that in all the four cases shown in Fig. 12,  $\alpha^{(k)}$  differs only in the last term in the denominator. The third term in the denominator represents the ratio of the capacitance of the switched bits to the total fine capacitance of the successively decided bits in the fine LSBs. It has the same format as in (4). However, the switched bits in the MSBs are different using different switching methods as reflected in the fourth term in the denominator for each case.

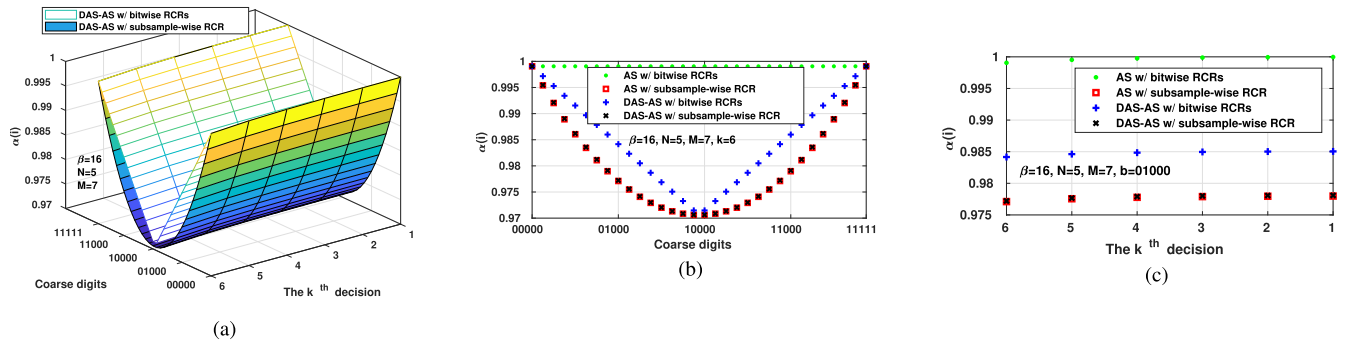


Fig. 13.  $\alpha^{(i)}$  versus coarse digits at each bit decision for the fine LSBs in a segmented architecture. (a) 3-D plot of  $\alpha^{(i)}$  versus coarse digits and decision step ( $k$ ). (b) 2-D plot of  $\alpha^{(i)}$  versus coarse digits for selected decision step ( $k$ ) = 6. (c) 2-D plot of  $\alpha^{(i)}$  versus decision step ( $k$ ) for selected coarse digits = 01000.

It is clear that the error increases by  $C_x$ . We see that  $C_x$  in case II is greater than  $C_x$  in case IV, greater than in case III, and greater than in case I. Hence, for fine LSB switching, AS with bitwise for MSB switching yields the minimal error. But since each of LSB switching has an exponentially smaller weight compared to MSB switching, the reference error introduced by  $\alpha^{(k)}$  is much smaller than  $\alpha^{(M)}$ .

Fig. 13(a) plots  $\alpha^{(i)}$  versus coarse digits (from 00000 to 11111) at each fine bit decision (from  $k = 6$  to 1) for DAS-AS. Fig. 13(b) shows  $\alpha^{(i)}$  versus coarse digits at  $k = 6$ , and (c) shows  $\alpha^{(i)}$  at each fine bit decision when coarse digits are 01000 at four difference cases. From Fig. 13(b) we see  $\alpha^{(i)}$  is almost the same when 5-bit fine MSBs use AS or DAS-AS with subsample-wise RCR. Observe the last term in (27),  $(C_{sw}/C_{TF})(2\beta + 1/2\beta(C_{TM}/C_{sw}) + 1) \geq (C_{sw}/C_{TF})(C_{sw}/C_{TM})$ . It has the same format with the last term in the denominator of (25).  $C_{sw}$  is symmetric according to (11). It has the minimum value at coarse digits 01111 and 10000. Thus,  $C_{sw}^2$  is minimum at 01111 and 10000. This explains why  $\alpha^{(i)}$  in (27) has a single valley at the middle codes.

#### IV. SIMULATION VALIDATION AND DISCUSSION

Behavioral modeling and schematic level simulations were performed to validate the analysis of the segmented SAR ADCs with RCRs. The simulated segmented SAR ADCs with RCRs is shown in Fig. 5, and is implemented in a 65 nm CMOS technology. The coarse unit capacitance  $C_c$  is 2 fF whereas the fine unit capacitance  $C_f$  is 1 fF.

##### A. Static Performance of RCR-Based Segmented SAR ADC

Using analytic formula derived, we can compute, simulate, and compare the static performance differential nonlinearity (DNL) and integral nonlinearity (INL) of RCR-based segmented SAR ADCs. Fig. 14(a)–(d) upper four plots show the respective DNLs and INLs of a segmented 11-bit SAR ADC with a 5-bit coarse and a 12-bit fine SAR ADC using four switching methods for the fine MSBs and  $\beta = 5$ . With  $\beta = 5$ , the 5-bit coarse ADC can compute output digits correctly. These five digits are loaded to the 5-bit fine MSBs using one of four switching methods. As we can see, AS with bitwise RCRs in Fig. 14(a) yields the best static performance (INL/DNL less

than 0.5 LSB). In fact from (7), we can compute the reference error for the 5-bit fine MSBs with  $\beta = 5$  as

$$(1 - \alpha^{(M)})(VRP - VRN) \approx 0.006(VRP - VRN) < \frac{1}{2^7}(VRP - VRN). \quad (28)$$

Thus, the 7-bit fine LSBs can compute results correctly. This yields the INL to be in the range of  $\pm 0.5$  LSB.

The DNLs and INLs in Fig. 14(b)–(d) have some similarities. The segmented misaligned ADC transfer curves lead to different analog input mappings to the same digits, thus causing the DNL at the digits corresponding to misaligned transfer curves to be more than +1 LSB. The INL is the deviation in LSB of the actual transfer function of the ADC from the ideal transfer curve ( $\beta = \infty$ ). The linearity of the segmented ADC is mainly decided by the reference error introduced in the 5-bit fine MSBs. This can be seen from  $\alpha^{(M)}$ , input-normalized ideal and actual transfer curves of 5-bit fine MSBs versus coarse digits plotted in Fig. 14(a)–(d) for four cases. The factor  $\alpha^{(M)}$  affects the transfer curve through modulating the reference voltage in a manner of  $\alpha^{(M)}(VRP - VRN)$ . Thus, the larger  $\alpha^{(M)}$ , the smaller the reference error  $1 - \alpha^{(M)}$ , the modulated actual transfer curve is more close to the ideal curve. To have a better visualization of reference modulation,  $\beta = 1$  is used in plotting  $\alpha^{(M)}$  and actual transfer curves. We see that the deviation of the actual transfer curve from the ideal curve in the 5-bit MSBs has the same shape with the INL of the 11-bit segmented SAR ADC. To minimize the reference error,  $\alpha^{(M)}$  shall be as large as possible. While for minimum switching energy associated with the MSBs switching, DAS-AS with a subsample-wise RCR is a good option.

##### B. Comparison of MCS Based Successive Decision Only and Segmented SAR ADCs With RCR

Table I shows the minimum  $\beta$  to achieve nonlinearity  $\leq 0.5$  LSB of an 11-bit SAR ADC of different architectures with different RCR types. In a segmented architecture, fine MSBs using AS with bitwise RCRs only requires  $\beta \geq 5$ , whereas  $\beta \geq 150$  is needed by using DAS-AS with a subsample-wise RCR. Table II shows the dynamic and static performance, as well as the average switching energy, of an 11-bit SAR ADC with  $\beta = 16$  of different architectures using different RCR types. The dynamic performance is simulated



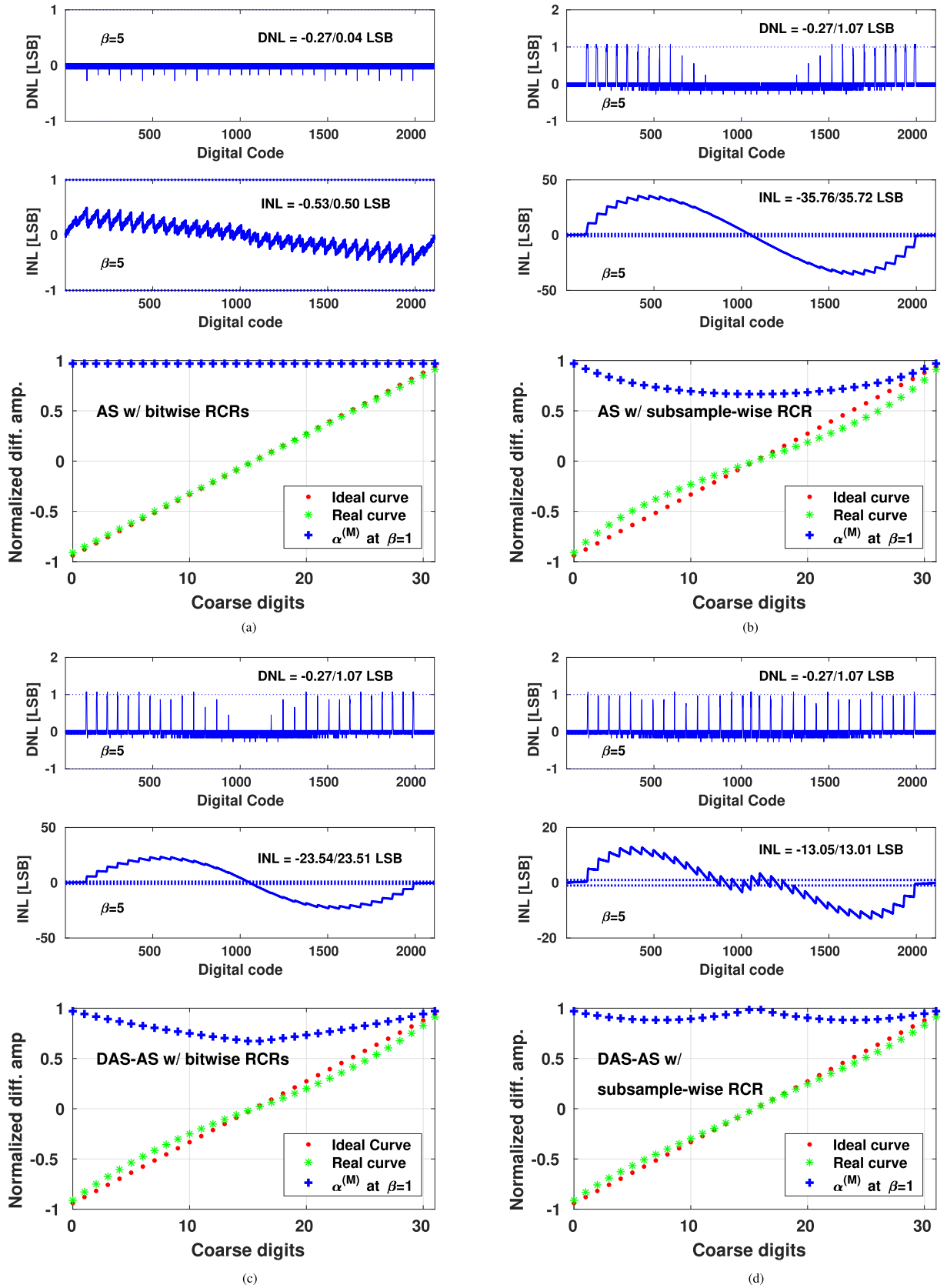


Fig. 14. Static performance and the fine CDAC top-plate voltage versus coarse digits of an 11-bit RCR based charge sharing segmented SAR ADC in which fine MSBs use different switching methods with bitwise or subsample-wise RCRs shown in (a)–(d).

using the sinusoidal input with an amplitude of 0.45 V. The segmented architecture using AS with bitwise RCRs has the best linearity than the other cases, whereas the segmented

architecture using DAS-AS with a subsample-wise RCR has the lowest switching energy at the cost of a slight reduction in the SNDR and linearity. We note that with closed-form

TABLE I  
MINIMUM  $\beta$  TO ACHIEVE NONLINEARITY  $\leq 0.5$  LSB OF AN 11-BIT SAR ADC BASED ON BEHAVIORAL MODEL SIMULATION

Architecture	MCS Decision Only		Segmented Architecture, Coarse: 5-bit, fine:(5+7)-bit *			
RCR Type	bitwise	sample-wise	AS, bitwise	AS, subsample-wise	DAS-AS, bitwise	DAS-AS, subsample-wise
$\beta$	170	256	5	400	280	150

TABLE II

DYNAMIC AND STATIC PERFORMANCE COMPARISON OF AN 11-BIT 50 MS/S SAR ADCS WITH  $\beta = 16$  BASED ON BEHAVIORAL MODEL SIMULATION

Architecture	MCS Decision Only		Segmented Architecture, Coarse: 5-bit, fine:(5+7)-bit *			
RCR Type	bitwise	sample-wise	AS, bitwise	AS, subsample-wise	DAS-AS, bitwise	DAS-AS, subsample-wise
SNDR (dB)	50.47	49.27	66.50	46.3	47.69	59.56
SFDR (dB)	53.56	49.54	84.8	46.43	47.92	63.75
ENOB (bits)	8.09	7.89	10.75	7.4	7.63	9.6
DNL (LSB)	-1/0.01	-1/7.59	-0.07/0.03	-0.17/1.07	-0.17/1.07	-0.17/1.07
INL (LSB)	-5.55/5.54	-6.46/6.45	-0.14/0.2	-11.59/11.66	-7.61/7.68	-4.31/4.38
$E_{ave}^\dagger$ (CVRP <sup>2</sup> )	340.83	340.83	345.36	345.36	105.36	105.36

\* The RCR type in segmented architecture only shows the fine MSBs. Both coarse and fine LSB successive decisions use bitwise RCRs.

† Calculated average switching energy. The energy consumed by  $C_{RCR}$  is almost the same as the DAC switching energy when the linearity is in the range of LSB.

analytic expressions of the reference error derived in this article implemented in digital circuitry, precise error correction can be accomplished even if smaller  $\beta$ s are used.

## V. CONCLUSION

This article presented the theoretical analysis of an RCR technique for segmented SAR-ADC design. Theoretical analysis and simulation have been performed to analyze the error due to the finite reference capacitance. Both the analysis and simulation show that in a segmented SAR ADC, successive bit decisions in both coarse and fine SAR ADCs using *bitwise* RCRs and the MSB copy from the coarse ADC to the fine ADC using *AS with bitwise RCRs*, can reduce  $\beta$  significantly compared with other cases without any performance loss. While the fine MSB copy using detect-and-skip, AS with subsample-wise RCR can reduce reference error and switching energy compared with a successive decision only SAR ADCs with bitwise or sample-wise RCR that have the same  $\beta$ .

## APPENDIX

We provide the derivation of analytic formula in this article. A complete derivation based on charge conservation was provided in [16]. Here, we use the principle of symmetry to simplify the derivation. Note that in the bit decision process of an SAR ADC, the common mode of  $VRP_i^{(k)}$  and  $VRN_i^{(k)}$ ,  $i = N - 1, \dots, k$ , and the common mode of the top plate voltages  $VIP^{(k)}$  and  $VIN^{(k)}$  always stay at the VCM shown in (A1) and (A2), respectively

$$VRP_i^{(k)} + VRN_i^{(k)} = 2VCM \quad (A1)$$

$$VIP^{(k)} + VIN^{(k)} = 2VCM. \quad (A2)$$

### A. Fine MSB Switching

This section derives the solutions of the fine MSB switching using AS and DAS-AS (DAS-AS) with bitwise RCRs from the principle of charge conservation. Refer to Fig. 5, the CDAC of the fine ADC is  $N + M$  bits, here  $N$  is the number of

fine MSBs that equals the number of bits in the coarse ADC, where  $M$  is the number of bits of the fine LSBs,  $C_{TM}$  denotes the  $N$ -bit fine MSB capacitance, and  $C_{TF}$  denotes the total capacitance in the fine ADC.

1) *AS With Bitwise RCRs*: When fine MSBs use AS with bitwise RCRs as described in Section III-C.1, the  $N$ -bit coarse digits are assigned to  $N$ -bit fine MSBs directly. First, the CDAC top-plate charge conserves from the end of the sampling phase to switching  $N$ -bit MSBs in the fine ADC

$$\begin{aligned} (VIP - VCM) \sum_{i=0}^{N+M-1} C_i \\ = \sum_{i=M}^{N+M-1} \left( VIP^{(M)} - (1 - b_i)VRP_i^{(M)} - b_iVRN_i^{(M)} \right) C_i \\ + (VIP^{(M)} - VCM) \sum_{i=0}^{M-1} C_i. \end{aligned} \quad (A3)$$

The term on the left-hand side shows the total charge at the end of sampling. The first term on the right-hand side is the total charge of the  $N$ -bit fine MSBs, and the second term is the total charge of the undecided fine LSBs. Equation (A3) can be rewritten as

$$VIP^{(M)} = VIP + \sum_{i=M}^{N+M-1} \left[ (1 - b_i)VRP_i^{(M)} + b_iVRN_i^{(M)} - VCM \right] (C_i / C_{TF}). \quad (A4)$$

Second, bitwise RCRs top-plate charge conserves, for each bit  $i = N + M - 1, \dots, M$

$$\begin{aligned} (VRP - VRN)\beta C_i + [VCM - (1 - b_i)VIP - b_iVIN]C_i \\ = (VRP_i^{(M)} - VRN_i^{(M)})\beta C_i \\ + \left[ VRP_i^{(M)} - (1 - b_i)VIP - b_iVIN^{(M)} \right] C_i. \end{aligned} \quad (A5)$$

Here, the first term is the charge of the reference capacitor, and the second term is the charge of the bit capacitor.

Equation (A5) can be rewritten as

$$\begin{aligned} \text{VRP}_i^{(M)} &= \frac{\beta}{\beta+1} \text{VRN}_i^{(M)} + \frac{\beta}{\beta+1} (\text{VRP} - \text{VRN}) \\ &+ \frac{1}{\beta+1} [\text{VCM} + (1-b_i)(\text{VIP}^{(M)} - \text{VIP}) \\ &+ b_i(\text{VIN}^{(M)} - \text{VIN})]. \end{aligned} \quad (\text{A6})$$

Using symmetry in (A1) and (A2) and then substituting (A6) into (A4), we obtain

$$\begin{aligned} \text{VIP}^{(M)} &= \text{VIP} + \frac{2\beta}{2\beta+1 - \frac{C_{\text{TM}}}{C_{\text{TF}}}} \\ &\times \sum_{i=M}^{N+M-1} \left[ \frac{(1-2b_i)C_i}{C_{\text{TF}}} (\text{VRP} - \text{VCM}) \right]. \end{aligned} \quad (\text{A7})$$

2) *DAS-AS With Bitwise RCRs*: Refer to Section III-C.2, fine MSBs use DAS-AS with bitwise RCRs. We derive the solution for the case of  $b_{N_i}^c = 1$  with the total switched capacitance  $C_{\text{sw}}$  of  $N$ -bit fine MSBs given in (11). First, the charge on the P-side top-plate is conservative; that is

$$\begin{aligned} (\text{VIP} - \text{VCM}) \sum_{i=0}^{N+M-1} C_i \\ &= (\text{VIP}^{(M)} - \text{VRN}_M^{(M)}) \sum_{i=M}^{N+M-1} (C_i b_i) \\ &+ (\text{VIP}^{(M)} - \text{VCM}) \sum_{i=M}^{N+M-1} [C_i (1-b_i)] \\ &+ (\text{VIP}^{(M)} - \text{VCM}) \sum_{i=0}^{M-1} C_i. \end{aligned} \quad (\text{A8})$$

The left-hand side term shows the total charge at the end of the sampling phase. The first term on the right-hand side is the total charge of the switched bits  $C_{\text{sw}}$  in fine MSBs, the second term is the charge of the skipped bits in the fine MSBs, and the last term is the total charge of the undecided LSBs. (A8) can be rewritten to

$$\text{VIP}^{(M)} = \text{VIP} + \frac{C_{\text{sw}}}{C_{\text{TF}}} (\text{VRN}_M^{(M)} - \text{VCM}). \quad (\text{A9})$$

When fine MSBs use DAS-AS with bitwise RCRs, the reservoir capacitance for each bit is  $\beta$  times larger than its bit capacitance. For each switched bit, that is,  $i = N + M - 1, \dots, M$ , at the reference VRN bottom-plate, we have

$$\begin{aligned} (\text{VRN} - \text{VRP})\beta C_i + (\text{VCM} - b_i \text{VIP})C_i \\ &= (\text{VRN}_i^{(M)} - \text{VRP}_i^{(M)})\beta C_i + (\text{VRN}_i^{(M)} - b_i \text{VIP}^{(M)})C_i \end{aligned} \quad (\text{A10})$$

(A10) is written to

$$\begin{aligned} \text{VRN}_i^{(M)} &= (\beta/(\beta+1))(\text{VRP}_i^{(M)} + \text{VRN} - \text{VRP}) \\ &+ (1/(\beta+1))(\text{VCM} + \text{VIN}^{(M)} - \text{VIN})b_i. \end{aligned} \quad (\text{A11})$$

Using symmetry of (A1) to eliminate  $\text{VRP}_i^{(M)}$ , and then substituting (A11) into (A9), we have

$$\text{VIP}^{(M)} = \text{VIP} + \frac{2\beta}{2\beta+1 - \frac{C_{\text{sw}}}{C_{\text{TF}}}} \frac{C_{\text{sw}}}{C_{\text{TF}}} (\text{VRN} - \text{VCM}). \quad (\text{A12})$$

## B. Comparison of Four Methods

We compare  $\alpha^{(M)}$  in (7) with the one in (20) by examining the last two terms in the denominator. Comparing  $1 - C_{\text{TM}}/C_{\text{TF}}$  with  $(C_{\text{sw}}/C_{\text{TM}})(1 - (C_{\text{sw}}/C_{\text{TF}}))$  is equivalent to compare a constant value to a code-dependent value. We see that  $(C_{\text{sw}}/C_{\text{TM}})(1 - (C_{\text{sw}}/C_{\text{TF}}))$  is a function of  $C_{\text{sw}}$ , while  $C_{\text{sw}}$  is code-dependent as described in (11) and (14). The maximum of  $C_{\text{sw}}$  is  $C_{\text{TM}}$  when the coarse digits are all 0 s or all 1 s. In this case,  $(C_{\text{sw}}/C_{\text{TM}})(1 - (C_{\text{sw}}/C_{\text{TF}})) = 1 - C_{\text{TM}}/C_{\text{TF}}$ . The minimum of  $C_{\text{sw}}$  is reached at the middle codes,  $C_{\text{sw}}$  equals the least significant bit in the  $N$  MSBs, which equals the redundant bit  $C_{\text{red}}$  that is the sum of the  $(M-1)$ -bit fine LSBs  $C_{(M-1)\text{lsbs}}$ . Thus, we have the fine total capacitance expressed as  $C_{\text{TF}} = C_{\text{TM}} + C_{\text{red}} + C_{(M-1)\text{lsbs}}$

$$\begin{aligned} \frac{C_{\text{sw}}}{C_{\text{TM}}} \left( 1 - \frac{C_{\text{sw}}}{C_{\text{TF}}} \right) \\ &= \frac{C_{(M-1)\text{lsbs}}}{C_{\text{TM}}} \left( 1 - \frac{C_{(M-1)\text{lsbs}}}{C_{\text{TF}}} \right) \\ &= \frac{C_{(M-1)\text{lsbs}}}{C_{\text{TM}}} \frac{C_{\text{TM}} + C_{\text{red}}}{C_{\text{TF}}} \leq \frac{C_{\text{red}} + C_{(M-1)\text{lsbs}}}{C_{\text{TF}}} \\ &= 1 - (C_{\text{TM}}/C_{\text{TF}}). \end{aligned} \quad (\text{A13})$$

Because of the redundant bit  $C_{\text{red}}$ , the unswitched bits is the sum of  $C_{\text{red}}$  and  $C_{(M-1)\text{lsbs}}$  in (7). So, we have the inequality in (A13). The “=” holds only at  $C_{\text{red}} = 0$ . Thus,  $\alpha^{(M)}$  in (20) is greater than the one in (7) at the middle codes. Now consider  $C_{\text{sw}}$  is the second smallest, which is the sum of the three least significant bits in the fine MSBs, so  $C_{\text{sw}} = 3C_{(M-1)\text{lsbs}}$

$$\begin{aligned} \frac{C_{\text{sw}}}{C_{\text{TM}}} \left( 1 - \frac{C_{\text{sw}}}{C_{\text{TF}}} \right) \\ &= \frac{3C_{(M-1)\text{lsbs}}}{C_{\text{TM}}} \left( 1 - \frac{3C_{(M-1)\text{lsbs}}}{C_{\text{TF}}} \right) \\ &= \frac{3C_{(M-1)\text{lsbs}}}{C_{\text{TM}}} \frac{C_{\text{TM}} - C_{(M-1)\text{lsbs}}}{C_{\text{TF}}} > \frac{C_{\text{red}} + C_{(M-1)\text{lsbs}}}{C_{\text{TF}}} \\ &= 1 - (C_{\text{TM}}/C_{\text{TF}}). \end{aligned} \quad (\text{A14})$$

For the other coarse codes,  $\alpha^{(M)}$  in (20) is less than  $\alpha^{(M)}$  in (7).

## ACKNOWLEDGMENT

The authors would like to thank anonymous reviewers for insightful comments and Dr. Chixiao Chen for helpful discussions. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of AFRL and DARPA or the U.S. Government.

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