Fully Implantable Cochlear Implant Interface Electronics With 51.2-μW Front-End Circuit

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***Abstract*— This paper presents an ultralow power interface circuit for a fully implantable cochlear implant (FICI) system that stimulates the auditory nerves inside cochlea. The input sound is detected with a multifrequency piezoelectric (PZT) sensor array, is signal-processed through a front-end circuit module, and is delivered to the nerves through current stimulation in proportion to the sound level. The front-end unit reduces the power dissipation by combining amplification and compression of the sensor output through an ultralow power logarithmic amplifier. The amplified signal is envelope detected, and fed to a voltage-controlled current source as a reference for stimulation current generation. The single channel performance has been tested with a thin film pulsed-laser deposition (PLD) PZT sensor for sound levels between 60- and 100-dB sound pressure level (SPL). The proposed front-end signal conditioning unit, which can support different back-end stimulators, dissipates only 25.4 and 51.2 μW based on measurement, for 1- and 8-channel operation, respectively. This represents the lowest in the literature. The interface generates linear stimulation current of 110–430 μA for the given sound range. The single-channel and eight-channel stimulator consume 105 and 691 μW, respectively, for 110-μA biphasic stimulation current.**

***Index Terms*— Fully implantable cochlear implant (FICI), hearing loss, logarithmic amplifier (LA), neural stimulation, piezoelectric (PZT) sensor, ultralow power.**

I. Introduction

ACCORDING to the World Health Organization (WHO), 360 million people have disabling hearing loss greater than 40-dB sound pressure level (SPL) as of 2017. The hearing loss can be mild, moderate, severe, or profound and leads to difficulty in hearing sounds that range from daily conversations to loud noises [1]. Conventional hearing aids can be used for the treatment of mild-to-moderate hearing loss and occupy the largest part of the market. However, for treatment of severe-to-profound hearing loss, where average loss is greater than 90-dB SPL, cochlear implants (CIs) have to be utilized. A CI is the most successful of neural prostheses with more than 120 000 utilizing patients worldwide [2]. Its operation principle is based on the direct stimulation of the auditory nerve, bypassing the eardrum, ossicles, and damaged hair cells. The CI is based on the idea that there is enough auditory nerve fibers left for stimulation. Once the nerve fibers are stimulated, they fire and propagate neural impulses to the brain. The brain interprets them as sounds.

Conventional CIs consist of both external and internal units. The external unit detects sound using a microphone, digitizes the input, and encodes the signal in radio frequency (RF) domain through a processor. The encoded RF signal is transferred to the implanted internal unit with a coupled RF coil pair. The received data are decoded, and the stimulation signal is sent to the auditory neurons through hermetically sealed electrodes [2]–[7]. Although advances in CIs have enabled relatively high quality of hearing, the requirement to wear an external processor that communicates with the implanted device increases power consumption. The limited energy storage and esthetic concerns have redirected recent studies to fully implantable CIs (FICIs) [3], [8].

Sarpeshkar *et al.* [9] proposed an ultralow power programmable analog bionic ear processor with 211 μW of power dissipation. The processor receives a signal from an electret microphone with an on-chip front-end circuit, and slightly compresses the front-end output with an automatic gain control (AGC) circuit. Further compression of the input sound level has been achieved with a logarithmic analog-to-digital converter. The system designed by Georgiou and Toumazou include a single-chip design for speech processor and stimulator for a totally implantable cochlear prosthesis system with processor power dissipation of 126 μW [10]. As in [9], the front-end circuit uses an AGC and a compressor circuit for compression. Both of the CI circuits in [9] and [10] only include the front-end signal conditioning circuit on-chip without high-voltage neural stimulation unit, which is required to deliver proper current stimulation to the auditory neurons. An implantable and low-power signal conditioning integrated circuit (IC) have been reported in [11] for sensing a piezoelectric (PZT) middle-ear sensor. Although the optimized stimulation pulse shape leads to reduced power dissipation

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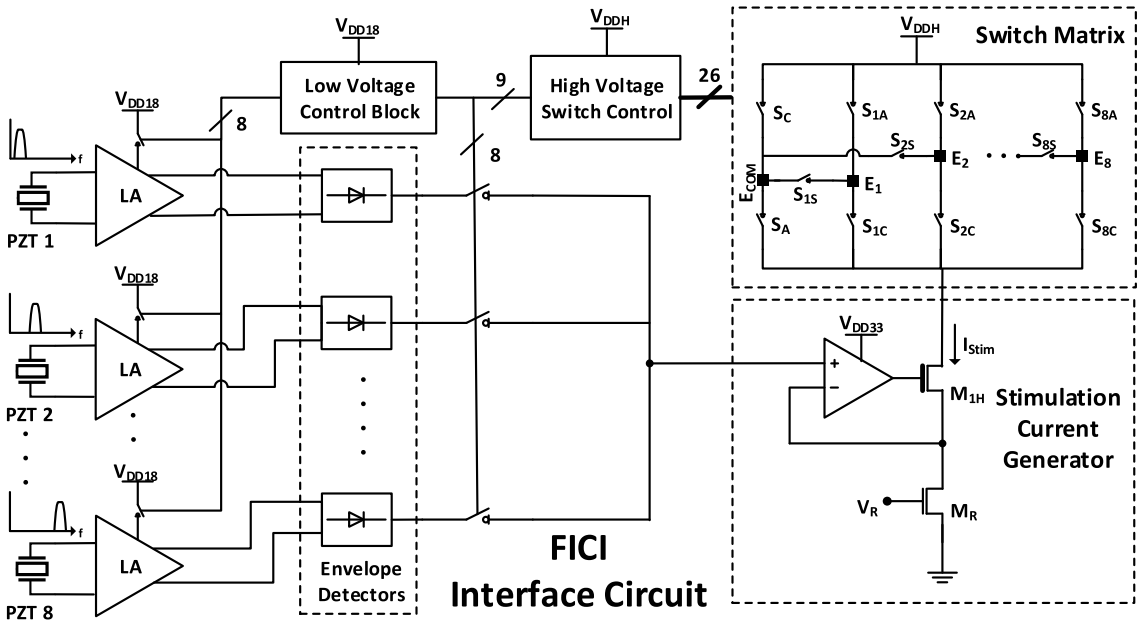

Fig. 1. FICI system architecture.

of about 572 μW, the single-sensor architecture with eight filters to isolate distinct frequencies leads to additional power dissipation. The front-end signal processor in the circuit dissipates 93 μW of power. In [12], a fully implantable artificial cochlea powered by energy harvesting is proposed. The interface circuit senses the acoustic sensor output and stimulates the auditory neurons; however, the interface electronics does not satisfy the basic requirements of FICIs such as continuous stimulation and on-chip integration for low volume. Marsman *et al.* [13] proposed a highly controllable signal conditioning front-end circuit, but the power dissipation of the circuit is above 1 mW.

In this paper, an ultralow power and FICI interface circuit are proposed in order to reduce the power dissipation compared to aforementioned systems, and improve the signal conditioning simultaneously. The circuit senses signals from a set of PZT cantilevers with different resonance frequencies and stimulates the auditory neurons according to the power level and frequency of the input signal. The organization of this paper is as follows. The proposed circuit design is briefly described in Section II. Section III presents the FICI test results with a thin film PZT sensor. Finally, the conclusion is summarized in Section IV.

II. Interface Circuit Design and Description

Fig. 1 depicts the block diagram of the FICI system with eight PZT sensors delivering signals at different frequency bands. This FICI system is an improved version of the one presented in [14] with an on-die control block. Implantable PZT sensors generate low voltage signals from input sound due to their limited size. Thus, the first block of the interface is a logarithmic amplifier (LA). The dynamic range of daily sound of relevance is around 40 dB, but the electrical stimulation range of the diseased cochlea is below 15 dB [15]. The LA helps to both amplify the PZT sensor output and compress the input sound range to the electrical dynamic range of the cochlea. The differential output of the LA is then envelope detected through a full-wave rectifier to obtain the sound level at each PZT sensor. The envelope detector output is sampled with a switch, and held stable as a reference to determine the amplitude of the stimulation current. The sampled signal is fed to the stimulation current generator block, which adjusts the current level to stimulate the auditory neurons. As the final stage, the stimulation current is converted into a biphasic pulse, and is transferred to the corresponding electrode (E_1–E_8) with the help of a switch matrix. The switch matrix control for the biphasic current is provided by a high-voltage switch control block, which uses level shifters to generate high-voltage switch control signals from the channel selection signals. Most of the stimulator power is dissipated on the neural load, and stimulator circuit design has specific criteria based on the voltage compliance and load characteristics. While the utilized topology provides more than 100-μA biphasic current, which is required for stimulation of the neurons, the number of low-power design techniques applicable to the stimulator circuit is unfortunately limited. On the other hand, circuit solution space available for the front end is much wider in addressing the system power dissipation problem. Therefore, most of the FICI low power enhancements proposed in this particular work have front end at the focus. Moreover, the front-end circuit is designed to operate in analog domain to prevent the power dissipation overhead due to analog-to-digital and digital-to-analog conversion. The design and analysis of each subcircuit is provided below.

A. Logarithmic Amplifier

Previously reported CI interfaces compressed the input sound with a nonlinear function through a dc compression stage after the envelope detector, to cover all daily sound levels [4]–[6]. In the scope of this paper, an LA has been designed as the first stage to both amplify and logarithmically compress the signal from the PZT sensor. Dual function of the amplifier eliminates power consumption associated with the

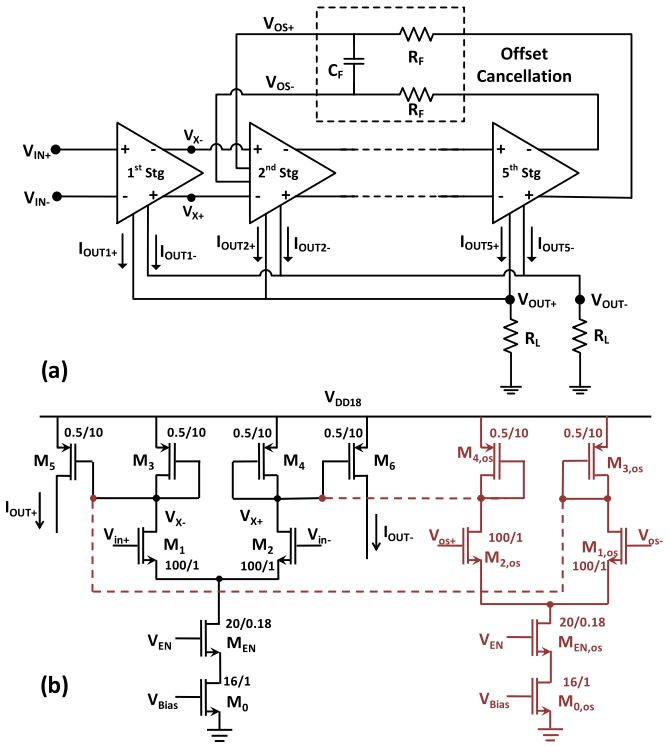

Fig. 2. (a) LA circuit with offset cancelation feedback from the last stage to the second stage. (b) Amplifier stage design with the second stage additions for enhanced offset cancelation highlighted in red.

compression block in the previous designs. The LA is composed of five stages, as shown in Fig. 2(a) and provides high enough gain to detect the low voltage sensor output (>1 mV). As the input amplitude increases, each stage enters the limiting state (saturation) one by one from the fifth stage toward the first stage. Increasing the number of stages leads to higher power dissipation, and early saturation of the output voltage. The number of stages has been determined by considering the tradeoffs between the input dynamic range and the power dissipation. Increasing the number of stages from 5 to 6 enables amplifier operation with lower input voltage (<1 mV); however, the PZT sensor utilized in this system operates with 1–100-mV output range at its resonance frequency, as shown in Fig. 12. On the other hand, increasing stage number from 5 to 6 increases the power dissipation of LA by about 20%. The five-stage is optimized to logarithmically amplify up to 100-mV input level, which matches the sensor output for 100-dB SPL.

Fig. 2(b) presents the topology utilized at each LA stage. Power consumption is managed through selective power gating of a lower supply voltage ($V_{\rm DD}$ = 1.8 V) compared to the rest of the FICI interface. When a particular channel is not sampled, the LA is dynamically disabled through enable signal [$V_{\rm EN}$ in Fig. 2(b)] for power management. The low-power and low-frequency operation of the system lead to low-dc droops, and low *di/dt* induced ac noise, which limits the fluctuations on the supply.

The differential output current from each amplifying stage ($I_{\rm OUT1-5}$) is delivered to a resistive load through current mirrors (M_3-M_6), to be summed with the differential output from the other stages. The input stage of each amplifier includes an isolated nMOS, which improves the gain through increased transconductance (g_m) for the same bias current and transistor size. The staging amplifiers operate in the subthreshold domain for lower power dissipation, and include diode connected transistors as active load, which results in stage voltage gain of $A_v = g_{m1}/g_{m3}$. Total output of the LA is $V_{\rm OUT} = R_L(I_{\rm OUT1} + I_{\rm OUT2} + I_{\rm OUT3} + I_{\rm OUT4} + I_{\rm OUT5})$ where ac output current at each stage is $I_{{\rm OUT},i} = (g_{m,M1,2})_i v_{{\rm in},i}$. For subthreshold operation $g_m = I_D/2nV_T$ and I_D has exponential characteristic with respect to the input voltage as $I_D \approx 2nK_N V_T^2 e^{(V_G - V_{\rm TH}/nV_T)}$ where n is the subthreshold slope factor, V_G is the gate voltage which is the input voltage for our case, V_T is the thermal voltage, K_N and V_{TH} are the transistor parameters [16]. Therefore, the cascade amplifier provides the logarithmical amplification and compression as given in the following equation:

$$V_{\rm OUT} = R_L \sum_{i=1}^{5} I_{{\rm OUT},i} = R_L \sum_{i=1}^{5} K_N V_T e^{\frac{v_{{\rm in},i} - V_{\rm TH}}{nV_T}} v_{{\rm in},i}. \quad (1)$$

Feedback from the last stage is applied to the second stage in order to cancel the effect of dc offset at the input. Fig. 2(b) highlights the offset cancelation enhancements (in red) to the amplifier at the second stage. Saturation of the stages causes clipping of amplifier output, and hence reduces the effect of offset cancelation, but built-in low-pass filter with low cutoff frequency in the feedback loop ensures continuous operation of the LA.

The subthreshold operation of the LA contributes to reduced noise level at the input. The total noise of a MOSFET can be modeled as given in the following equation, where first and second terms shows the drain thermal noise and gate voltage flicker noise, respectively [16]:

$$\overline{v_n^2} = \frac{4kT\gamma}{g_m} + \frac{K_f}{C_{\rm ox}WLf} \quad (2)$$

where k is the Boltzmann constant, T is the operation temperature, g_m is the transconductance of the MOSFET, and γ is the excess noise factor which is around 1/2 for weak inversion region. The empirical coefficient K_f for nMOS devices is essentially independent of bias, fabrication, and technology, while for pMOS devices, this coefficient depends on the biasing condition [16], [17]. Therefore utilizing nMOS transistor as the input pair helps to increase the design reliability after fabrication. $C_{\rm ox}$, W, and L are the technology and design parameters that represent the oxide capacitance, width, and length of the MOSFET. f is the operation frequency.

The total input-referred noise for the first and the second stages of the amplifier is given respectively, in

$$\overline{v_{\rm eq,stg1}^2} = 2\left(\overline{v_{n,M_1}^2} + \frac{g_{m3}^2}{g_{m1}^2}\left(\overline{v_{n,M_3}^2} + \overline{v_{n,M_5}^2} + \frac{\overline{v_{n,R_L}^2}}{R_L^2 g_{m5}^2}\right)\right) \quad (3)$$

$$\overline{v_{\rm eq,stg2}^2} = 2\left(2\overline{v_{n,M_1}^2} + \frac{4g_{m3}^2}{g_{m1}^2}\left(2\overline{v_{n,M_3}^2} + \overline{v_{n,M_5}^2}\right) + 2\overline{v_{n,R_F}^2}\right). \quad (4)$$

The loading effect of offset cancelation stage applied at the second stage reduces the voltage gain of this stage to $g_{m1}/2g_{m3} = A_v/2$. The input-referred noises of 3rd–5th stages

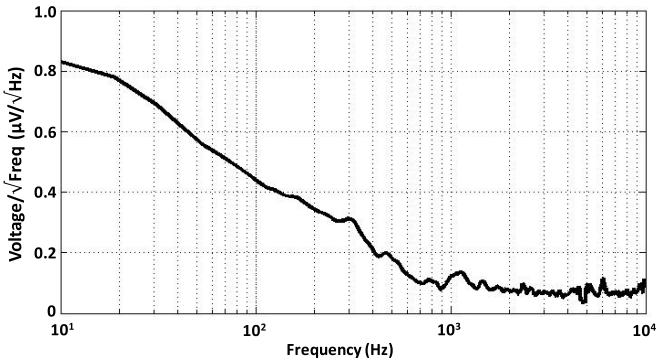

Fig. 3. Measured input-referred noise density variation of LA with frequency.

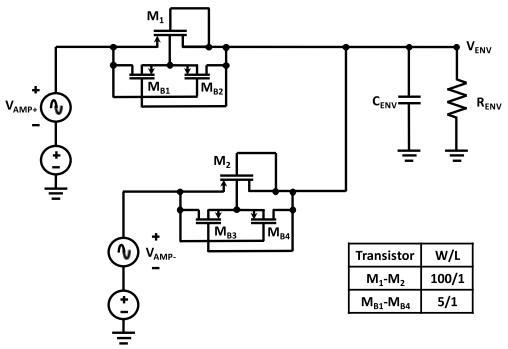

Fig. 4. Two-transistor full-wave rectifier circuit.

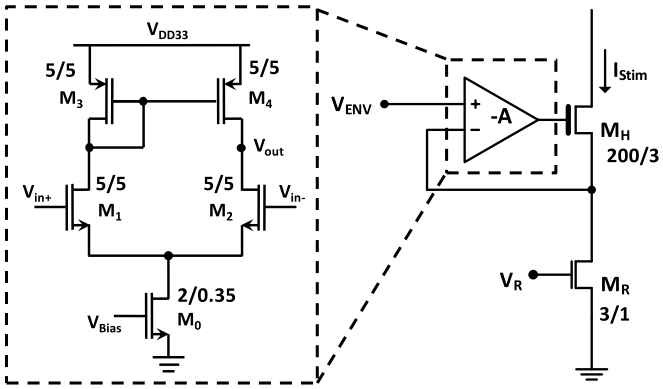

Fig. 5. Schematic of the stimulation current generator with VCR.

are the same with the first stage; hence, the total input-referred noise ($v^2_{\text{eq,LA}}$) can be expressed as shown in

$$\overline{v^2_{\text{eq,LA}}} = \overline{v^2_{\text{eq,stg1}}}\left(1+\frac{4}{A_v^4}+\frac{4}{A_v^6}+\frac{4}{A_v^8}\right)+\overline{v^2_{\text{eq,stg2}}}\frac{1}{A_v^2} \quad (5)$$

where A_v is the voltage gain at first stage as given above. Noise coming from the next stages can be reduced by increasing the voltage gain (A_v). When the voltage gain (A_v) is higher than 10 V/V, the terms with A_v^2, A_v^4, A_v^6, and A_v^8 in the denominator can be eliminated by approximating $1/x \approx 0$ for $x \gg 1$. Therefore, the total input-referred noise can be approximated as given in the following equation:

$$\overline{v^2_{\text{eq,LA}}} \approx \overline{v^2_{\text{eq,stg1}}}. \quad (6)$$

The input transistors M_1 and M_2 are the most critical components that influence the input-referred noise of the amplifier. The size of these MOSFETs are arranged to get higher transconductance hence lower thermal noise. The flicker noise of the circuit is reduced by using large gate area at M_1 and M_2 [18]. The amplifier flicker noise could be further ratified by applying chopping and stabilizing circuits; however, this was not deemed necessary for this application, since input-referred noise is much lower than sensor output [19]. Moreover, high voltage gain leads to $g_{m1} \gg g_{m3,5}$ and decreases the effect of M_3 and M_5 on the input-referred noise. Fig. 3 presents the measurement at the variation of the input-referred noise of the LA with frequency. The total measured input-referred noise integrated from 10 Hz to 10 kHz is 11.1 μV_{rms} where the simulated input-referred noise is 6.83 μV_{rms}. The small variation between the simulation and measurement results can be caused due to the parasitic resistances obtained after fabrication and through the wire bonds. The noise of the large feedback resistors (>100 MΩ) at the offset cancelation stage is around 10 μV_{rms} for the 10-Hz–10-kHz frequency range. Therefore, the feedback is applied to the second stage instead of the first stage to reduce their effect at the input of the LA (10 $\mu V_{\text{rms}}/A_v < 1$ μV_{rms}) while providing offset cancelation below 10 mV. The low input noise of the amplifier provides safe operation for inputs >100 μV.

B. Envelope Detector

The envelope detector at the next stage of the FICI system senses the amplitude of the signal from the amplifier and controls the stimulation current level. The envelope detection can be achieved with either half-wave or full-wave rectification. Half-wave rectifiers with a single diode have high output ripple. On the other hand, the conventional full-wave rectifiers have lower output ripple, but suffer from twice the voltage drop and higher power dissipation due to the four-diode design. The designed envelope detector can achieve full-wave rectification with only two diode-connected MOSFETs, as shown in Fig. 4. The differential output of the previous stage provides both noninverted and inverted outputs which enable the full-wave rectification. The operation principle of the envelope detector is as follows. When $V_{\text{AMP+}}$ is positive, MOSFET M_1 turns on to charge the envelope capacitor C_{ENV}up to peak voltage, minus a diode drop. When $V_{\text{AMP+}}$ falls below C_{ENV} voltage, M_1 is turned off. $V_{\text{AMP–}}$ signal is the inverse of $V_{\text{AMP+}}$, and works in a similar fashion. The passive structure of the envelope detector limits the power dissipation to voltage drops at diode-connected transistors. The voltage drop is minimized by using pMOS transistors which have lower the threshold voltage due to bulk regulation. Bulks of the pMOS transistors are shorted to their sources via bulk regulation transistors (M_{B1-B4}), which prevent the threshold voltage variation due to body effect [20], [21]. A similar two diode envelope detection structure has been proposed in [22], but the pMOS transistors in [22] do not include bulk regulation, and suffers from higher threshold voltage. The envelope detector capacitor (C_{ENV}) and resistor (R_{ENV}) are arranged to have a cutoff frequency of 400 Hz which is close to the frequency of temporal pitch observed in daily life [23], [24]. The envelope detector output is sampled with a switch, and held stable as a reference to determine the amplitude of the stimulation current.

C. Stimulation Current Generator

A current source with a voltage-controlled resistor (VCR) is designed based on [25], where the output current is determined by the envelope detector voltage V_{ENV} and the resistance of M_R, which operates in linear region (Fig. 5). The voltage-controlled current source provides both high-output impedance and high-voltage compliance. The output resistance of the current generator is $R_{\mathrm{OUT}} = Ag_{m,M_H}r_{o,M_H}R_{M_R}$ where A is the open-loop voltage gain of the feedback amplifier, r_{o,M_H} is the output resistance of M_H transistor, and R_{M_R} is the resistance of the VCR. High gain of the feedback amplifier provides higher output for the current generator which results in lower load sensitivity for the stimulation current. Fig. 5 also depicts the utilized single stage active loaded differential amplifier for feedback, which provides about 50-dB voltage gain. The amplifier is supplied by 3.3 V to provide enough voltage for driving the high voltage M_H transistor that is connected to the high-voltage switch matrix. The negative feedback at the amplifier circuit equalizes drain voltage of M_R to the input voltage (V_{ENV}); hence, the generated stimulation current is $I_{\mathrm{stim}} = V_{\mathrm{ENV}}/R_{M_R}$. The maximum and minimum stimulation current levels can be customized for the patient by controlling the gate voltage of M_R. In the proposed design V_R is an analog calibration pin to externally control $R_{\mathrm{MR}} = 1/K_N(V_{\mathrm{GS}} - V_{\mathrm{TH}})$, where K_N and V_{TH} are the MOSFET parameters, and $V_{\mathrm{GS}} = V_R$. The external control of V_R also enables calibration of the circuit for variation across process, voltage and temperature (PVT).

D. Switch Matrix

As the final stage, the generated stimulation current is converted into a biphasic pulse, and is transferred to the corresponding electrode (E_1–E_8) with the help of a switch matrix. Fig. 6 depicts the schematic of the switch matrix used to drive Electrode 1, and the biphasic stimulation current generated through the control of this matrix in time domain. $\mathrm{S}_{1,A}$ and S_C in the switch matrix are pMOS switches whereas $\mathrm{S}_{1,C}$, $\mathrm{S}_{1,S}$, and S_C are nMOS switches. The anodic pulse is generated by turning ON $\mathrm{S}_{1,A}$ and S_A while the cathodic pulse is propagated through $\mathrm{S}_{1,C}$ and S_C. The load driven by the switches is the electrode tissue impedance, which is modeled as a series resistor-capacitor pair (R_S = 1–10 kΩ and C_d = 1–10 nF) [11], [26]. Switch $\mathrm{S}_{1,S}$ is utilized to remove the charge on the capacitor at the load, and prevents the charge imbalance at the electrodes by shorting them to the common electrode (E_{COM}) when they are disabled. The channel length of the MOSFET switches is 3 μm, the minimum allowed value for high-voltage MOSFETs in the utilized process. The switch matrix is powered by a high-voltage supply (V_{DDH} = 7–10 V) to deliver the sufficient voltage to the stimulation electrodes. The stimulation electrode is driven according to the well-known continuous interleaved sampling (CIS) sound processing strategy, which provides sequential interleaved stimulation of the electrodes at fixed frequency, and delivers the better performance compared to other synchronous implementations by preventing the electromagnetic interference between the electrodes [27], [28]. The sequential electrode stimulation at the CIS strategy prevents the electromagnetic interference between the electrodes that may leads to charge imbalance at the neurons.

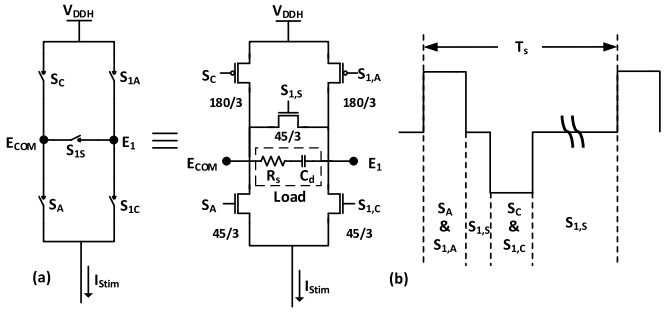

Fig. 6. (a) Switch matrix utilized at electrode 1. (b) Generated biphasic stimulation current.

E. Control Unit

The control unit comprises a resettable one-hot state machine, as depicted in Fig. 7 that generates LA enable signals, sampling signal of the switching between channels, and switch matrix control signals for eight-channel CIS stimulation. The LA enable and sampling signals consist of 100-μs pulses triggered by a 10-kHz clock. Sampling is followed by the stimulation signal generation per electrode. Stimulation period of 1 ms at each channel is timed by a second (1 kHz) clock. After the stimulation of the last channel, a done signal is generated to reset the machine, and wait for the next rising edge of the low-frequency clock. A "CH_MODE" signal allows switching between 1-channel and 8-channel operation modes. The anodic and cathodic pulses at each stimulation electrode are obtained through a simple combinational logic which uses electrode selection signals (S_1–S_8) and the clock signals as the input.

III. Test Results and Discussion

The FICI interface circuit was designed and implemented in 180-nm high-voltage CMOS technology. Fig. 8 presents the die micrograph of the implemented FICI interface circuit, where the layout of the one-channel neural stimulation circuit is highlighted. As the first step, the performance of amplifier was tested for varying input voltage and frequency conditions. The LA not only amplifies the sensed voltage at the input but also fits the input voltage range to the electrical dynamic range of auditory neurons as well. Fig. 9(a) shows the input–output characteristics of the LA that compresses 40-dB input voltage to 12-dB output. The compression is done according to $y = C\ln(x) + D$, where the compression ratio is determined by C. The trendline shows that the LA output linearly changes with the logarithm of the input, and the measurements are consistent with the simulations. Moreover, the error at the output voltage with respect to the linearity curve is obtained. The results indicate that the error at the output is always lower than 20 mV, and the maximum percent error is below 10%. Therefore, the linearity of the amplifier stays in the acceptable range to be utilized at implantable applications. The LA is tested with 40 dB (1–100 mV) input dynamic range, which is the range

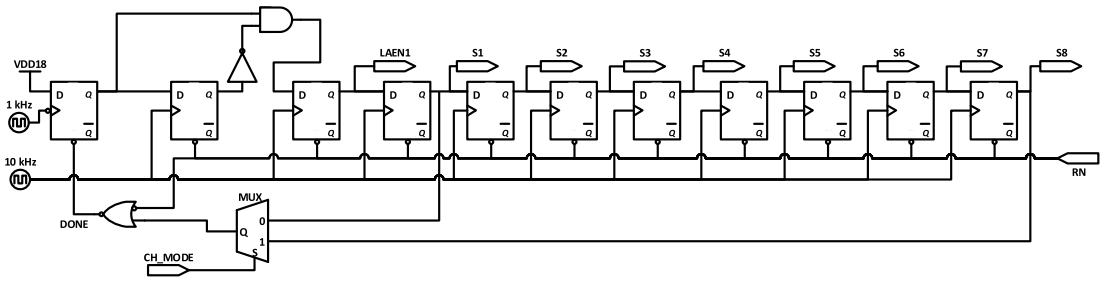

Fig. 7. Schematic of the resettable one-hot state machine of the control unit.

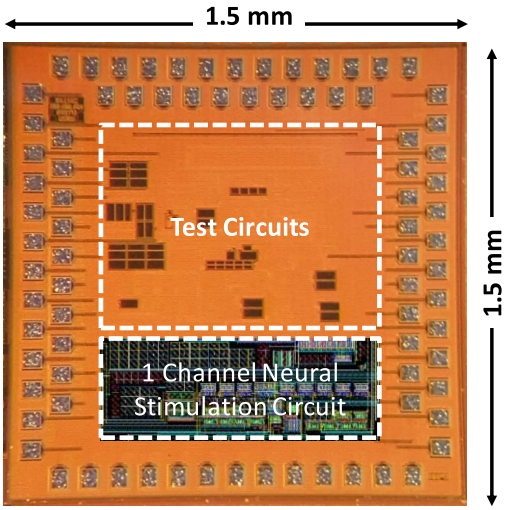

Fig. 8. Die micrograph of the designed and implemented FICI interface circuit.

of the low-volume PZT sensor utilized during the tests. The simulations demonstrate more than 50-dB input range, which shows that the circuit is well suited for an implantable sensor with a wider dynamic range. The amplifier has been tested at different frequencies to validate its operation. Moreover, the gain response of the amplifier is obtained for input voltage with 1- and 10-mV peak as shown in Fig. 9(b). A -3-dB bandwidth of the LA is higher than 10 kHz that captures the whole daily speech band. The normal mode of operation for an LA includes saturation of the stages, which leads to THD of the amplifier increases with increasing input voltage. The measured THD of the LA for 1- and 100-mV inputs are 3% and 46%, respectively. Since daily sounds are not observed at high frequencies, the amplifier design provides a favorable tradeoff between bandwidth and power dissipation.

Operation of the front-end circuit is validated as shown in Fig. 10. The input signal is a sinusoid with time-domain frequency of 1.5 kHz and amplitude modulation frequency of 200 Hz with 10-mV maximum peak. The amplifier generates a differential output pair, which is amplified and compressed with respect to the input voltage level. At the next stage, the envelope of the amplifier output is captured via the envelope detector through which the amplitude variation of the input signal is determined. The envelope detector output is then sampled to provide stable voltage at the stimulation current generator input. This enables the same current level at anodic and cathodic stimulation pulses.

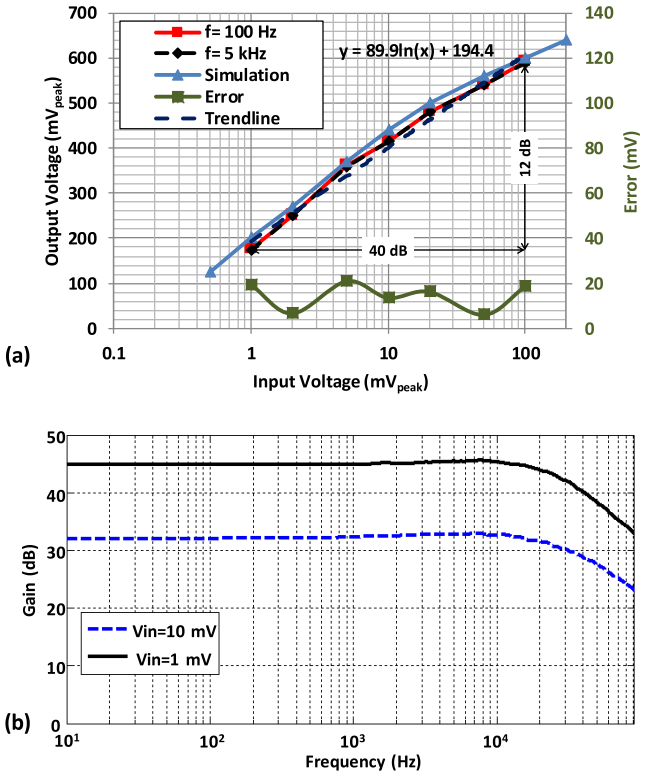

Fig. 9. (a) Output voltage variation of the LA with respect to the input peak voltage at different frequencies. (b) Gain response of the LA for 1- and 10-mV input peak voltages.

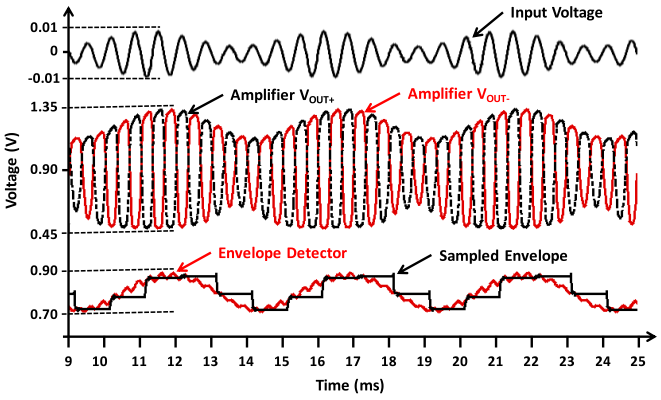

Fig. 10. Schematic of the stimulation current generator with VCR.

The single channel performance of the FICI interface circuit has been tested with a thin film pulsed-laser deposition (PLD) PZT sensor to provide a proof of concept. Fig. 11 shows the

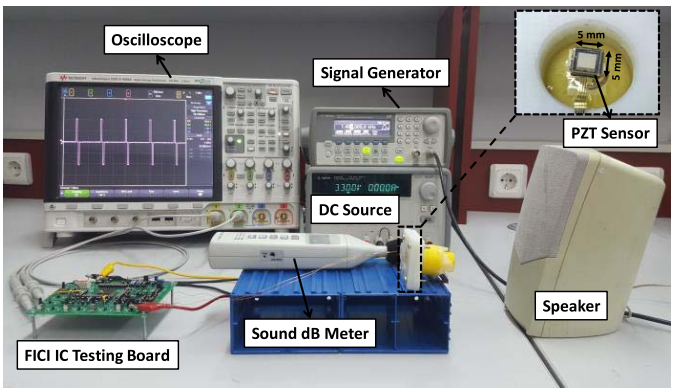

Fig. 11. Test setup of the single channel FICI interface circuit with a thin film PZT sensor.

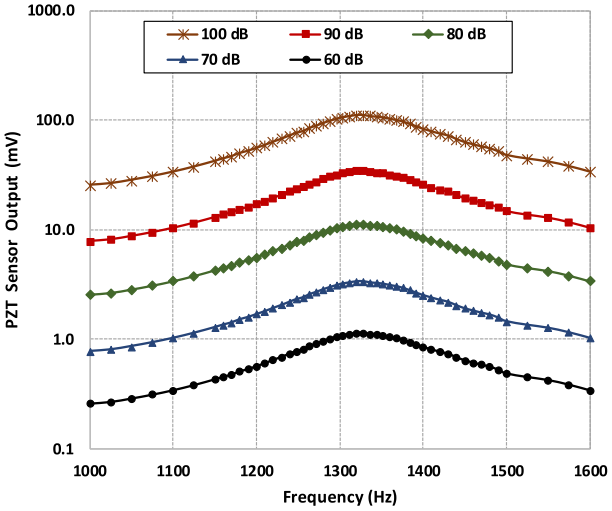

Fig. 12. Frequency response of the thin film PLD PZT sensor attached on the parylene membrane.

test setup of the design. The input sound of the testing system is generated by a speaker which is driven by a signal generator to control the sound frequency and level. The generated sound level by the speaker has been measured by sound decibel meter. The incoming sound vibration has been detected by the PZT sensor on a parylene membrane and converted into electrical signal. Size of the sensor is adjusted to be 5×5 mm^2 which can be implanted on the eardrum or on the umbo at middle ear [29], [30]. The fabrication process of the sensor is similar to the one explained in [31]. Moreover, a more compact design that fits eight PZT sensors to the volume of the middle ear has been proposed in [24]. Fig. 12 presents the frequency response of the PZT sensor attached on the membrane at different input sound levels. The resonance frequency of the PZT sensor is 1330 Hz. The sensor output at resonance frequency changes from 1 to 100 mV at a range of 60–100-dB SPL. The sensor output is then fed to the FICI interface on the testing board which is powered by a dc source. Test results of the FICI interface are observed with the help of a digital signal oscilloscope.

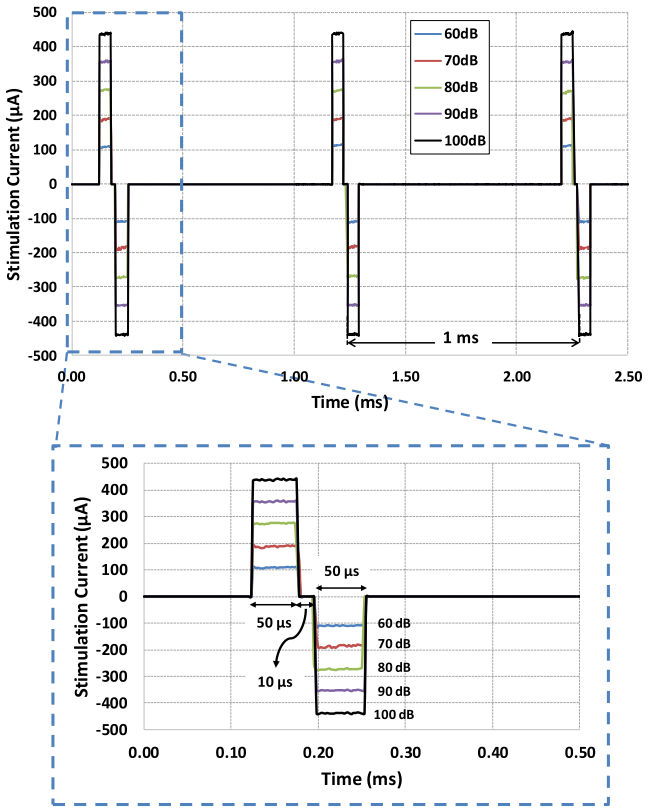

Fig. 13. Stimulation current generated by the FICI interface electronics when fed with a thin film PLD-PZT film PLD PZT sensor attached on the parylene membrane.

TABLE I
POWER CONSUMPTION OF THE FICI INTERFACE CIRCUIT

System Components	Supply Voltage (V)	Power (µW)	
		1-Ch	8-Ch
Logarithmic Amplifier	1.8	0.35	2.8
Envelope Detector	1.8	0.38	3.0
Control Block	1.8	20.0	20.0
Stimulation Current Generator	3.3	1.7	5.2
Switch Matrix (Stimulator)	7-10	80	640
HV Switch Control	10	3	20.2
Total		105.43	691.2

The neural stimulation performance of the FICI is tested with an artificial neural load ($R_s = 3$ kΩ and $C_d = 10$ nF). Fig. 13 shows the neural stimulation current generated at Electrode 1, for different input sound levels at the resonance frequency of the PZT sensor. The generated biphasic pulses have linear response with the input sound level. The stimulation current amplitude changes between 110 and 430 μA, which represent the threshold and comfort levels. The stimulation generator is programed to yield 1000 pulses/s with 50 μs of biphasic pulsewidth per phase.

Table I shows the power consumption for various blocks in the FICI system. The LA, envelope detector, and control

TABLE II
COMPARISON OF FICI INTERFACE CIRCUIT WITH STATE OF THE ART

Parameters	Sarpeshkar TBME05 [9]	Georgiou JSSC05 [10]	Yip JSSC15 [11]	This Work
Technology	1.5 µm	0.8 µm	180 nm	180 nm
Number of Electrodes	16	16	8	8
Operation Domain	Analog + Digital	Analog	Analog + Digital	**Analog**
Dynamic Range (dB)	77	45	59	40
Front-End Power (µW)	211	126	93	**51.2**
Stimulator Power (µW)	-	2000*	479	640
FoM**	5.84	5.71	5.16	**6.25**

*Estimated by Georgiou *et al*., not implemented on the chip
**FoM=(Dynamic Range)x(Number of Electrodes)/(Front-End Power)

unit operate with 1.8-V supply voltage. The average power dissipation of the LA in one period is less than 3 μW due to the implemented power management scheme. If the LA is not disabled when corresponding channel is not active, the total power dissipation of LA and envelopes detectors for eight channel are about 60 μW which is higher than total power dissipation of the proposed front-end circuit. The stimulation current generator operates with standard 3.3-V supply to drive M_{1H} with a sufficiently high voltage and provides wide operation range for this high threshold transistor. The switch matrix that actuates the stimulation current requires at least 7 V in order to accommodate the high impedance of the electrode–tissue interface. The high-voltage switch control circuit is hence supplied to 10 V in this implementation in order to completely turn the switches on and off, and prevent leakage to the auditory neurons. Different supply voltages can be utilized at the FICI system through power management circuits with dc–dc converters, which is out-off scope of this paper. The front-end signal conditioning circuit, excluding the stimulation current, dissipates only 25.43 and 51.2 μW at single and eight-channel operation, which is the lowest value in the literature to the best of our knowledge. The total power dissipation of the single and eight-channel circuit at 110-μA stimulation current is 105.43 and 691.2 μW, respectively. The power consumption of the eight-channel circuit is extrapolated from single channel measurements and the simulation results. Implantable neural stimulator systems can be powered by lithium/manganese dioxide ($LiMnO_2$) batteries with 3.3-V nominal voltage and 300-mAh/g gravimetric capacity density [32]. Using a power management circuit for buck (1.8 V) and boost (10 V) voltage conversion with a modest 70% power conversion efficiency, the total power dissipation of the neural stimulator can be kept below 1 mW. The proposed system can thus operate for 37 days on a 1-g battery.

Table II presents the comparison of the FICI interface with the state of the art. The input dynamic range of the proposed design is slightly lower than the previously reported interface circuits, but provides the sufficient range to cover daily sounds [33], [34]. The input dynamic range of the circuit is designed according to the range of the targeted PZT sensor. The input dynamic range of the amplifier can be increased by extending the gain and cascaded stage numbers if the system dynamic range is targeted differently, but there is likely to be a power dissipation penalty. Neural stimulation consumes 479 μW in [11] using nonrectangular stimulation waveforms. The proposed FICI interface in this paper dissipates 640 μW with regular biphasic pulses. This can be further decreased by optimizing current waveform shape, which is not the focus of this paper. A figure of merit (FoM) has been determined to quantitatively compare system performance against the state of the art by combining three important parameters for FICI design: dynamic range, electrode number, and power dissipation. Although, increasing dynamic range and channel number of the circuit is effective on the speech perception, power dissipation is a limiting factor for the lifetime of an implantable system. The proposed circuit provides the highest FoM compared to previous works. Most of the previously reported studies operate both in analog and digital domains to obtain filtering, compression, and patient fit of the incoming sound, whereas the proposed design eliminates digital filter and compression blocks. Therefore, the proposed circuit does not require ADC and DAC blocks to switch between analog and digital domains. The front-end signal conditioning circuit, which is the main focus of this paper, has the lowest power consumption compared to the previous studies due to the circuit reduction and power optimization techniques detailed in Section II.

IV. CONCLUSION

In this paper, an ultralow power FICI interface circuit has been presented, which senses the multiple signals from PZT sensors with distinct resonant frequencies and stimulates the auditory neurons with biphasic stimulation current. Multiple PZT sensor inputs eliminate the bandpass filters utilized in previous CIs. The LA array carries out the amplification and compression of the signals from PZT sensors. Amplification and compression are separately implemented functions in previous CI designs with higher aggregate power dissipation. Each LA is powered by the lowest supply voltage in the system when active, and is otherwise power-gated to further reduce both active and idle power dissipation. The neural stimulation performance of the interface circuit has been tested with a thin film PLD PZT sensor while driving an artificial neural load. The system provides 110-μA stimulation current for 60 dB of input sound, which is the threshold stimulation level of the system, and the comfort level of 430 μA for 100-dB SPL. Threshold and comfort levels can be adjusted postimplantation through a properly designed patient fitting circuit with digital interface. The digital inputs can be utilized to control the gate voltage, V_R at the stimulation current generator block through a low-power DAC. The minimum power dissipation of the front end and overall FICI interface is

25.4 and 105.4 μW, respectively, for single channel. For eight-channel operation, the extrapolated power data shows that the front-end circuit dissipates 51.2 μW, and the full circuit dissipates 691.2 μW. While the front-end circuit achieves the lowest power dissipation in the literature as the main focus of this paper, full-circuit power dissipation is also one of the lowest for biphasic stimulation. Power dissipation of the overall circuit can be further decreased by applying optimized nonrectangular waveform shapes for neural stimulation. The eight channel performance of the FICI system will be tested with properly designed eight PZT sensors in the speech band.

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