A Fully Integrated Discrete-Time Superheterodyne Receiver

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***Abstract*— The zero/low intermediate frequency (IF) receiver (RX) architecture has enabled full CMOS integration. As the technology scales and wireless standards become ever more challenging, the issues related to time-varying dc offsets, the second-order nonlinearity, and flicker noise become more critical. In this paper, we propose a new architecture of a superheterodyne RX that attempts to avoid such issues. By exploiting discrete-time (DT) operation and using only switches, capacitors, and inverter-based gm-stages as building blocks, the architecture becomes amenable to further scaling. Full integration is achieved by employing a cascade of four complex-valued passive switched-cap-based bandpass filters sampled at 4× of the local oscillator rate that perform IF image rejection. Channel selection is achieved through an equivalent of the seventh-order filtering. A new twofold noise-canceling low-noise transconductance amplifier is proposed. Frequency domain analysis of the RX is presented by the proposed DT model. The RX is wideband and covers 0.4–2.9 GHz with a noise figure of 2.9–4 dB. It is implemented in 65-nm CMOS and consumes 48–79 mW.**

***Index Terms*— Bandpass filter (BPF), discrete time (DT), IIP2, process scalable, receiver (RX), superheterodyne, switched capacitor.**

I. Introduction

THE superheterodyne with resonant bandpass filters (BPFs) tuned at a fixed intermediate frequency (IF) was the architecture of choice for wireless receivers (RXs) that were constructed with discrete components [1]. With the invention and popularization of integrated circuits (ICs), the zero IF (ZIF) architecture (and also low IF) has attracted designers to make fully monolithic RXs. It has been predominant ever since [1].

A. Superheterodyne Versus Zero-IF Receiver Architecture

The main attraction of the ZIF architecture is that it does not require a BPF, which is needed in a superheterodyne for image rejection. Instead, it relies on low-pass filters (LPFs) for channel selection, which are much easier to integrate in CMOS. This has traditionally resulted in a lower cost and power consumption.

The advantages of ZIF obviously do not come for free. Since the local oscillator (LO) coincides with the RF signal of interest, LO self-mixing problems arise [2]. The LO leakage to the LNA input is amplified and then mixed with LO again, creating a *dc offset* that could be two to three orders of magnitude larger than the wanted signal [2]. If that leakage is radiated through the antenna and received back, it can create a *time-variant* dc offset. Consequently, in general, a dc offset cancellation loop is required to dynamically remove it [3].

Furthermore, ZIF RXs suffer from *limited IIP2*, mainly by the RF downconversion mixer. When a large modulated (or closely spaced two-tone) blocker is received, a second-order nonlinearity intermodulates the blocker to around dc (IM2 product), where the wanted signal also resides, thus deteriorating the signal-to-noise ratio. In the superheterodyne front end, the wanted signal resides at a high IF that is far from the IM2. Therefore, this architecture shows a very high IIP2. For applications requiring a high IIP2 [3], [4], ZIF RXs need elaborated IIP2 calibration techniques [4]–[8].

In addition, most of the filtering and amplification in a ZIF RX are done after the mixer at low frequency, where *flicker noise* of devices corrupts the wanted signal and increases noise figure (NF). In contrast, filtering and amplification in a superheterodyne are usually done beyond the devices' flicker corner.

However, the superheterodyne architecture has its own challenges. The first one is integration of BPF that has been targeted in recent works [9]–[12]. The second challenge is image frequency due to phase/amplitude mismatch between quadrature LO signals at the RF mixer. An in-band/out-of-band blocker (depending on the IF) could be located at the image frequency that demands a high quadrature accuracy.

In summary, the ZIF architecture can be easily integrated, but it suffers from dc offset, IIP2, and flicker noise. Supplementary circuitry and techniques are used to relax these handicaps. Instead, superheterodyne avoids all these problems, while it has its own challenges to the integration of BPF and handling the IF image. Now, accounting for the recent advancements in CMOS technology and RF techniques, the historical superheterodyne could afford full integration of RX to deliver an acceptable performance with less overhead.

B. Why Discrete Time?

While key motivations of CMOS scaling have been to reduce transistor cost and to improve digital performance,

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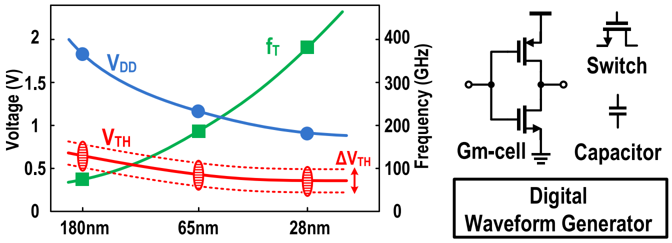


(a) (b)

Fig. 1. (a) Typical CMOS scaling trends for low-power/low-leakage process technology. (b) Components used in DT signal processing.

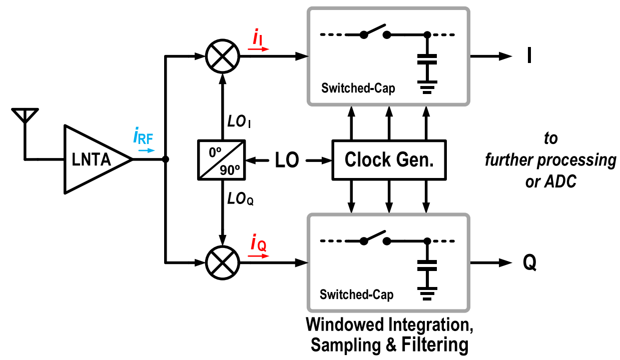


Fig. 2. Simple DT RX with passive switched-capacitor filter.

conventional RF/analog designs do not benefit significantly. As shown in Fig. 1(a), going from 180- to 28-nm CMOS, V_{DD} is reduced almost by half while MOS threshold voltage (V_{th}) has not changed considerably. Therefore, the available precious voltage headroom for RF/analog design is now reduced dramatically [13]. Also, considering the reduced MOS intrinsic gain [13] and its saturation linearity [14], RF/analog design is becoming generally more difficult. On the other hand, majority of cellular and wireless standard frequency bands are allocated in 0.4–6 GHz, and have not significantly changed for many years. Meanwhile, transistor cutoff frequency (f_T) has improved dramatically with scaling [see Fig. 1(a)]. This suggests that conventional RF/analog techniques, which were optimized and fine-tuned for the older IC processes, do not effectively use the ultrahigh speed of transistors of scaled CMOS to improve performance (except NF that improves with f_T increase [13]).

In contrast, discrete-time (DT) passive RF/analog building blocks, shown in Fig. 1(b), avoid using complicated analog components, such as opamps. Most signal processing and filtering are done using passive switched-capacitor circuits [15], [16] that can work at low V_{DD}. As the technology scales, MOS switches become faster and tinier with less parasitic capacitances. Moreover, capacitor density improves, resulting in a reduced area. Clocks are also generated using digital logic that becomes also faster and more power efficient with the scaling. To provide signal gain, DT techniques use inverter-based gm-cells that are always compatible with digital technology with improving gm over bias current. In this way, DT RXs directly benefit from scaling similarly to digital circuits. References [9], [10], [12], and [17]–[21] are the examples of DT process-scalable RXs.

C. Paper Structure

This paper is organized as follows. Section II describes theoretically required sampling scheme for the superheterodyne architecture without IF images. In Section III, the proposed DT superheterodyne RX, its model, and operation are explained. Then, in Section IV, operation and implementation of a sampling mixer and BPF are described. An analysis is done to find location of images and their rejections in this RX. In Section V, a new low-noise transconductance amplifier (LNTA) with twofold noise canceling is proposed to be used at the RF front end. Section VI elaborates on the analog baseband (BB) signal processing, up to the Analog-to-Digital Converter (ADC). Measurement results are presented in Section VII, with the conclusions in Section VIII.

II. Discrete-Time Receiver

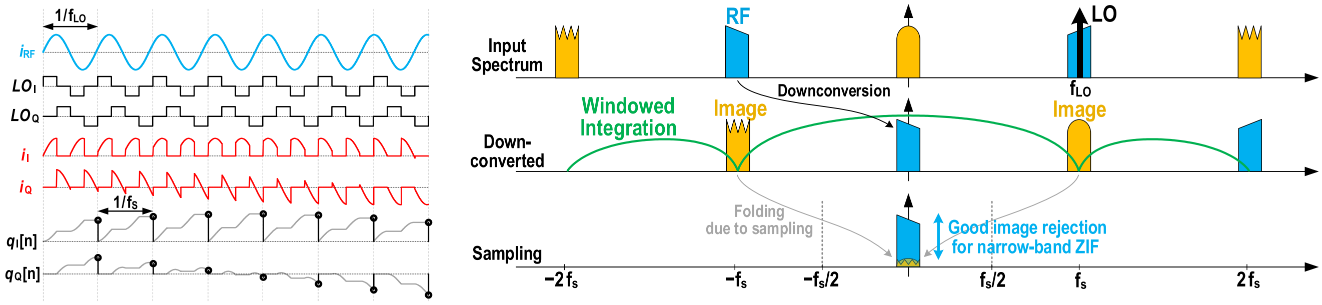
A simplified conceptual diagram of a DT ZIF RX is shown in Fig. 2. It consists of an LNTA, a pair of quadrature mixers, and DT sampling LPFs. The received RF signal is amplified and converted into current, i_{RF}, by the LNTA with high output impedance [22]. This current is then downconverted to ZIF by the quadrature mixers. The mixers are driven by the quadrature $\mathrm{LO}_{I,Q}$ signals (at f_{LO}), which are differential 25% duty-cycle clocks with 90° phase shift. Fig. 3(a) shows signal waveforms for a narrow-band modulated RF signal. The downconverted current $i_{I/Q}$ is integrated over a time window $T_i = 1/f_s$ and sampled as DT charge packets, $q_{I,Q}[n]$ [16]. The windowed integration (WI) forms a continuous-time (CT) *sinc* antialiasing filter just before the sampling, and attenuates unwanted signals folded from multiples of the sample frequency f_s (i.e., sampling images) [17]–[19], [23]. The DT data are then low-pass filtered by a passive switched-cap circuit (e.g., a second-order IIR [15]–[17]). In most of the DT ZIF RXs, this sampling is done at a significantly lower rate than f_{LO} [17]–[19], [24], [25].

A. 1× Sampling in Zero IF

In the DT ZIF RX in Fig. 2, consider a case where the signal $i_{I,Q}$ is sampled at the same rate as the LO frequency ($f_s = f_{\mathrm{LO}}$), hereafter, 1× *sampling*, also known as "direct sampling" in [18]. The time-domain signal waveforms were shown in Fig. 3(a). This RX has sampling images at multiples of f_{LO}. Fig. 3(b) shows the frequency translations. The wanted RF signal is downconverted to dc by mixing with the quadrature LO tone. At the same time, frequency bands near dc and $-2f_{\mathrm{LO}}$ are translated to $\pm f_{\mathrm{LO}}$. The CT antialiasing filter created by WI has its notches coinciding with the sampling images. The narrower the bandwidth, the stronger the image attenuation [19], [22]. After the sampling, attenuated images at multiples of $\pm f_s$ are folded over the wanted signal at BB.

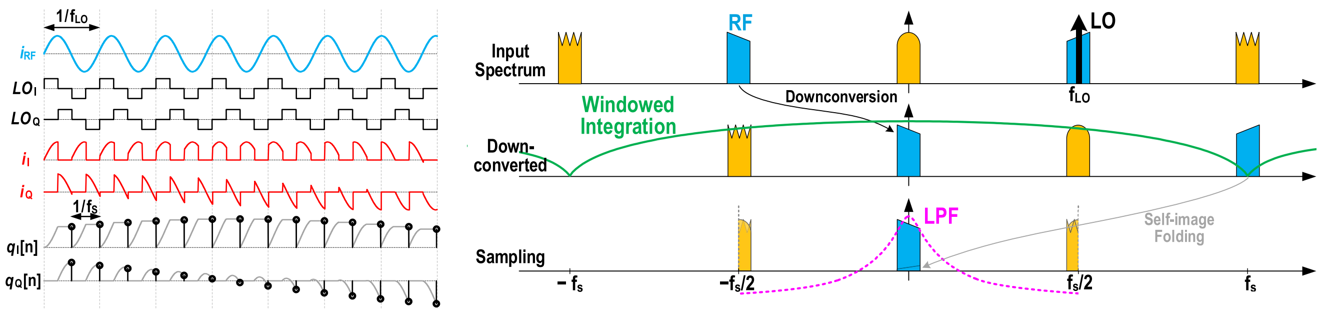
B. 2× Sampling in Zero IF

By doubling the sample rate to $f_s = 2f_{\mathrm{LO}}$ (hence, 2× *sampling*), the ZIF RX does not introduce any sampling images (other than those caused by the mixer's odd harmonics). As shown in Fig. 4, the antialiasing filter is widened



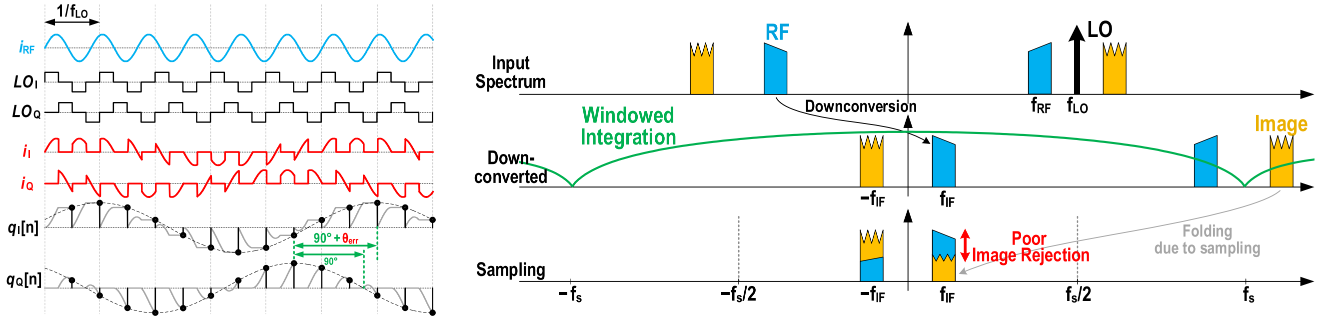
(a) (b)

Fig. 3. (a) Time-domain signal waveforms and (b) frequency translations in a 1× sampling ZIF DT RX. Input spectrum is shifted right (RF downconversion), and after WI, it is then sampled.



(a) (b)

Fig. 4. (a) Time-domain signal waveforms and (b) frequency translation in a 2× sampling ZIF DT RX. "Yellow" bands after the sampling are folded on themselves, but remain apart from the wanted signal and can be filtered afterward by a DT LPF.



(a) (b)

Fig. 5. (a) Time-domain signal waveforms and (b) frequency translation in a 2× sampling DT superheterodyne RX. After the sampling, image is aliased on the wanted signal without enough attenuation.

twofold. After the 2× sampling, the "yellow" bands still remain at high frequency as they are not mixed with the wanted signal. Therefore, it is possible to further filter the images prior to decimation and folding over the wanted signal. The only images created by sampling are self-image of the wanted RF signal and the images that come from the odd harmonics of f_{LO} (e.g., $3f_{\mathrm{LO}}$, not shown in Fig. 4), all attenuated earlier by the antialiasing filter.

C. 2× Sampling in Superheterodyne

If the 2× sampling was to be used in a DT superheterodyne with a high-IF frequency (f_{IF}), where $f_{\mathrm{LO}} = f_{\mathrm{RF}} + f_{\mathrm{IF}}$, it would show a poor image rejection. To illustrate that, let us assume spectra shown in Fig. 5(b). The wanted signal is downconverted to $+f_{\mathrm{IF}}$, while part of the image power is upconverted to $2\ f_{\mathrm{LO}} + f_{\mathrm{IF}}$. By sampling this signal at the 2× rate, this image folds over the wanted signal at $+f_{\mathrm{IF}}$. In addition, note that the notch of WI is not aligned with the image (it is separated by f_{IF}), so the image is not effectively filtered out. To get further insight, let us closely inspect the resulting time-domain $q_I[n]$ and $q_Q[n]$ signals in Fig. 5(a). The phase shift between them is not exactly 90°, as expected for quadrature signals. There is an error of half the sampling period that creates $\theta_{\mathrm{err}} = (T_s/2) \times 2\pi f_{\mathrm{IF}}$ [26] and limits the image rejection.

III. Proposed Discrete-Time Superheterodyne RX

A. 4× Sampling

To solve the above problem of high-IF images introduced by sampling, we propose advancing to a *4× sampling*, i.e., $f_s = 4f_{\mathrm{LO}}$. The I and Q sampled signals in Fig. 6(a) have now precisely 90° phase shift. Although samples with zero value

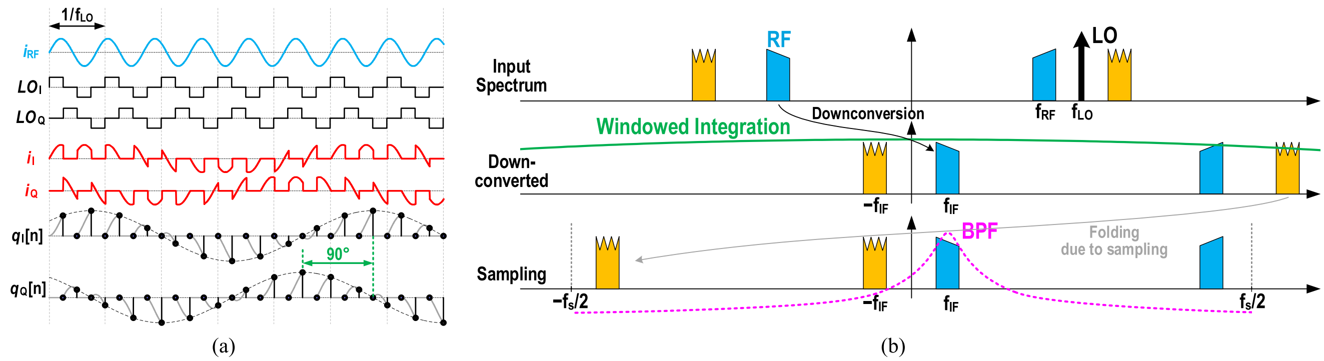


Fig. 6. (a) Time-domain signal waveforms and (b) frequency translations in a 4× sampling DT superheterodyne RX. Since f_s is increased to $4f_{\mathrm{LO}}$, IF image is completely distinct from the wanted signal and can be filtered afterward by a DT BPF.

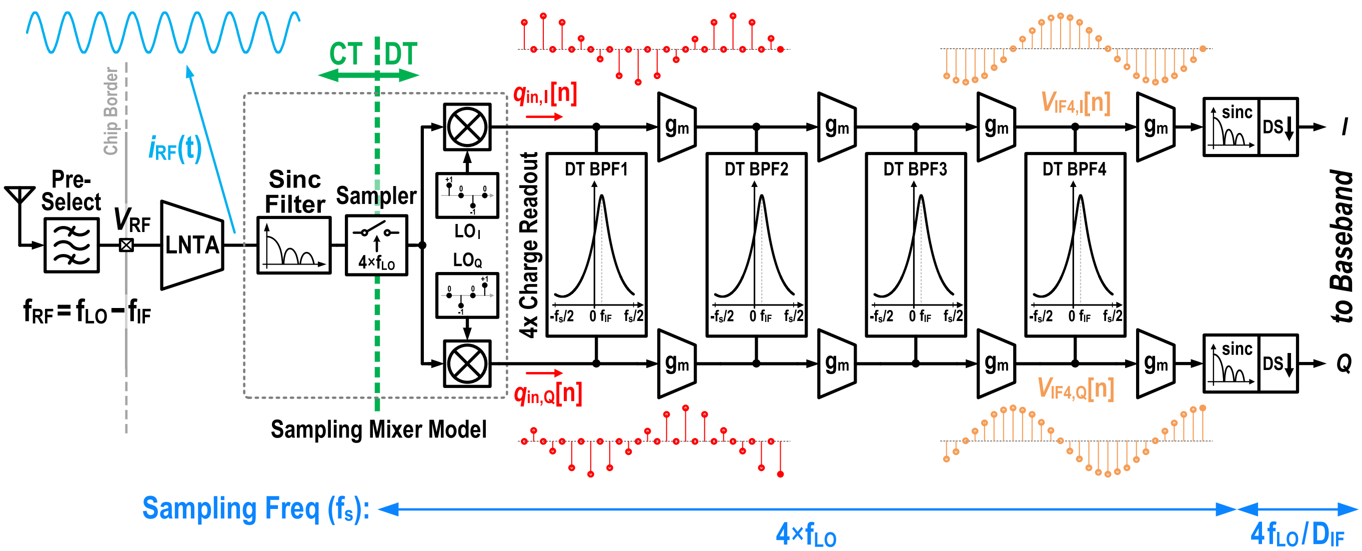


Fig. 7. Proposed DT superheterodyne RX using 4× sampling.

between nonzero samples seem to be noninformative, they are ensuring the quadrature accuracy. Furthermore, consider the signal spectrum in Fig. 6(b). This time, the upconverted image at the mixer output $(2f_{\mathrm{LO}} + f_{\mathrm{IF}})$ folds over $-f_s + f_{\mathrm{IF}}$ by the sampling, keeping it apart from the wanted signal. Then, a DT complex BPF is able to select the wanted signal and filter out the rest. The only images that are translated directly on top of the wanted signal are the mixer's odd harmonic images.

B. DT Model of the Superheterodyne RX

As shown in Fig. 2, the signals at the mixer output are still CT [22]. In reality, the windowed current integration, sampling, and DT processing happen in the subsequent switched-capacitor block. In addition, the squarelike waveforms of mixer clocks, $\mathrm{LO}_{I/Q}$, in Fig. 6(a) possess odd harmonics (i.e., +third, −fifth, and so on), which not only downconvert high-frequency images on top of the wanted signal, but also upconvert the input spectrum to high frequencies around the harmonics. The sampling also folds the spectrum of the signal that is outside of the Nyquist range into the $-f_s/2$ to $+f_s/2$ range. Since both *mixing* and *sampling* processes translate frequencies with respect to the LO harmonics and sampling rate, respectively, they make a rather complicated matrix for a complete picture of frequency translations.

Top-level diagram in Fig. 7 provides a straightforward yet accurate model for the DT RX, illustrating its functionality and the scheme of frequency translations. Since the accumulated charge is read out by the switched-capacitor filter at the 4× rate, and also the states of mixer clocks are changing at the same rate (i.e., 4× in each cycle), these operations are mutually commutative so it would make no difference if we (advantageously) consider the WI and sampling executed ahead of the mixing. In this way, the rest of signal processing after the sampling is done in the DT domain ([26] explains well the difference between CT and DT interpretation of signals in a DT mixing RX). Therefore, the "DT mixers" interpret their input signals as DT input sequences instead of the CT square waveform. Also, the outputs of DT mixers become sampled-charge data rather than the CT i_I and i_Q waveforms of Fig. 6(a).

DT charge packets after WI and sampling are described as

$$q_{\mathrm{in}}[n] = \int_{(n-1)T_s}^{nT_s} i_{\mathrm{RF}} \cdot dt \tag{1}$$

where i_{RF} is the result of LNTA input voltage (v_{RF}) multiplied by its transconductance $g_{m,\mathrm{LNTA}}$. This WI creates a CT *sinc* type filter [16]–[19], [22]–[24] prior to the sampler

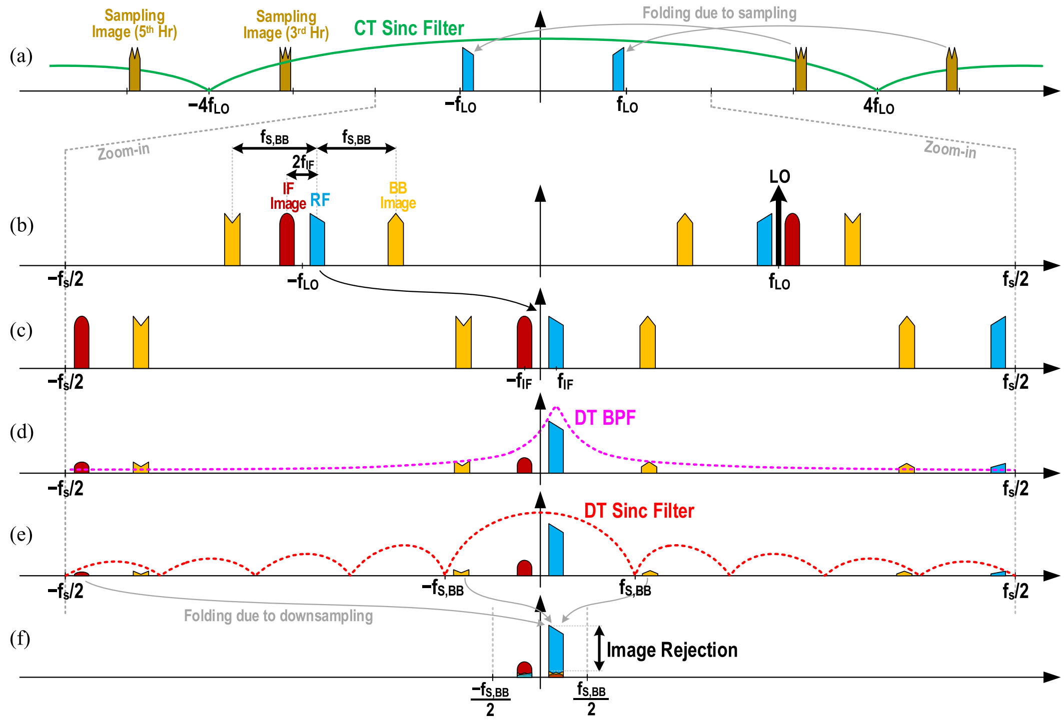


Fig. 8. Operation of the DT superheterodyne RX. (a) Images caused by sampling of CT signal. (b) Input spectrum after the sampling. (c) Downconverted spectrum after the DT mixer. (d) Signals after IF filter stages. Decimation by (e) applying an antialiasing filter before (f) BB downsampling.

in Fig. 7

$$H_{\mathrm{WI}}(f) = T_s \times \frac{\sin(\pi f T_s)}{\pi f T_s} = T_s \times \operatorname{sinc}\left(\frac{f}{f_s}\right). \qquad (2)$$

C. Operation of the Receiver

Operation of the proposed HIF DT RX is shown in Fig. 8. As the CT input signal enters the RX (Fig. 7), it is filtered by the CT sinc filter described in (2) with $f_s = 4f_{\mathrm{LO}}$. Images are then created due to sampling, as indicated in brown in Fig. 8(a). In this example (with $f_{\mathrm{RF}} = f_{\mathrm{LO}} - f_{\mathrm{IF}}$), sampling images are at $-f_{\mathrm{LO}} + f_{\mathrm{IF}} + k\cdot(4f_{\mathrm{LO}})$ and $f_{\mathrm{LO}} - f_{\mathrm{IF}} + k\cdot(4f_{\mathrm{LO}})$ for $k = 1, 2, 3, \ldots$ From (2), sinc filter attenuations of the first two images ($k = 1$) near the third and the fifth f_{LO} harmonics are 9.5 and 14 dB, respectively, the same as the image attenuation of a CT four-phase mixer. The sampling images are further attenuated by the LNTA, but generally a preselect filter is required.

After sampling, the DT input spectrum is now spread from $-f_s/2$ to $+f_s/2$, where $f_s = 4f_{\mathrm{LO}}$. Fig. 8(b) shows the wanted RF signal and the important images. After mixing the entire signal spectrum with the complex LO tone, the negative side is downconverted to around dc, while the positive side is upconverted to close to $\pm f_s/2$ [see Fig. 8(c)]. At this point, the wanted signal is located at $+f_{\mathrm{IF}}$ while its IF image (in red) is at $-f_{\mathrm{IF}}$.

The spectrum of Fig. 8(c) is then filtered by the complex DT BPFs in the IF strip [see Fig. 8(d)]. At this point, out-of-band images and blockers are attenuated enough, such that the signal of interest can be decimated to a lower BB sample rate, $f_{s,BB}$. This leads to power consumption reduction for the remainder of processing blocks. The decimation is being protected by a DT sinc antialiasing filter that is simply achieved by adding up D_{IF} samples [also known as moving average (MA)] [22]. Therefore, the images are further filtered out [Fig. 8(e)] before downsampling and aliasing [Fig. 8(f)].

IV. Receiver Chain

In this section, the RX chain of Fig. 7 (after the LNTA) is described and analyzed. The LNTA is later discussed in Section V.

A. Sampling Mixer

After conversion of the RF input voltage into current, the sampling mixer does both sampling and DT downconversion of the signal. The LO clock sequences in Fig. 7 are $\mathrm{LO}_I[n] = \{1, 0, -1, 0\}$ and $\mathrm{LO}_Q[n] = \{0, -1, 0, 1\}$. In frequency domain, they exhibit two tones at $\pm f_s/4$, which is f_{LO}, with 90° phase shift between I and Q. From the clock sequences, downconversion gain of each DT mixer becomes $A_{\mathrm{mix},I/Q} = 1/2$. Implementation of the sampling mixer is shown in Fig. 9 and consists of two current commutating passive mixers for I and Q paths.

B. DT I/Q Charge-Sharing Bandpass Filter

After downconversion of the signal, a BPF selects the desired band/channel. Fig. 10 shows the DT charge-sharing BPF (CS-BPF) used in the IF strip [10]. Its inputs are DT charge packets ($q_{\mathrm{in},I}[n]$ and $q_{\mathrm{in},Q}[n]$), and its output are voltage samples ($V_{o,I}[n]$ and $V_{o,Q}[n]$). This filter is based

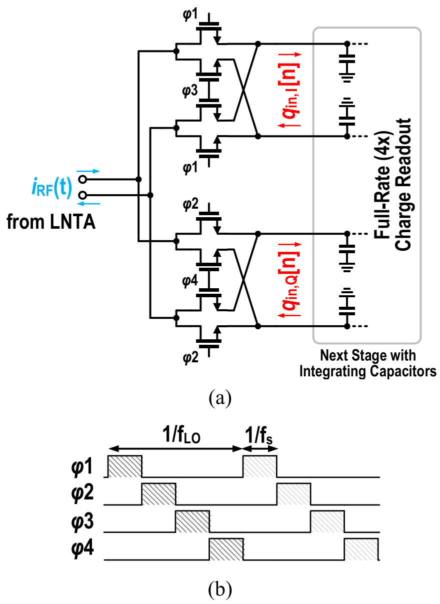


Fig. 9. (a) Implementation of the sampling mixer in Fig. 7 with passive current commutating mixer. (b) Driving clock waveforms.

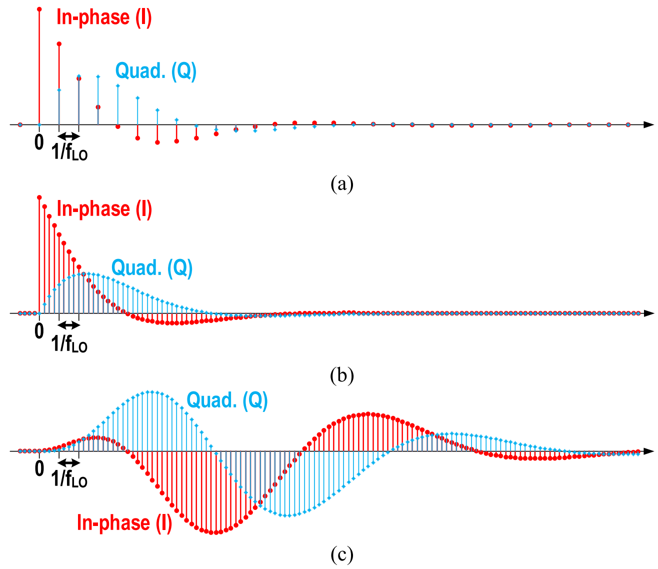


Fig. 11. In-phase impulse response of DT I/Q CS-BPF. Single stage (a) before and (b) after 4× parallelized operation. (c) Four stage with parallelized operation. Note that phase shift between I and Q is 90°.

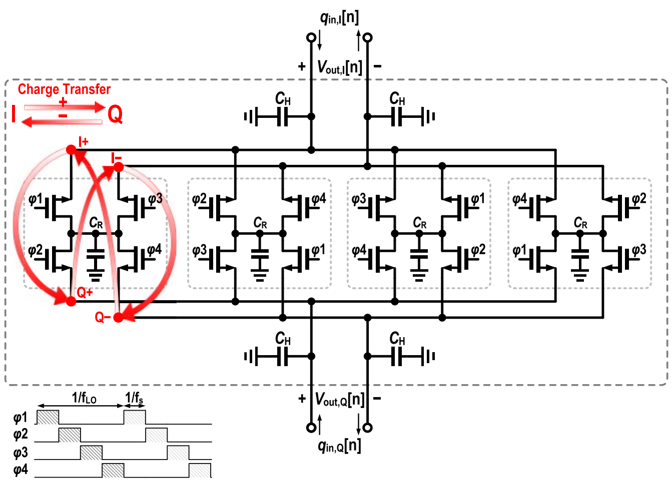


Fig. 10. DT passive I/Q CS-BPF.

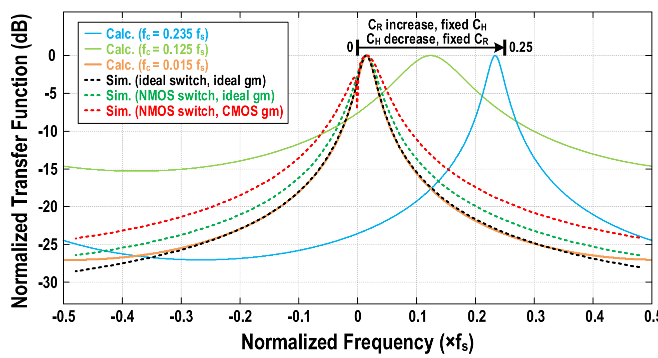


Fig. 12. Normalized TF of the I/Q CS-BPF.

in a sense on the idea of polyphase filter where inputs with different phases (e.g., quadrature I/Q) are combined with different phase shifts [25], [27]. In this way, a real-input/output transfer function (TF) that is symmetric around dc can be shifted to positive or negative frequencies. Thanks to the *passive* implementation of this filter, its linearity is excellent (IIP3 > +30 dBm) while supporting high sample rates of >12 GS/s.

To visualize operation of this BPF, first consider only one of the switched-capacitor banks in Fig. 10. In each cycle ($\varphi 1$ to $\varphi 4$), C_R keeps on sequentially charge sharing with a part of a C_H charge residing at $I+$, then $Q+$, then $I-$ and finally, $Q-$. Therefore, during the whole cycle, part of charge is transferred from I to Q path with positive sign, and from Q to I path with negative sign (shown in red in Fig. 10). As this charge sharing lasts four phases, it does not satisfy the requirement of the 4× sampling. Sample rate is increased 4× through *parallelized operation*[1] [16]: an array of four rotating capacitor banks is used in parallel, each with one additional phase delay. The sample rate is thus increased to $4f_{LO}$.

Assuming inputs and outputs of this filter as complex signals, DT TF of this filter can be derived [30][2]

$$H_{BPF}(z) = \frac{V_{out}}{q_{in}} = \frac{1/(C_H + C_R)}{1 - [\alpha + j(1-\alpha)]z^{-1}} \tag{3}$$

where α is defined as $C_H/(C_H + C_R)$. Fig. 11 shows the impulse response of this filter before and after the parallelized operation. Fig. 12 plots the normalized TFs and compares them with circuit simulations. As C_H increases, center frequency (f_c) of its TF moves toward zero where the BPF gets closer to an LPF, similar to that in [18]. By increasing C_R, charge sharing between I/Q increases as well and shifts f_c away from zero toward $f_s/4$. In the case where C_H is zero, the BPF turns to a complex N-path filter ($N = 4$) with center frequency at $f_s/4$ (i.e., the same as f_{LO}), similar to the one

[1]This is different than the traditional parallelism and pipelining techniques [1], [2] used in digital implementation.

[2]Reference [3] performs full noise analysis of this filter and derives its TF.

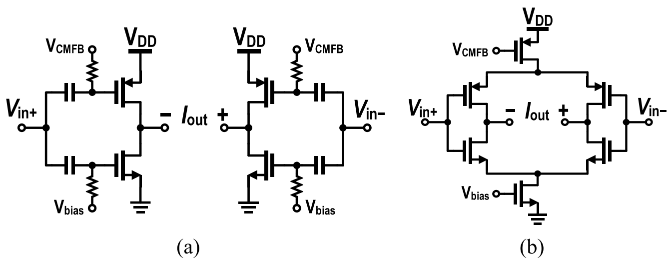


Fig. 13. Implementation of (a) IF and (b) BB gm-cells.

in [31]. Also calculated in [25], f_c derived from (3) is

$$f_c = \frac{f_s}{2\pi}\arctan\left(\frac{C_R}{C_H}\right). \tag{4}$$

This shows that TF of this filter is set only by the sampling frequency f_s and C_R/C_H capacitor ratio. Therefore, it has little sensitivity to process, voltage, and temperature variations. Passband gain (output voltage over input charge) of this filter is calculated by replacing $z = e^{j\cdot 2\pi f \cdot T s}$ in (3) at the center frequency (4)

$$\begin{aligned} A_{\mathrm{BPF}} &= \frac{1}{C_R + C_H\left(1 - \sqrt{1 + (C_R/C_H)^2}\right)} \\ &\approx \frac{1}{C_R} \quad \text{for } C_R \ll C_H. \end{aligned} \tag{5}$$

The only bottleneck of the CS-BPF is its relatively low quality factor, expressed as f_c/BW, of about 0.5 (for $f_c \ll f_s$). Out-of-band filtering can be improved by lowering the f_c value to reduce the bandwidth, or also by cascading more stages to increase the filter's order. Shown in Fig. 7, four BPFs are cascaded to effectively filter out unwanted interferers and blockers.

Gm-cells are exploited to facilitate cascading single-stage filters. Implementation of the IF gm-cell as a simple inverter-based gm [16], [32] [Fig. 13(a)] makes it process scalable. By properly sizing of transistors, their nonlinearities could be canceled out [33], [34]. It could be shown that gain of each gm-cell, defined as output charge over input voltage, is $A_{gm} = g_m T_s$.

C. Decimation

A signal decimation at the end of the IF chain reduces the sample rate. This has been implemented as an MA filter in Fig. 7. It has the following TF:

$$H_{\mathrm{MA,IF}}(f) = D_{\mathrm{IF}} \times \mathrm{sinc}(f/f_{s,BB}) \tag{6}$$

where $f_{s,BB} = f_s/D_{\mathrm{IF}}$. A small resulting attenuation of the wanted signal at f_{IF} is neglected in the rest of the text. The decimation is trivially implemented by lowering the readout rate of the block succeeding the gm-cell. Several samples are accumulated, and then processed once (*temporal decimation* [22]).

D. Image Rejection

Considering the frequency translations in Fig. 8 and the RX model shown in Fig. 7, we are now able to calculate gains of signals at different frequencies from the LNTA RF input to the IF strip output. Using (2), (5), and (6), gain of the wanted RF signal from LNTA input until V_{IF4} is

$$\begin{aligned} G_{\mathrm{wanted}} &= V_{\mathrm{IF4},I/Q}/V_{\mathrm{RF}} \\ &= [g_{m,\mathrm{LNTA}} H_{\mathrm{WI}}(f_{\mathrm{LO}} - F_{\mathrm{IF}}) A_{\mathrm{mix}} A_{\mathrm{BPF}}] \\ &\quad \times [A_{gm,\mathrm{IF}} A_{\mathrm{BPF}}]^3 \\ &\approx \left[g_{m,\mathrm{LNTA}} \mathrm{sinc}(1/4) \times 1/2 \times \frac{1}{f_s C_R}\right] \times \left[\frac{g_{m,\mathrm{IF}}}{C_R f_s}\right]. \end{aligned} \tag{7}$$

In (7), $f_{\mathrm{IF}} \ll f_{\mathrm{LO}}$ is considered.

The closest image that could fold onto the wanted RF signal is the IF image at $f_{\mathrm{LO}} + f_{\mathrm{IF}}$. As shown in Fig. 8(e), part of the IF image energy after mixing and attenuation resides at $-f_s/2 + f_{\mathrm{IF}}$. This signal is folded over the wanted signal after downsampling, assuming an even D_{IF}. Rejection of this image can be calculated by adding attenuations of the BPFs and DT MA filter, from (3) and (6), respectively. Considering $f_{\mathrm{IF}} = f_{\mathrm{LO}}/16$ and $D_{\mathrm{IF}} = 16$, the total IF image rejection (caused by sampling) reaches more than 135 dB. However, quadrature inaccuracy of the practical LO signals also aliases a tiny part of the IF image right after the mixers, from $f_{\mathrm{LO}} + f_{\mathrm{IF}}$ to $+f_{\mathrm{IF}}$ in Fig. 8(b) and (c). The latter effect is predominant and limits the IF image rejection to 40–80 dB, depending on the quadrature accuracy, layout, and mixers' matching.

The second important class of images is BB downsampling images. Translated back to the RF input, they are located at $f_{\mathrm{RF}} \pm k \cdot f_{s,BB}$. The first two (for $k = 1$) are shown in yellow in Fig. 8(b). After mixing down [Fig. 8(c)] and passing through the BPFs [Fig. 8(d)], they are attenuated by the DT MA filter [Fig. 8(e)], and then folded over the wanted signal via downsampling [Fig. 8(f)]. By means of (3), the exact attenuation of BPF can be calculated. As a first-order approximation of (3) for midrange frequencies ($f_{\mathrm{IF}} \ll f \ll f_s/2$), Bode plot of a first-order LPF with a 3-dB bandwidth of f_{IF} is being considered that is shifted to be centered at f_{IF}. So, BPF rejection at $f_{s,BB}$ offset from the passband is approximated as

$$R_{\mathrm{BPF}}(f) \approx \left.\frac{f - f_{\mathrm{IF}}}{f_{\mathrm{IF}}}\right|_{f=f_{\mathrm{IF}}+f_{s,BB}} = \frac{f_{s,BB}}{f_{\mathrm{IF}}}. \tag{8}$$

Both sampling images are attenuated by the same amount, due to the symmetry around f_{IF}. The higher the $f_{s,BB}$ value, the stronger the attenuation. Then, the images are attenuated by the MA filter in (6). A higher $f_{s,BB}$ makes the images relatively closer to notches of the sinc filter, thus improving the attenuation. Adding up all these attenuations, BB downsampling image rejection ratio (IMRR) becomes

$$\mathrm{IMRR}_{BB} \approx \left(\frac{f_{s,BB}}{f_{\mathrm{IF}}}\right)^4 \Big/ \left|\frac{f_{\mathrm{IF}} \pm f_{s,BB}}{f_{s,BB}}\right| \tag{9}$$

where a small attenuation of the wanted signal by (6) is neglected. By choosing a proper number of BPF stages and decimation factor to set $f_{s,BB}$, a desired IMRR can be achieved.

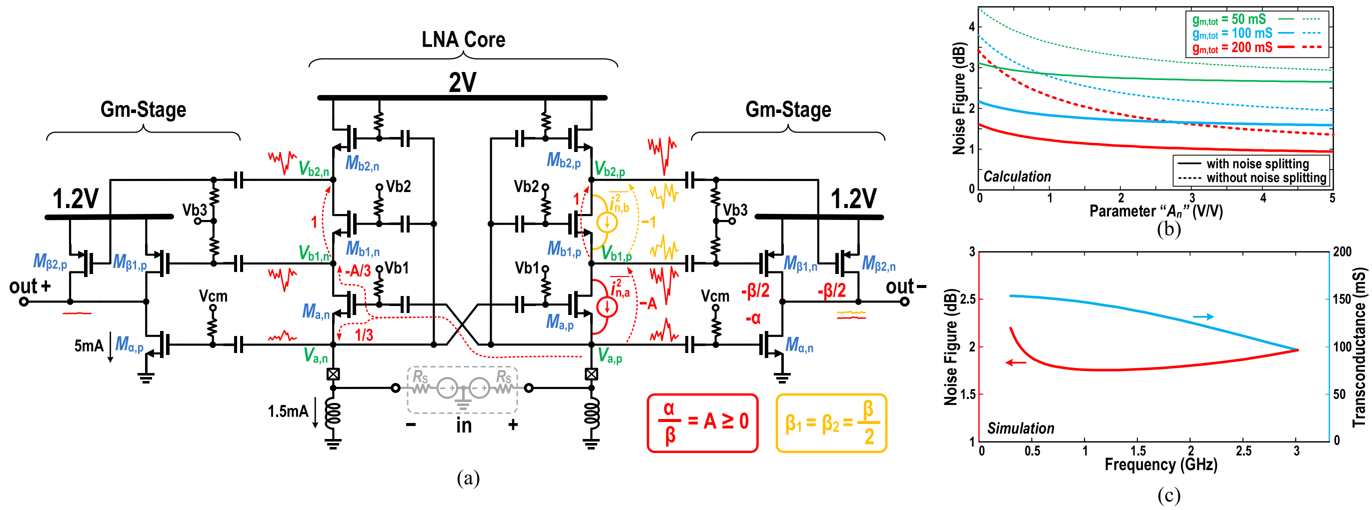


Fig. 14. (a) Wideband noise canceling LNTA. Noise cancellation mechanisms of M_a and M_{b1} are shown in red and yellow, respectively. (b) Calculated LNTA NF versus A parameter and (c) simulated NF and total g_m versus frequency, with $S_{11} < -10$ across the range. Note that LNA core gain is $A + 2$.

E. Selection of IF Frequency

Based on (9), if the ratio of $f_{s,BB}/f_{\mathrm{IF}}$ is fixed, changing IF would not have any major impact on the BB IMRR. To increase this rejection, $f_{s,BB}$ would have to go up independently. In the case of ADCs terminating the IF chain, it implies a higher ADC sample rate. On the other hand, if a fixed ratio is considered, lowering f_{IF} results in a narrower BPF bandwidth, and hence, higher linearity (IIP2 and IIP3) at a fixed offset frequency. However, f_{IF} should be always higher than the IM2 product and the flicker noise corner.

In this paper, for the sake of simplicity, a sliding IF approach with $f_{\mathrm{IF}} = f_{\mathrm{LO}}/16$ is used. With $f_{s,BB} = 4f_{\mathrm{IF}}$ used in our analog BB implementation, theoretical BB IMRRs could reach 59 and 63 dB for the images at $f_{\mathrm{RF}} + f_{s,BB}$ and $f_{\mathrm{RF}} - f_{s,BB}$, respectively. In transistor-level simulations, 46- and 51-dB rejections are obtained. The shortfall is due to lowering of the quality factor of BPFs by the output resistance of IF gm-cells.

V. Low-Noise Transconductance Amplifier

To be able to amplify the RF signal located at any of the supported frequency bands, wideband noise canceling LNA [35] appears to be a good choice. As the proposed RX is based on sampling the input charge, the RF amplifier needs to provide current rather than voltage, thus acting as a TA exhibiting a high output impedance. Core of the proposed LNTA in Fig. 14(a) is a combination of cross-coupled common-gate LNA [36] and common-gate-source-follower noise-canceling structure in [37]. The gm-stage is devised to produce the output current by adding three interstage in-phase signals generated by the LNA core. As will be shown in the following, by properly sizing the output transistors, noises of M_a and M_{b1} transistor pairs are completely canceled out (via a twofold cancellation) and noise contribution of M_{b2} is significantly reduced.

The input transistor pair, M_a, provides the input matching. Thanks to cross coupling of their gates to the differential input, input impedance (R_S) matching is achieved with half the input g_m,[3] $g_{m,a} = 1/(2R_S)$. Considering the noise of $M_{a,p}$ [indicated in red in Fig. 14(a)], we can show that it appears on $V_{a,p}$ as

$$\overline{V_{a,p}^2} = (3/4R_S)^2\overline{i_{n,a}^2} \tag{10}$$

where $\overline{i_{n,a}^2}$ is a spectral density of the $M_{a,p}$ noise current. As M_{b1} and M_{b2} transistors are identical, we can show that the $M_{a,p}$ noise appears equally on the $V_{b1,p}$ and $V_{b2,p}$ nodes with $-A_n$ times $V_{a,p}$, where A_n is given by

$$A_n = \frac{1}{g_{m,b}R_S} - 1. \tag{11}$$

Normally, M_{b1-2} transconductance $g_{m,b}$ is set to ensure $A_n \geq 0$. If $g_{m,b} = 1/R_S$, A_n becomes zero and noise of $M_{a,p}$ is canceled completely on $V_{b1-2,p}$ [37]. However, in general, higher A_n increases signal gain and, consequently, reduces noise from M_{b1-2} and the gm-stage. Signal voltage gain from V_a to V_{b1} and V_{b2} is given by

$$A_v = \frac{V_b}{V_a} = \left(\frac{1}{g_{m,b}R_S} + 1\right) = 2 + A_n. \tag{12}$$

To cancel noise of $M_{a,p}$ transistor for an arbitrary A_n value, we propose to exploit the available degree-of-freedom in the gm-stage, where signals from $V_{a,p}$ and $V_{b,p}$ ($V_{b1,p}$ and $V_{b2,p}$) to *out*- have a gain of $-g_{m,\alpha}$ and $-g_{m,\beta}$, respectively

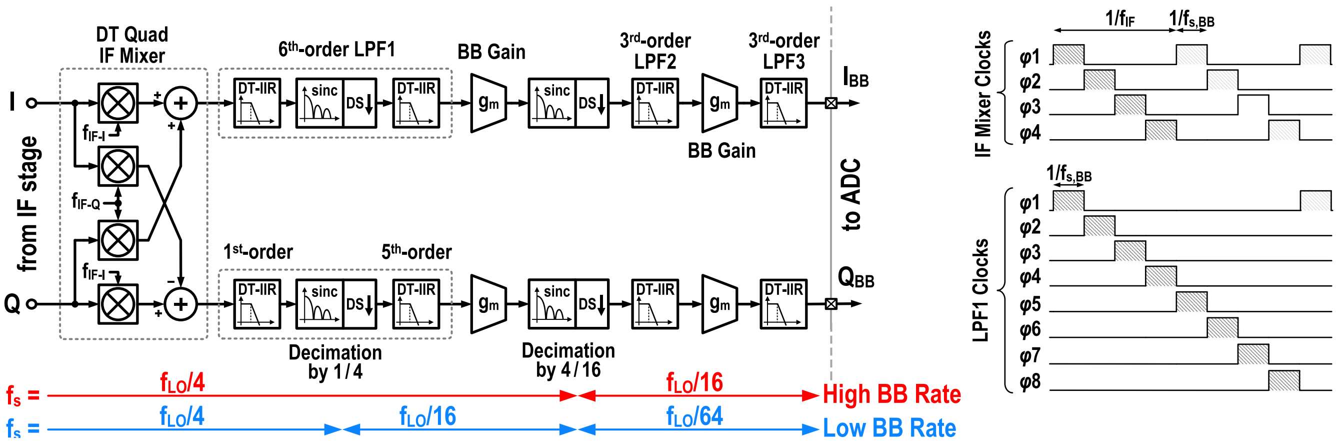
$$g_{m,\alpha} \cdot V_{a,p} + g_{m,\beta} \cdot V_{b,p} = 0. \tag{13}$$

Substituting (12) into $V_{b,p}$ in (13) gives the condition that the noise of $M_{a,p}$ does not appear at the output

$$g_{m,\alpha} \cdot V_{a,p} + g_{m,\beta}(-A_n \cdot V_{a,p}) = 0 \Rightarrow \frac{g_{m,\alpha}}{g_{m,\beta}} = A_n. \tag{14}$$

In addition to canceling the noise of M_a, noise of M_{b1} is also canceled at the output. Instead of using only one M_b on each side of the LNA core, as in [37], two identical transistors M_{b1} and M_{b2} are stacked in our proposed scheme. Although

[3] In the LNTA analysis, MOS output resistance is neglected for simplicity.



(a) (b)

Fig. 15. (a) BB DT signal processing of the RX. (b) Required clock waveforms for the IF mixer and LPF1.

the amplified input signal appears in-phase, noise of $M_{b1,p}$ [$\overline{i_{n,a}^2}$ shown yellow in Fig. 14(a)] appears antiphase between $V_{b1,p}$ and $V_{b1,n}$. Then, splitting $M_{\beta,n}$ into two half transistors ($M_{\beta1,n}$ and $M_{\beta2,n}$) cancels noise of $M_{b1,p}$ at the output (the proposed noise splitting technique). This way, only noise of $M_{b2,p}$ from the LNA core contributes to the output, but with a reduced gain of $g_{m,\beta}/2$, instead of $g_{m,\beta}$.

Total gain of LNTA from its input to output is provided by three paths: through V_a, V_{b1}, and V_{b2} nodes. Using (12) and (14), the total single-ended gain is derived

$$g_{m,\text{tot}} = -(g_{m,\alpha} + g_{m,\beta}(2 + A_n)) = -2g_{m,\beta}(1 + A_n). \quad (15)$$

Total NF of the LNTA is calculated by referring noise contribution of M_{b2}, M_α, and M_β from the output to the input, which is simplified to

$$\text{NF} = 1 + \frac{\gamma_b}{4(1 + A_n)} + \frac{2\gamma_{\alpha,\beta}}{g_{m,\text{tot}} R_S} \quad (16)$$

where γ is an MOS noise excess factor. The second term is due to noise of M_{b2} that is substantially reduced $4\times$ by the proposed noise splitting technique, and $1 + A_n$ times by signal gain from other paths. The third term is the total noise contribution of the gm-stage that is reduced $2\times$ by the gain provided in the LNA core. Fig. 14(b) plots NF of the LNTA with and without the noise splitting technique. In this calculation, perfect ac coupling is considered and parasitics are neglected. Simulated NF and g_m of our implementation are shown in Fig. 14(c). The parameter A_n is chosen to be about 1 (LNA core gain about $A_v = 10$ dB) in this design to have a balance between NF and IIP3 (about 0 dBm based on simulation). The covered LNTA frequency range is wideband: from 0.3 up to 3 GHz (verified through measurements). For frequencies lower than 0.4 GHz, noise of *RC* biases comes into play, thus increasing the NF. For frequencies higher than 3 GHz, parasitic capacitors reduce the gain and gradually increase NF.

VI. Baseband Signal Processing

The signal at the end of IF strip can be directly sampled and digitized using Nyquist rate or bandpass ADC [9]. Afterward, the BB signal processing, including IF mixing and channel select filtering, can be done entirely in a digital domain. However, this approach might not be the most power efficient in the chosen process technology, i.e., 65-nm CMOS, because of stringent sample rate and high dynamic range requirements imposed on the ADC. The alternative approach chosen in our implementation is to process the signal through DT analog BB, as shown in Fig. 15(a). The main goal of this BB strip is to reduce the required sample rate and dynamic range of the ADC by means of prior filtering and decimation. The proposed DT BB consumes only a few milliwatts, while significantly saving power consumption of the ADC and digital BB.

A. DT Analog Baseband Signal Processing

The first stage of the analog BB circuitry is a quadrature DT IF mixer. A set of *four* mixers downconvert the complex-valued IF signal to dc. Implementation of each mixer is similar to the passive RF mixer shown in Fig. 9. The BB sample rate ($f_{s,BB}$) is chosen $4f_{\text{IF}}$ ($=f_{\text{LO}}/4$) to simplify the generation of IF mixer clocks. As shown in Fig. 15(b), the IF clocks are similar to those in the RF mixer, but the period is $1/f_{\text{IF}}$. The IF mixer is the only circuitry in this RX that limits the overall IIP2, even though it is still a very high value. Since the IF mixer is clocked at a much lower rate than the RF mixer, its IIP2 is substantially better [38]. Moreover, the IF filtering considerably improves its IIP2 referred back at the antenna for offset frequencies higher than the bandwidth of BPFs.

The second stage of the analog BB strip is a channel-select DT sixth-order LPF (IIR6), derived from the work in [16]. Fig. 16 shows the switch-level implementation. C_{H1} at the input port accumulates the input charge. Through a prearranged switching sequence, each of the C_S capacitors rotates the partial charge of C_{H1} to other history capacitors, C_{H2-6}, and then gets reset. Each charge-sharing operation within the cycle adds one order of filtering [16]. Using eigth sampling capacitors, each with a delay of one phase, increases the filter's sampling rate $8\times$ while using the same clock signals (i.e., the parallelized operation). In the normal high sample-rate mode, "black" and "red" switches are clocked and the filter works as described. This mode is used for high bandwidth signals up to 30 MHz (e.g., for the LTE standard). For narrowband

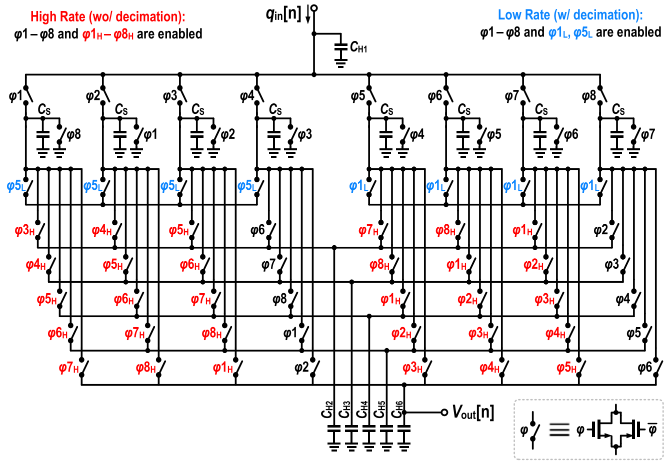


Fig. 16. Implementation of the DT sixth-order IIR LPF with selectable decimation by 4.

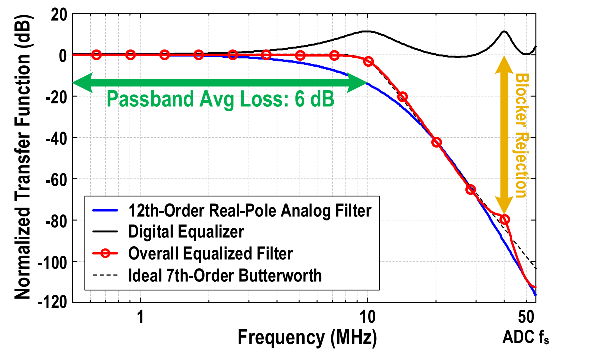


Fig. 17. Digital equalization of 12th-order real-pole TF to a seventh-order Butterworth filter. The ADC and digital equalizer are clocked at 50 MHz.

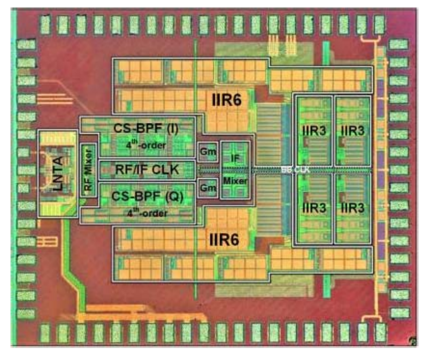


Fig. 18. Proposed RX's chip micrograph 1.9 × 2.4 mm^2.

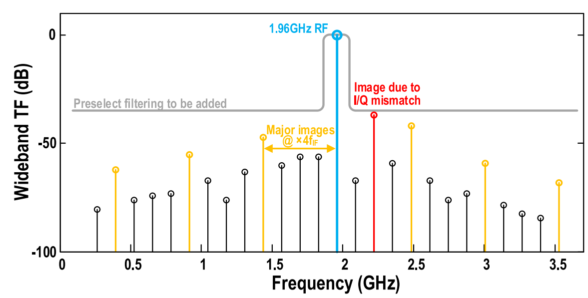


Fig. 19. Measured wideband TF of the RX for a representative 1.96-GHz expected input carrier setting.

signals (e.g., 200 kHz in GSM standard), the sample rate of $4f_{\text{IF}}$ (several hundreds of MS/s) would be excessive, so further decimation should be done to save power. In this low sampling rate mode, only "black" and "blue" switches are clocked and the "red" switches are disengaged. After a set of four succeeding C_S values are charge shared with C_{H1}, they are shorted together to make a *spatial decimation* by 4 [22]. Charge sharing of the four C_S values makes a four-tap MA as a sinc antialiasing filter prior to the subsequent decimation. Then, one of them continues charge sharing with C_{H2-6}. This also reduces the required C_H value to support the narrow bandwidth. Clock waveforms required for driving this filter are shown in Fig. 15(b).

Since the RX path up to the end of IIR6 already enjoys sample gain and filtering, noise and IIP3 of the remaining stages are less of a concern, so they can be implemented in an ultralow-power fashion. After IIR6, two extra filter stages are cascaded with two gm-cells. Fig. 13(b) shows the implementation of the gm-cells, which are constructed as fully differential inverters. Both stages of the third-order IIR LPFs ("IIR3") are identical and use similar structure as in Fig. 16, though with a lower order and without spatial decimation [16]. To further save power, their clocks are reduced by 4×. This creates a temporal decimation after the first BB gm-cell. At the bottom of Fig. 15(a), sample rate of each block, from IF to the end of BB, is displayed. Due to the high total order of filtering, ADC sample rate could be further reduced below the RX output sample rate without any other antialiasing filter.

B. Digital Equalization

Despite reaching the 12th order of DT analog filtering, only real poles are realized. A high-order real-pole filter provides a gradual and smooth transition between its passband and its sharp out-of-band roll-off (Fig. 17). Therefore, in [16], we have proposed employing a low-power digital equalizer after the ADC to map the real-pole TF to a sharp complex-pole filter, but at a reduced order. In Fig. 17, the total TF of BB filtering is mapped to a better than the seventh-order Butterworth filter. In this way, passband of the filter experiences a small average loss of ~6 dB, which can be compensated by the preceding gain stages or one additional effective number of bits (ENOB) in the ADC [16]. Considering the complete system-level view, the proposed BB processing consumes several times lower power (total I/Q BB: 2.3 mW for 1.96-GHz RF input) than the conventional CT or active switched-capacitor approaches [39], [40], while providing a much lower NF and a very high linearity [16].

VII. Measurement Results

The RX is implemented in standard TSMC 1P7M 65-nm CMOS and occupies an active area of 1.1 mm^2 (Fig. 18). It mostly consists of MOS switches, capacitors, and inverter-based gm-cells, making it process scalable and amenable to digital deep-nanoscale CMOS. Majority of the chip area is occupied by capacitors used for BB filtering that supports BB

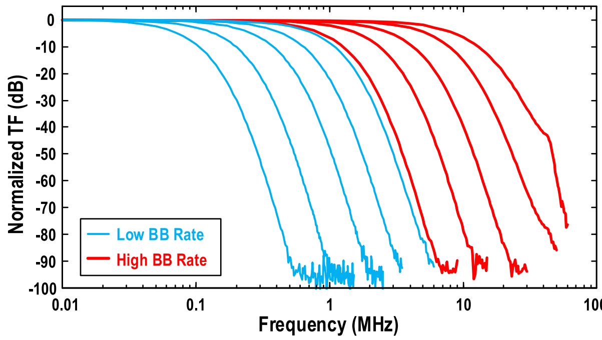


Fig. 20. Measured close-in TF of the RX.

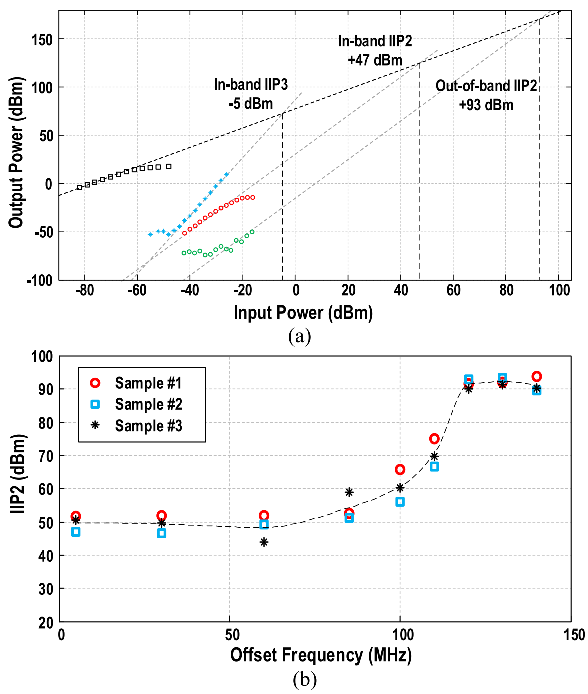


Fig. 21. (a) Measured IIP2 and IIP3 and (b) IIP2 versus offset frequency at 1900-MHz RF frequency.

cutoff frequencies down to 100 kHz. Therefore, the chip area scales very well with the CMOS technology advancements.

Measured wideband TF of the complete RX is plotted shown in Fig. 19. There are only discrete frequency points that can fold into the received band of interest. As analyzed in Section IV-D, major images (shown in yellow) are located at multiples of $4f_{\mathrm{IF}}$ away from f_{RF}. The first two major images are rejected by 42 and 46 dB, which closely agree with simulations. The reminder of images at f_{IF} multiples (in black) are much smaller, and are caused by the BB decimations. The exception is the image of 37-dB rejection (marked in red) that was traced to a systematic I/Q clock mismatch. Therefore, unaccounted parasitics on the mixer clock lines in the layout make the I/Q unbalanced. Based on simulations, a phase mismatch of about 1° could lead to the measured degraded rejection. A more careful layout design solves this in future designs (in [12], a 65-dB I/Q matching is achieved). Including an antenna preselect filter with a moderate out-of-band rejection of 40 dB, the total image rejection easily improves to better than 77 dB. Measured close-in TFs for

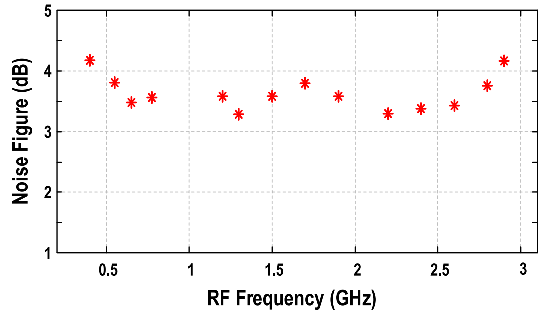


Fig. 22. Measured NF of the complete RX versus RF frequencies.

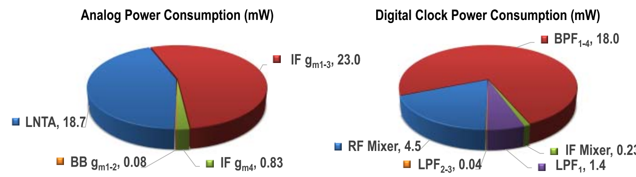


Fig. 23. Power consumption budget of various blocks at maximum gain setting for 1.96-GHz RF input.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART RXs

	This Work	[4] RFIC'13	[5] JSSC'11	[6] JSSC'10	[7] JSSC'06	[8] JSSC'14	[9] JSSC'14	[10] JSSC'09
Technology	65 nm	65 nm	65 nm	90 nm	90 nm	65 nm	28 nm	90 nm
Architecture	HIF	HIF	HIF	ZIF	ZIF	ZIF	ZIF	ZIF
Description	Full DT	DT/ N-Path	N-Path	Full DT	CT / DT	DT / CT	Full CT	Full CT
Analog BB / Order	Yes / 7 §	No	No	Yes / 2 ¶	Yes / 3 ¶	Yes / 2 ¶	Yes / 2 &	Yes / 2 &
RF Freq (GHz)	0.4–2.9	0.5–1.2	1.8–2.2	0.5–3.8	0.8–6	0.5–3	0.4–6	0.8–2.2
V_{DD} (V)	1.2 / 2	1.2	1.2 / 2.5	1.2	1.0 / 2.5	1.2 / 2.5	0.9	1.5
Power† (mW)	48–79	24.5	39	67–115	45–65	210–540#	35–40	19–23
NF (dB)	2.9–4.0	7.5	2.8	5.3–6.0	5–5.5	5.5–8.8	1.8–3.1	2.2–3.2
Max Gain (dB)	83	35	55	58 / 64	> 47	35	70	61.5
IB IIP3 (dBm)	-5	+10	-8.5	+1 / +2.5	-3.5	> -12.5	+4	N/A
OOB IIP2 (dBm) / Cal.	+93 / No	–*	–*	38–52 / No	+60 / No	> +46 / No	+80 / Yes	+90 / Yes
Channel BW‡ (MHz)	0.2–30	4.5	4	0.2–20	0.2–20	~ 26	1–100	0.2–3.8
Area (mm^2)	1.1	0.45	0.76	0.5	3.8##	1.85#	0.6	–*

† At highest gain setting
‡ Two times BB BW
* Not reported
§ 12^{th}-order real-pole mapped to a 7^{th}-order Butterworth
¶ Real-pole
& Biquad
# Synthesizer and bias are excluded
Including synthesizer

different programmed bandwidths at low/high BB rates are shown in Fig. 20. As a whole, RF bandwidth of the RX is programmable from 200 kHz to 30 MHz.

Fig. 21(a) shows the measured uncalibrated IIP2 and IIP3 at a medium gain setting with 78-dB gain. In-band IIP3 is measured −5 dBm with 1-MHz tone spacing, which is mainly limited by the linearity of IF gm-cells. While the high-IF front end has extremely high IIP2, the IF mixer limits the RX's IIP2. The IF filters in this RX attenuate blockers, and so, the out-of-band IIP2 increases rapidly at higher frequency offsets [Fig. 21(b)], from +47 dBm in-band to +93 dBm at 120-MHz offset, all *uncalibrated*. If bandwidth of the BPFs is reduced (e.g., by decreasing IF in this paper), IIP2 improvement starts at lower offset frequencies.

Plotted in Fig. 22, NF of the complete RX is between 2.9 and 4.0 dB for different bands from 0.4 to 2.9 GHz. At higher frequencies, duty cycle of φ_{1-4} RF clocks is reduced because of limited rise/fall times. Hence, the gain of RF mixer reduces, which directly degrades the RX NF.

Table I summarizes the measured RX performance and compares it with the published state of the art. The analog part consumes 43 mW in total for the high-gain setting. The clock waveform generator consumes 5–36 mW that linearly scales with f_{LO}. Fig. 23 shows the power consumption budget of different blocks. Compared with the other leading implementations in Table I, this paper demonstrates a full chain RX, including a high-order BB, with a good NF, high IIP2, and with reasonable power consumption. The RX has a maximum gain of 83 dB.

VIII. Conclusion

The complete chain of a DT superheterodyne RX with high reconfigurability is described. The full monolithic integration is made possible by the proposed DT BPF. While common handicaps of the ZIF architecture are solved, superheterodyne architecture is sensitive to quadrature accuracy of the clock signal that needs a careful design and layout. DT signal processing using passive switched-capacitor circuits makes this RX process scalable. It only uses switches, capacitors, and inverter-based gm-cells. Sampling of RF signal using $4\times$ frequency could theoretically avoid creating IF image caused by sampling. Frequency domain analysis of this RX using the proposed DT model shows that the two closest images are located at ± 4-f_{IF} offset (verified by measurement). Also, a new LNTA structure featuring twofold noise canceling is proposed and described.

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