Built-in Self-Calibration and Digital-Trim Technique for 14-Bit SAR ADCs Achieving ±1 LSB INL

Shankar Thirunakkarasu, *Member, IEEE*, and Bertan Bakkaloglu, *Senior Member, IEEE*

***Abstract*— Several state-of-the-art monitoring and control systems, such as dc motor controllers, power line monitoring and protection systems, instrumentation systems, and battery monitors, require direct digitization of high-voltage (HV) input signals. Analog-to-digital converters (ADCs) that can digitize HV signals require high linearity and low-voltage coefficient capacitors. A built-in self-calibration and digital-trim algorithm correcting static mismatches in capacitive digital-to-analog converter (DAC) used in successive approximation register analog-to-digital converters (SAR ADCs) is proposed. The algorithm uses a dynamic error correction (DEC) capacitor to cancel the static errors occurring in each capacitor of the array as the first step upon power-up and eliminates the need for an extra calibration DAC. Self-trimming is performed digitally during normal ADC operation. The algorithm is implemented on a 14-bit HV input range SAR ADC with integrated DEC capacitors. The IC is fabricated in 0.6-μm HV-compliant CMOS process, accepting up to 24V_{pp} differential input signal. The proposed approach achieves 73.32-dB signal-to-noise and distortion ratio, which is an improvement of 12.03 dB after self-calibration at 400-kS/s sampling rate, consuming 90 mW from a ±15 V supply. The calibration circuitry occupies 28% of the capacitor DAC and consumes <15 mW during operation. Measurement results show that this algorithm reduces integral nonlinearity from as high as 7 LSBs down to 1 LSB, and it works even in the presence of larger mismatches exceeding 260 LSBs. Similarly, it reduces differential nonlinearity errors from 10 LSBs down to 1 LSB. The ADC occupies an active area of 9.76 mm^2.**

***Index Terms*— Analog-to-digital (A/D) conversion, digital trimming, mismatch correction, self-calibration.**

I. Introduction

SUCCESSIVE approximation register analog-to-digital converters (SAR ADCs) are used in medium-resolution and medium-speed applications, such as motor control, battery monitoring, touch-screen control, and other sensor interfaces, requiring low latency, monotonicity, and low quiescent power consumption [1]–[6]. A high-voltage (HV) input range operation is enabled by directly sampling on the bottom plate of the capacitor array to achieve higher input impedance at a lower operating frequency specifically for industrial motor control applications [7]. In conventional high-performance and high-resolution SAR converters, the fundamental bottleneck in achieving lower integral and differential nonlinearity (INL/DNL) is the mismatches found between the binary weighted capacitors in the capacitive DAC due to process mismatches [5], [6]. The HV-SAR-ADCs enable direct connection to HV inputs, minimizing the need for voltage scaling. However, in HV-SAR-ADCs, apart from the mismatches between the capacitors, linear and quadratic voltage coefficients of capacitors also dominate the INL. In addition, HV sampling switches need to maintain constant impedance over the entire input HV range in order to reduce distortion. Also, these HV devices are prone to leakage and low speed with pronounced memory effect. Finally, it takes up a huge area to facilitate higher breakdown voltages, thereby increasing parasitics. Therefore, HV-SAR-ADCs typically achieve lower linearity performance than low-voltage SAR ADCs. In this paper, a fully integrated self-calibration and digital trimming algorithm is proposed. The proposed approach does not require any physical trim capacitors on the SAR ADC and performs calibration upon power-up.

The proposed all-digital self-trim algorithm is implemented on a 14-bit SAR ADC with integrated dynamic error correction (DEC) capacitors and the results were verified on a stand-alone SAR-ADC. This paper is organized as follows. The conventional SAR-ADC calibration/trimming procedures are reviewed in Section II. Section III explains the architecture, algorithm, and implementation details of this paper. The experimental results are provided in Section IV, and finally, Section V draws the conclusion.

II. Conventional SAR-ADC Calibration/Trimming

Conventional built-in self-calibration procedures are carried out using extra physical trim capacitors, without using digital-only trimming [8]–[12], which takes additional die area. In [13], each capacitor in the main array requires an individual calibration capacitor, and calibration voltages are generated by resistive DACs, which again increases the area. Implementation in [14] involves extra switching sequences for cancelling the errors in the capacitors, reducing throughput. Another technique proposed in [15] collects 200 000 samples using two independent half-sized ADCs driving a least mean square feedback loop in order to calibrate the capacitive digital-to-analog converter (CDAC), thereby trying to achieve convergence in the calibration algorithm. This takes a lot of time in calibrating the mismatches. There are also a number of other derived techniques [16]–[19] to calibrate the mismatches

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S. Thirunakkarasu is with RF Mixed Signal Group, Broadcom Corporation, Austin, TX 78746 USA (e-mail: shankart@broadcom.com).

B. Bakkaloglu is with Ira A. Fulton School of Engineering, Arizona State University, Tempe, AZ 85287-08406 USA (e-mail: bertan@asu.edu).

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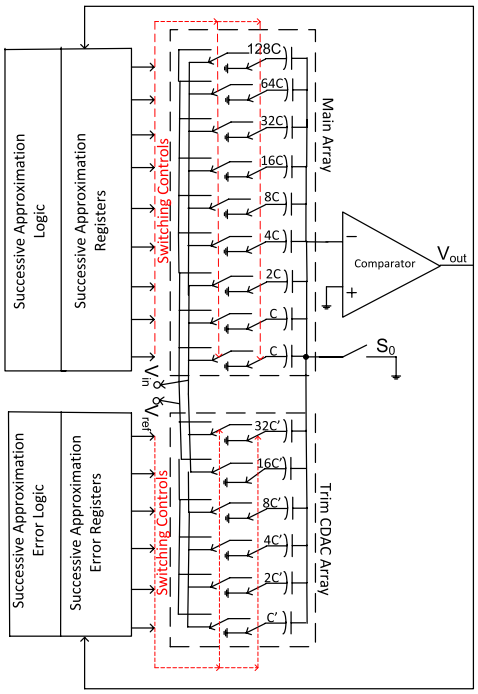

Fig. 1. Self-calibration using memory and extra trim CDAC.

in the capacitors, which either occupy extra area or extra time. In this paper, an efficient self-calibration and digital trimming algorithm is proposed, which does not take any area for implementing trim capacitors, does not reduce throughput, and takes almost negligible time in calibrating the mismatches.

An example of a traditional self-calibration and trim topology is shown in Fig. 1. Fig. 1 uses a memory for storing the errors occurring in each capacitor of the main array and corrects it through an extra error correction trim CDAC array [8]. In the case of finding the mismatch of capacitor 16C from the main array, a set of lower capacitors 8C, 4C, 2C, and C are sampled to V_{ref} while the top plate switch S_0 is grounded. This will store a known charge on the top plate node. Then, the bottom plate of capacitor 16C is tied to V_{ref}, while the top plate switch S_0 is open, and other capacitors are grounded. The exact point at which the comparator output changes sign is found by connecting bottom plates of the capacitors in the trim-CDAC array one by one to V_{ref}. This is the point at which the charge stored on the lower set of capacitors 8C, 4C, 2C, C, and C gets neutralized by the charge stored on mismatched capacitor 16C together with the trim-CDAC array, achieving binary relationship. Once the error corresponding to capacitor 16C is stored in the memory, the errors of other higher capacitances 32C, 64C, and 128C are stored accordingly. After this calibration mode, during normal A/D conversion process, whenever the MSB capacitors 16C, 32C, 64C, and 128C toggle from Gnd to V_{ref}, the trim capacitors associated with each of these capacitors, which are calculated as described earlier, are also toggled from Gnd to V_{ref} using trim-CDAC array to maintain the binary relationship between the capacitors. In this technique, the calibration and trimming are performed using physical trim capacitors from the trim CDAC array.

In another traditional technique [11], [12], multiple trim capacitors were used for each individual primary capacitor in the array. In this approach, errors associated with each primary capacitor are measured and calculated during the final test, and the error calibration codes are stored to program the trim capacitors during normal operation.

III. Proposed Self-Calibration and Digital-Trim Algorithm

The algorithm is implemented with the help of DEC capacitors explained in Section III-A. Section III-B introduces the actual self-calibration. A novel method to cancel out the charge injection-based offset error due to hold switch is explained in Section III-C. Section III-D introduces two different methods of digital trimming algorithm.

A. Dynamic Error Correction

DEC helps in achieving redundancy during SAR ADC operation. There are different techniques to achieve redundancy, as explained in [20]–[24]. Among them, [22] and [23] use nonbinary capacitor array implementation that is not effective in a monolithic implementation with different capacitor dimensions, which is difficult to implement and will not match properly. A general architecture for the proposed 14-bit CDAC with DEC is shown in Fig. 2. There are two extra capacitors next to normal bit-6 capacitor, which are called $b_{6\text{down-p}}$ and $b_{6\text{up-p}}$ on the P-side and $b_{6\text{down-n}}$ and $b_{6\text{up-n}}$ on the N-side. These two capacitors on both P-side and N-side are employed for differential DEC purposes, and it has the same value as normal bit-6 capacitor (256 LSBs). Similarly, there are two extra capacitors next to normal bit-12 capacitor, which are called $b_{12\text{down-p}}$ and $b_{12\text{up-p}}$ on the P-side and $b_{12\text{down-n}}$ and $b_{12\text{up-n}}$ on the N-side. These two capacitors on both P-side and N-side are employed for differential DEC purpose, and it has the same value as normal bit-12 capacitor (4 LSBs). Similarly, there is one extra capacitor next to normal bit-14 capacitor, which is called $b_{14\text{up}}$. This capacitor on both P-side and N-side is employed for single-ended DEC purpose, and it has twice the value as normal bit-14 capacitor (2 LSBs).

The ideal values of the capacitors for a 14-bit converter configuration are shown below. Differential DEC at bit-6 and bit-12 and a single-ended DEC at bit-14 capacitor values are underlined.

P-side caps = [8192 4096 2048 1024 512 256 <u>256</u> <u>256</u> 128 64 32 16 8 4 <u>4</u> <u>4</u> 2 1 <u>2</u> 0.5 0.25 0.25].

N-side caps = [8192 4096 2048 1024 512 256 <u>256</u> <u>256</u> 128 64 32 16 8 4 <u>4</u> <u>4</u> 2 1 <u>2</u> 0.5 0.25 0.25].

Fig. 2 exactly shows the position of switches during sampling phase. In the sampling phase, top plates of all the capacitors in the MSB array on both CDACs are grounded. Bottom plates of certain capacitors on both P-side CDAC and N-side CDAC sample V_{inp} and V_{inn}, respectively. The number of capacitors used for sampling is dependent on the following gain equation stated in (1). This also decides the gain of the ADC [25]. Typically, the inputs are sampled on

$$C_{\text{samp}} = \frac{V_{\text{ref}} \,.\, C_T}{V_{\text{inp}} - V_{\text{inn}}} \tag{1}$$

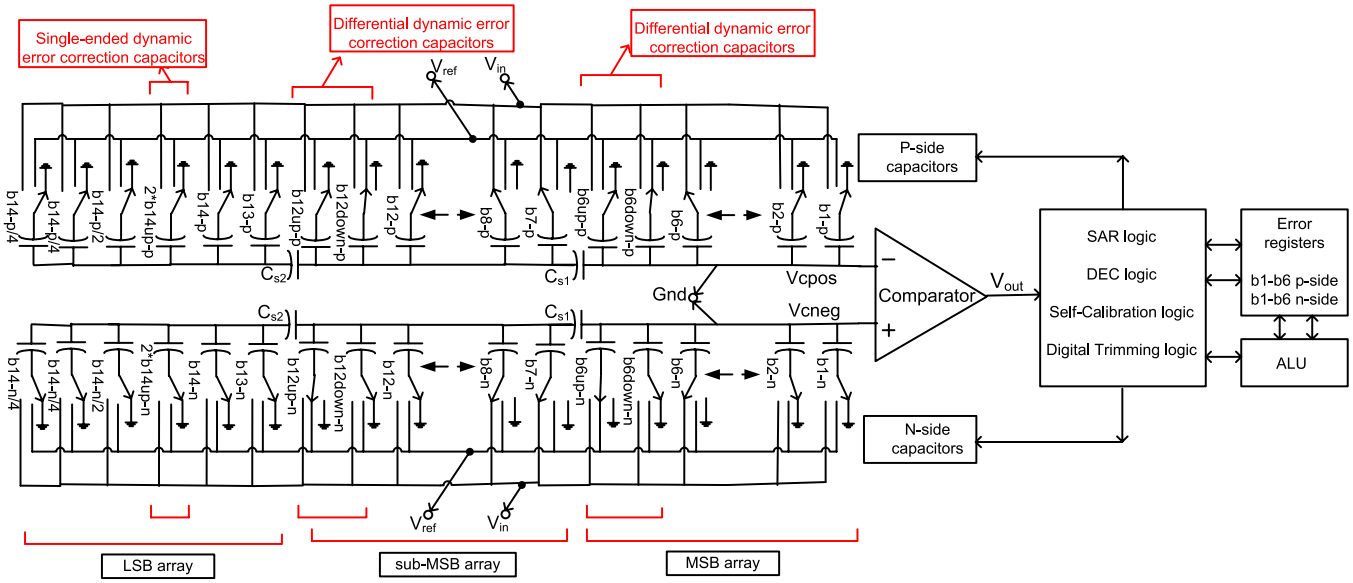

Fig. 2. Differential CDAC SAR A/D architecture utilizing the proposed self-calibration method in the sampling phase.

where C_{samp} is the total sampling capacitance and C_{T} is the sum of all capacitances on either P-side or N-side.

In the case of differential error correction on bit-6 and bit-12, one of the error correction capacitors is sampling Gnd and the other one is sampling V_{ref}. As shown in Fig. 2, $b_{6\text{down-p}}$ and $b_{6\text{up-n}}$ sample V_{ref}, and $b_{6\text{up-p}}$ and $b_{6\text{down-n}}$ sample Gnd, respectively. Similarly, in the bit-12 error correction capacitors, $b_{12\text{down-p}}$ and $b_{12\text{up-n}}$ are sampling V_{ref} and $b_{12\text{up-p}}$ and $b_{12\text{down-n}}$ are sampling Gnd, respectively. In the case of single-ended error correction on bit-14, the bottom plate of this error correction capacitor $2 \times b_{14\text{up}}$ is sampling the Gnd.

Once the input is sampled, the top plate of the capacitors in the MSB array is disconnected from Gnd. The inputs are then disconnected from the bottom plates, and a typical differential SAR conversion process is performed. During conversion, the main aim is to achieve voltage convergence between V_{cpos} and V_{cneg}, which are the two inputs of the comparator. The difference or the residue between V_{cpos} and V_{cneg} should be less than 1 LSB at the end of conversion to achieve a valid 14-bit ADC output.

Also, during multiple clock cycles in a conversion phase, V_{cpos} and V_{cneg} could attain any voltage value depending on the input voltage V_{in} equivalent to sampled V_{inp}–V_{inn}. At any given clock cycle of a conversion process, the maximum difference between V_{cpos} and V_{cneg} should be less than or equal to two times of its corresponding bit-test weight, i.e., assume that at the end of sixth clock cycle in which bit-6 capacitor is tested, the difference of voltages between V_{cpos} and V_{cneg} should be less than or equal to two times b_6 weight as stated in (2) as long as the input is within the specified range

$$V_{\text{cpos}} - V_{\text{cneg}} <= 2 . \frac{b_6}{C_{\text{T}}} . V_{\text{ref}}. \tag{2}$$

This condition is checked using either differential or single-ended DEC capacitors, and it ensures that, at the end of conversion process, V_{cpos} and V_{cneg} would converge to less than 1 LSB. If this condition is met, dynamic error does not occur and all the MSB capacitors are completely settled during the conversion process. And if this condition is not met, it means that dynamic error exists and the MSB capacitors are not settled. The DEC capacitors add or subtract voltages to V_{cpos} and V_{cneg} to achieve convergence within 1 LSB. This is later accounted for digitally in a DEC process.

Figs. 3 and 4 explain the differential DEC in detail, specifically with respect to differential DEC capacitors placed between b_6 and b_7 capacitors above the scale-down capacitor. The same explanation is valid for operation of differential DEC capacitors placed between b_{12} and b_{13} capacitors, and the same concept is true for single-ended DEC capacitor placed after b_{14}. The value of the differential DEC capacitor is equal to that of the normal b_6 capacitor. In Fig. 3(a), it is assumed that V_{cneg} is greater than V_{cpos} during b_5 testing. During b_6 testing, $b_{6\text{-p}}$ capacitor on the P-side is brought up from Gnd to V_{ref}, while the $b_{5\text{-n}}$ capacitor on the N-side is brought down from V_{ref} to Gnd and $b_{6\text{-n}}$ capacitor is brought up from Gnd to V_{ref}. Equivalently, there is an addition of b_6 weight on the P-side in V_{cpos} node while there is a subtraction of b_6 weight on the N-side in V_{cneg} node.

Since V_{cneg} is greater than V_{cpos} during b_6 testing, DEC needs to be performed by increasing the weight of V_{cpos} to another b_6 weight by switching the bottom plate of $b_{6\text{up-p}}$ on the P-side from Gnd to V_{ref} and decreasing the weight of V_{cneg} to the same amount by switching the bottom plate of $b_{6\text{up-n}}$ from V_{ref} to Gnd. If the signs change, then this means that V_{cpos} was closer to V_{cneg} by less than two times the corresponding b_6 weight at the end of normal b_6 testing. By ensuring this, V_{cpos} and V_{cneg} would converge to less than 1 LSB at the end of conversion. In this case, the differential DEC capacitors could be switched back to their original default position before going ahead with b_7 testing and so on, as shown in Fig. 3(a).

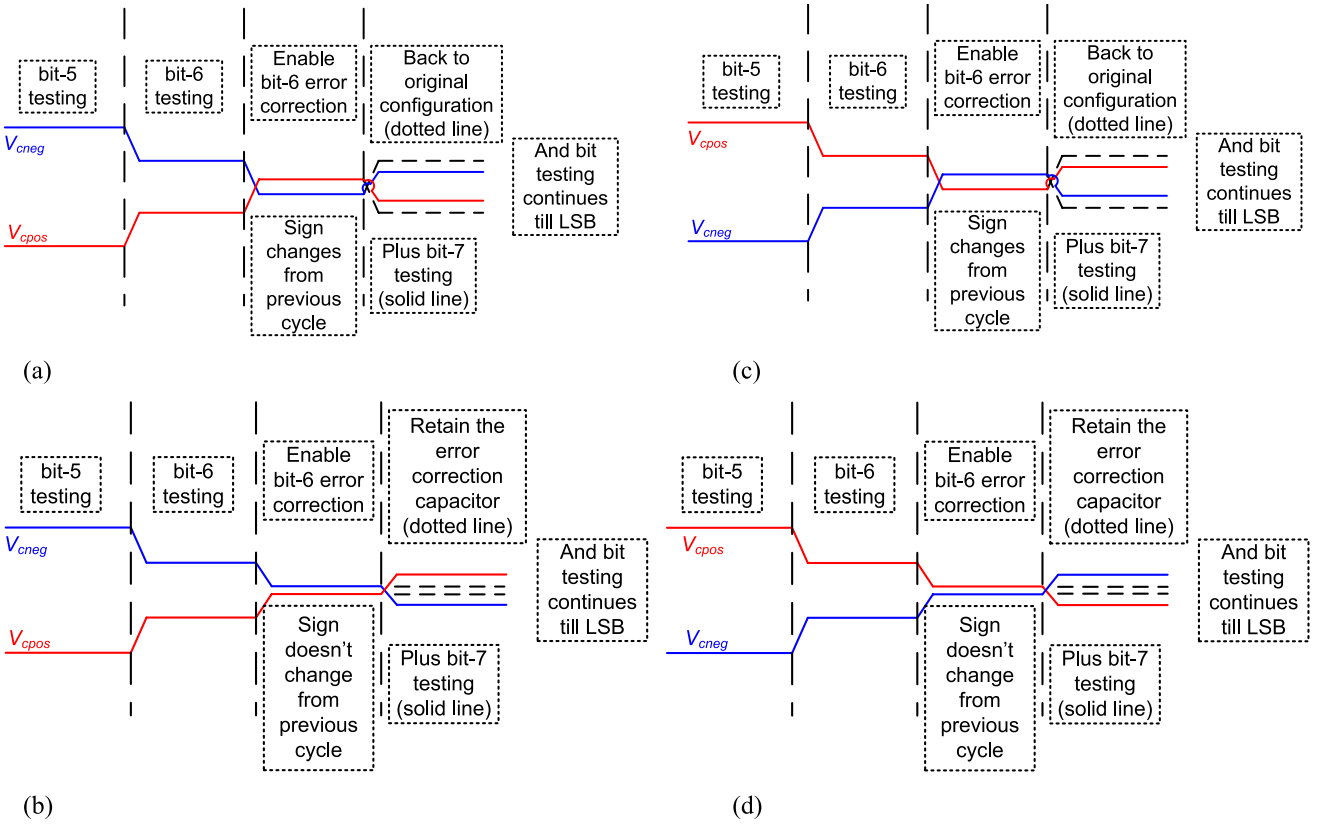

Fig. 3. Conceptual diagram—differential DEC operation. (a) Up-transition check. Sign changes during error correction testing, and no digital correction is needed. (b) Up-transition check. Sign does not change during error correction testing. Digital subtraction equivalent to b_6 weight is needed at the end of conversion. (c) Down-transition check. Sign changes during error correction testing and no digital correction needed. (d) Down-transition check. Sign does not change during error correction testing. Digital subtraction equivalent to b_6 weight is needed at the end of conversion.

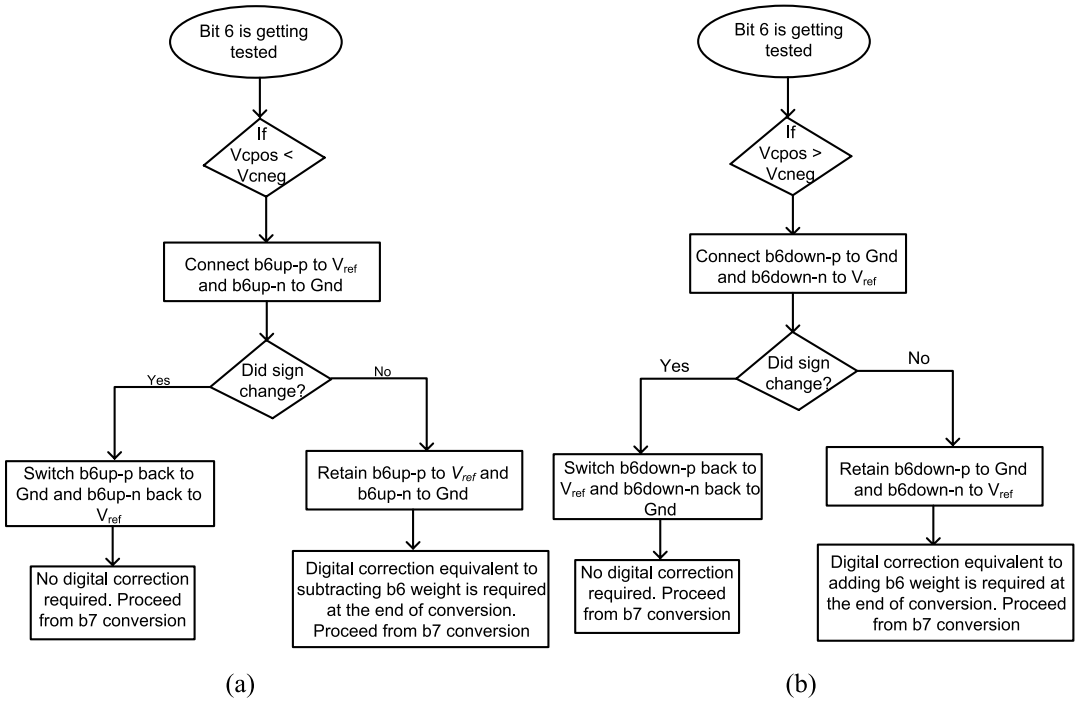

Fig. 4. Flowchart for differential DEC up-transition and down-transition. (a) Flowchart when *V*cpos is less than *V*cneg. (b) Flowchart when *V*cpos is greater than *V*cneg.

Otherwise, as shown in Fig. 3(b), if the sign does not change during b_6 error correction cycle, then it means that V_{cpos} was away from V_{cneg} by more than two times the corresponding b_6 weight at the end of normal b_6 testing. This shows that the MSB capacitors have not settled causing dynamic errors. Therefore, there is a possibility that V_{cpos} and V_{cneg} would not

converge to less than 1 LSB at the end of SAR conversion. In this case, differential DEC capacitors are retained in the same way as they were switched during error correction cycle till the end of SAR conversion. The amount of charge added by the differential DEC capacitors in analog domain is equivalently subtracted in digital domain. This helps in achieving ease of convergence between V_{cpos} and V_{cneg}. This also helps in bit cycling the SAR capacitors at the pretty fast rate achieving higher speed in high precision converters.

Fig. 4(a) shows a flowchart of the above mentioned procedure in the case of up-transition where the V_{cpos} is less than V_{cneg} during the start of b_6 error correction cycle.

Similarly, Fig. 3(c) and (d) shows the node voltages of V_{cpos} and V_{cneg} during b_5, b_6, and b_6 error correction cycle for the case in which V_{cpos} is greater than V_{cneg} at the end of b_6 testing. Therefore, we need to check dynamic errors for down-transition in this case. Also, Fig. 4(b) shows the flowchart of this procedure to check for DEC.

B. Built-in Self-Calibration Algorithm

The architecture for the proposed built-in self-calibration algorithm is shown in Fig. 2. In this segmented, differential CDAC architecture, it is assumed that the first scale-down capacitor is placed between b_6 and b_7 capacitors and the second scale-down capacitor is placed between b_{12} and b_{13} capacitors. The first and second scale-down capacitors separate the MSB array from the sub-MSB array and LSB array, respectively. The scale-down capacitor provides the capacitive division between the MSB array and sub-MSB array. Because of this capacitive division, the scale-down capacitor decreases the sensitivity of mismatch between the capacitors in sub-MSB and LSB arrays. Therefore, only the MSB array is trimmed. Also, the variation in the parasitic capacitor on the bottom plate of the first scale-down capacitor causes an intrinsic mismatch between the MSB and the sub-MSB arrays. This mismatch needs to be corrected either by trimming the first scale-down capacitor or equivalently each of the MSB capacitors from b_1 to b_6. Trimming of the scale-down capacitor C_{s1} may require laser trimming techniques or more analog switches tied to the floating nodes, which leads to extended test time, cost, and complexity. Also, trimming b_1–b_6 individual capacitors can be achieved by additional analog circuits as discussed in Section II. In the proposed technique, a purely digital trimming approach completely eliminating the trim capacitors, is followed without using input voltage V_{in}, where the errors in each capacitor from b_1 to b_6 can be found using self-calibration technique. The proposed method can correct for mismatches within an array and also between the P-side and N-side arrays in a fully differential CDAC since the errors will be found independently on both sides. In this built-in self-calibration approach, the capacitor errors are found by first sampling $b_{6\text{down}}$ capacitor on the P-side ($b_{6\text{down-p}}$) to V_{ref} and then performing differential conversion from b_7. The error of $b_{6\text{down-p}}$ is obtained by subtracting the ideal expected value from this conversion result. The error obtained on $b_{6\text{down-p}}$ will be half the value of the original error because of the single-ended sampling (P-side alone) on a single capacitor. In contrast to the traditional easier techniques using physical trim capacitors in which single-ended sampling and single-ended conversion are performed [8], [11] or differential sampling and differential conversion are performed [8], [11], this technique eliminates physical trim capacitors and adopts the single-ended sampling independently on both P-side and N-side with differential conversion to account for the mismatches occurring in the bit capacitances between the P-side and N-side arrays. In addition, this technique also corrects the mismatches found between the binarily weighted capacitors within any array.

Similarly, the errors of $b_{6\text{up-p}}$ and $b_{6\text{-p}}$ capacitors are found by sampling the respective capacitors followed by performing differential conversion from b_7 and then subtracting from its ideal value. In the same way, the errors on $b_{5\text{-p}}, b_{4\text{-p}}, \ldots, b_{1\text{-p}}$ capacitors are also found by sampling each one of them separately and then performing differential conversion from $b_6, b_5, \ldots, b_2$, respectively, with dynamic correction employed at b_6, b_{12}, and b_{14} positions followed by subtraction from its ideal expected values.

The DEC is employed in [20] and [24] to reduce the settling errors during MSB cycles while the ADC is converting at full speed. In the proposed architecture, the DEC is also employed during self-calibration at bit positions b_6, b_{12}, and b_{14} while measuring the errors of b_5, $b_4, \ldots, b_1$ so that even if each of these MSB capacitors are mismatched by a large margin, up to the order of ± 261 LSBs ($b_6 + b_{12} + b_{14}$), the error transfer function would still result in less than 1 LSB. In this way, the DEC capacitors are also used for calculating static mismatches in this algorithm. Using a similar procedure, the errors are calculated on P-side and N-side capacitors independently. Let the errors of capacitors $b_{1\text{-p}}, b_{2\text{-p}}, \ldots, b_{6\text{-p}}, b_{6\text{up-p}}, b_{6\text{down-p}}, b_{1\text{-n}}, b_{2\text{-n}}, \ldots, b_{6\text{-n}}$, $b_{6\text{up-n}}$, and $b_{6\text{down-n}}$ obtained in this step be $\varepsilon_{1\text{-p}}, \varepsilon_{2\text{-p}}, \ldots, \varepsilon_{6\text{-p}}, \varepsilon_{6\text{up-p}}, \varepsilon_{6\text{down-p}}, \varepsilon_{1\text{-n}}, \varepsilon_{2\text{-n}}, \ldots, \varepsilon_{6\text{-n}}, \varepsilon_{6\text{up}-\text{n}}$, and $\varepsilon_{6\text{down-n}}$.

The values of $\varepsilon_{6\text{-p}}, \varepsilon_{6\text{up-p}}, \varepsilon_{6\text{down-p}}, \varepsilon_{6\text{-n}}, \varepsilon_{6\text{up}-\text{n}}$, and $\varepsilon_{6\text{down-n}}$ obtained in the previous self-calibration step are not modified. But, the errors associated with other capacitors are modified depending on how the correction capacitors are used while doing conversion in the self-calibration phase. The modifications that the capacitors on the P-side and N-side go through while calculating $\varepsilon_{5\text{-p}}$ to $\varepsilon_{1\text{-p}}$, $\varepsilon_{5\text{-n}}$ to $\varepsilon_{1\text{-n}}$ is shown in Fig. 5. Fig. 5 is similar to Fig. 4(a) and (b) except that it is explained with context to self-calibration rather than pure DEC. For example, during self-calibration, while finding the error associated with $b_{5\text{-p}}$, after initially sampling $b_{5\text{-p}}$ alone to V_{ref}, V_{cpos} in Fig. 2 would be less than V_{cneg}. Therefore, DEC needs to be performed by switching $b_{6\text{up-p}}$ to V_{ref} and $b_{6\text{up-n}}$ to Gnd, as shown in the flowchart in Fig. 5. The steps in the flowchart should be exactly followed while calculating $\varepsilon_{5\text{-p}}$. Similarly, the errors associated with $b_{4\text{-p}}, b_{3\text{-p}}, \ldots, b_{1\text{-p}}$ are also calculated based on the flowchart shown in Fig. 5. In the same way, the errors associated with $b_{5\text{-n}}, b_{4\text{-n}}, \ldots, b_{1\text{-n}}$ are also calculated. In the previous step, it could be seen that the errors calculated on the $b_{5\text{-p}}$ is correct only based on the assumption that b_6 capacitors are all perfect. However, there can be a mismatch on the b_6 capacitors, which needs to be considered. Similarly, while calculating the errors associated

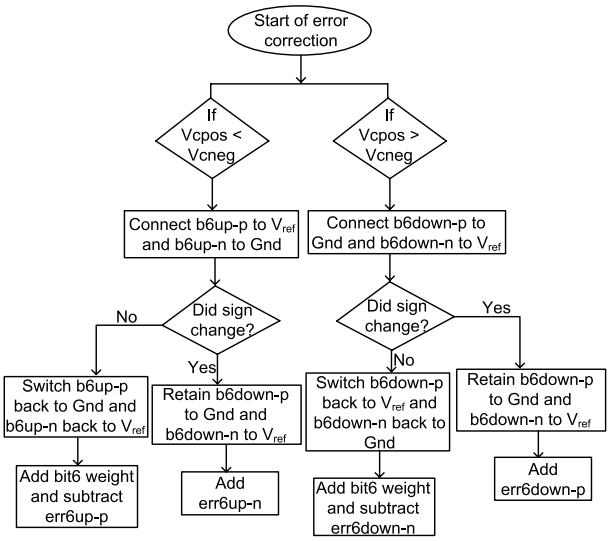

Fig. 5. Differential DEC flowchart for up- and down-transition.

with $b_{4\text{-p}}$, $b_{3\text{-p}}, \ldots, b_{1\text{-p}}$, it is assumed that all the lower capacitors are all accurate. But then in real scenario, the lower capacitors would also be mismatched. In order to compensate for this, a compensation factor needs to be added as follows. The final value of $\varepsilon_{5\text{-p}}$ is obtained by adding the previous $\varepsilon_{5\text{-p}}$ with the $\varepsilon_{6\text{-p}}$ and $\varepsilon_{6\text{down-p}}$ as shown in (3) assuming that $b_{6\text{down-p}}$ is always connected to V_{ref} during sampling and also during initial conversion till b_6 capacitor

$$\varepsilon_{5\text{-p}}(\text{final}) = \varepsilon_{5\text{-p}}(\text{previous}) + \varepsilon_{6\text{-p}} + \varepsilon_{6\text{down-p}}. \tag{3}$$

Similarly, final value of $\varepsilon_{4\text{-p}}$ is obtained by adding the previous $\varepsilon_{4\text{-p}}$ with $\varepsilon_{5\text{-p}}$, $\varepsilon_{6-\text{p}}$, and $\varepsilon_{6\text{down}-\text{p}}$, as shown in (4). The final value of $\varepsilon_{3\text{-p}}$ to $\varepsilon_{1\text{-p}}$ is computed in the same manner

$$\varepsilon_{4\text{-p}}(\text{final}) = \varepsilon_{4\text{-p}}(\text{previous}) + \varepsilon_{5\text{-p}}(\text{previous}) + \varepsilon_{6\text{-p}} + \varepsilon_{6\text{down-p}}. \tag{4}$$

For the case of $\varepsilon_{5\text{-n}}$, its final value is computed by adding the previous value of $\varepsilon_{5\text{-n}}$ with $\varepsilon_{6\text{-n}}$ and $\varepsilon_{6\text{up-n}}$ assuming $b_{6\text{up-n}}$ is initially connected to V_{ref} during sampling, as shown in Fig. 2, and also during initial conversion until differential DEC testing

$$\varepsilon_{5\text{-n}}(\text{final}) = \varepsilon_{5\text{-n}}(\text{previous}) + \varepsilon_{6\text{-n}} + \varepsilon_{6\text{up-n}}. \tag{5}$$

The final value of $\varepsilon_{4\text{-n}}$ to $\varepsilon_{1\text{-n}}$ is found using the same method

$$\varepsilon_{4\text{-n}}(\text{final}) = \varepsilon_{4\text{-n}}(\text{previous}) + \varepsilon_{5\text{-n}}(\text{previous}) + \varepsilon_{6\text{-n}} + \varepsilon_{6\text{up-n}}. \tag{6}$$

By doing so, an estimate of the errors occurring on the capacitors of both P- and N-side from b_1 to b_6 is known during this self-calibration step. Once the estimate of errors is known for each capacitor above the scale-down during self-calibration step, it is stored in local registers.

C. Charge Injection-Based Offset Error in Self-Calibration

During self-calibration, when each capacitor is individually calibrated from $b_{6\text{down-p}}$, $b_{6\text{up-p}}$, $b_{6\text{-p}}, \ldots, b_{1\text{-p}}$ on the P-side and from $b_{6\text{down-n}}, \ldots, b_{6\text{up-n}}$, $b_{6\text{-n}}, \ldots, b_{1\text{-n}}$ on the N-side, errors occur due to charge injection of the hold switch. The amount of charge injection will be based on the impedance looking into the top plate of the calibrating capacitor, which is different for different calibrating capacitor. For example, as shown in Fig. 2, at the end of sampling phase in a self-calibration algorithm, when the hold switch opens, charge injection from the hold switch is different when $b_{6\text{down-p}}$ is sampled to V_{ref} than when $b_{1\text{-p}}$ is sampled. This creates offset error between different capacitors and may provide false correction value during calibration. So, there should be a charge injection-based offset cancellation that needs to be performed for different capacitors while it is being calibrated.

This is usually done after self-calibration algorithm is completed. To cancel the offset provided by the charge injection of the hold switch during $b_{6\text{down-p}}$ sampling phase, $b_{6\text{down-p}}$ is sampled to V_{ref} on the bottom plate while the top plate is grounded. In the hold phase, top plate hold switch is opened, while the bottom of $b_{6\text{down-p}}$ is still connected to V_{ref}. Next differential conversion is performed from b_7 to calculate the offset due to charge injection of hold switch during $b_{6\text{down-p}}$ calibration. Similarly, offset due to charge injection of hold switch for different capacitors is found independently and stored. These values are subtracted from the errors of different capacitors found in self-calibration algorithm to calculate the exact mismatches in each capacitor.

D. Digital Trimming

In the proposed digital-trimming process, during normal ADC conversion process, whenever the MSB capacitors from $b_{1\text{-p}}$ to $b_{5\text{-p}}$ is decided to be connected from Gnd to V_{ref} on the positive side, the sum of the respective errors computed for those bits on both positive and negative sides need to be added to the final digital output with mismatched physical capacitance. Also, whenever a b_6 weight is subtracted, the $\varepsilon_{6\text{down-p}}$ and $\varepsilon_{6\text{down-n}}$ are also subtracted. In the same way, whenever a b_6 weight is added, the $\varepsilon_{6\text{up-p}}$ and $\varepsilon_{6\text{up-n}}$ are also added. Implementing all the steps as stated earlier would ensure that the final error plot to be within ± 1 LSB.

Alternatively for digital trimming process, during normal ADC conversion, it would also make sense to add the errors found on the positive side alone whenever the decision is taken for those MSB bits to be connected to V_{ref} and the errors found on the negative side could be subtracted when the corresponding MSB capacitor on the positive side is decided to be connected to Gnd. Both the options for digital trimming process would function similarly and it could be proved mathematically as follows. Let the reference voltage used in the circuit be V_{ref} and let $\Sigma C_{\text{high},P}$ denote the summation of all capacitors tied high on the P-side at the end of conversion, $\Sigma C_{\text{high},N}$ denotes the summation of capacitors tied high on the N-side. If $C_{\text{total},P}$ and $C_{\text{total},N}$ denote the sum of all capacitors tied both high and low, respectively, then (7) is valid at the end of conversion. If we assume that $\Sigma d\text{N}_{\text{high}}$, $\Sigma d\text{N}_{\text{low}}$, $\Sigma d\text{P}_{\text{high}}$, and $\Sigma d\text{P}_{\text{low}}$ denote the delta errors due to

mismatches occurred on the capacitors of N-side tied high, low and on P-side tied high, low, respectively, at the end of conversion, then (8) is valid

$$\frac{V_{\text{ref}} \cdot \sum C_{\text{high},N}}{C_{\text{total},N}} = \frac{V_{\text{ref}} \cdot \sum C_{\text{high},P} - C_{\text{total},P} \cdot V_{in}}{C_{\text{total},P}} \tag{7}$$

$$\frac{V_{\text{ref}}.(\sum C_{\text{high},N} + \sum dN_{\text{high}})}{C_{\text{total},N}} = \frac{V_{\text{ref}}.(\sum C_{\text{high},P} + \sum dP_{\text{high}}) - C_{\text{total},P}.V_{in}}{C_{\text{total},P}}. \tag{8}$$

The relationship that describes the complementary nature of $\Sigma C_{\text{high},P}$ and $\Sigma C_{\text{high},N}$ is given by

$$\frac{\sum C_{\text{high},N}}{C_{\text{total},N}} = 1 - \frac{\sum C_{\text{high},P}}{C_{\text{total},P}}. \tag{9}$$

Since the two DACs are independent in terms of their actual capacitor values, it is possible to write it in terms of ratios

$$\frac{\sum C_{\text{high}}}{C_{\text{total}}} = \frac{\text{Code}}{\text{FS}_{\text{Code}}} \tag{10}$$

where Code represents the equivalent digital output code for the capacitors tied high and FS_{Code} represents the full scale output code. Also, since both DACs have the same resolution, FS_{Code} is same for both and the compliment between the digital equivalent of capacitors tied high on the positive side Code_P and the one on the negative side Code_N is described as

$$\text{Code}_N = \text{FS}_{\text{Code}} - \text{Code}_P. \tag{11}$$

Assuming that $D_{\text{pcode,h}}$ and $D_{\text{ncode,h}}$ represents the summation of digital equivalent of errors occurred in the capacitors tied high on the positive and negative side, respectively, then

$$\frac{D_{\text{ncode},h}}{\text{FS}_{\text{Code}}} \cdot V_{\text{ref}} + \left(1 - \frac{\text{Code}_P}{\text{FS}_{\text{Code}}}\right) \cdot V_{\text{ref}} = \frac{D_{\text{pcode},h}}{\text{FS}_{\text{Code}}} \cdot V_{\text{ref}} - V_{\text{in}} + \frac{\text{Code}_P}{\text{FS}_{\text{Code}}}.V_{\text{ref}} \tag{12}$$

$$\frac{V_{\text{in}}}{V_{\text{ref}}} = \frac{2.\text{Code}_P - D_{\text{ncode},h} + D_{\text{pcode},h}}{\text{FS}_{\text{Code}}} - 1 \tag{13}$$

$$\text{Code}_P - \frac{D_{\text{ncode},h}}{2} + \frac{D_{\text{pcode},h}}{2} = \frac{\text{FS}_{\text{Code}}}{2} + V_{\text{in}}. \tag{14}$$

Here, if it is assumed that the input range is V_{in} or equivalently FS_{Code} range from $-V_{\text{ref}}$ to $+V_{\text{ref}}$, then $\text{FS}_{\text{Code}}/2$ indicates bipolar zero. Therefore, V_{in} is equal to the summation of decisions taken on the positive side minus the summation of half of the errors occurred in the capacitors tied high on the negative side plus the summation of half of the errors occurred in the capacitors tied high on the positive side. Similarly, for the alternative digital trimming procedure, reworking the above derivation by substituting

$$\frac{V_{\text{ref}}.\sum C_{\text{high},N}}{C_{\text{total},N}} = V_{\text{ref}} - \frac{V_{\text{ref}}.\sum C_{\text{low},N}}{C_{\text{total},N}} \tag{15}$$

$$V_{\text{ref}} - \frac{V_{\text{ref}}.(\sum C_{\text{low},N} + \sum dN_{\text{low}})}{C_{\text{total},N}} = V_{\text{ref}} \cdot \frac{(\sum C_{\text{high},P} + \sum dP_{\text{high}}) - C_{\text{total},P} \cdot V_{\text{in}}}{C_{\text{total},P}}. \tag{16}$$

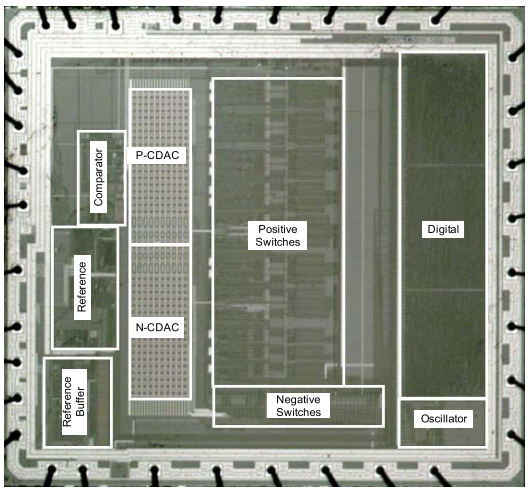

Fig. 6. Die micrograph.

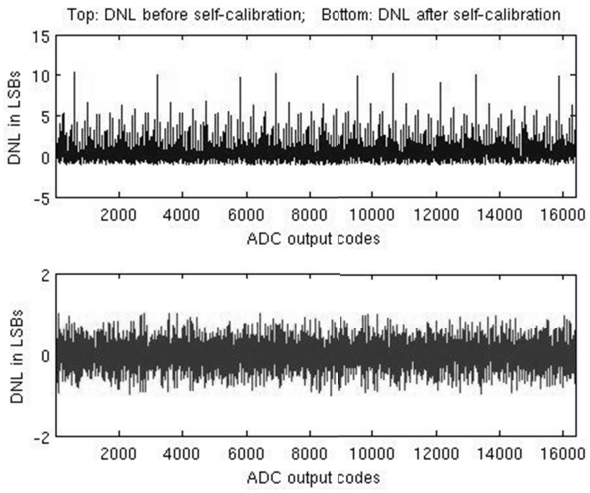

Fig. 7. DNL before and after self-calibration.

Proceeding ahead in the same way as shown above for the first case, it will turn out to be

$$\text{Code}_P + \frac{D_{\text{ncode},l}}{2} + \frac{D_{\text{pcode},h}}{2} = \frac{\text{FS}_{\text{Code}}}{2} + V_{\text{in}}. \tag{17}$$

In this case, $D_{\text{ncode,l}}$ denotes the summation of digital equivalent of errors occurred in the capacitors tied low on the negative side. Equation (17) states that during digital trimming process, it is possible to add the sum of the errors found on the positive and negative side of the MSB capacitors that are decided to be connected to V_{ref} on the P-side. This sum need to be added with the intermediate digital output got with mismatched physical capacitances to get the final digital output value. Equations (14) and (17) show different ways of doing digital trimming process both of which are valid.

IV. Measurement Results

The proposed on-chip, self-calibrated, and digitally trimmed HV compliant SAR ADC core occupies an area of 9.76 mm^2. This area includes HV compliant bootstrapped input switches, internal reference, reference buffer, internal oscillator, fuses,

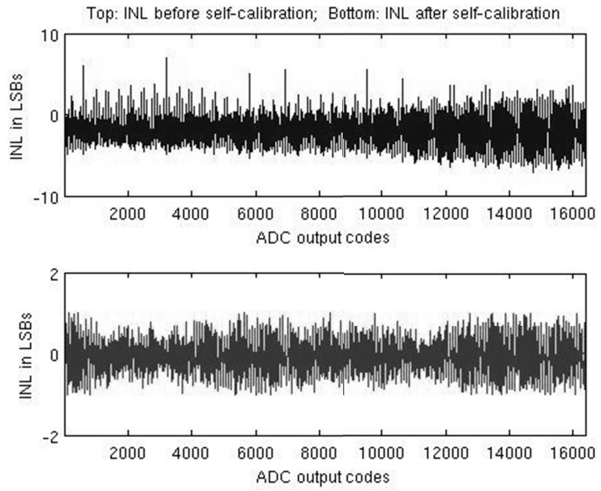

Fig. 8. INL before and after self-calibration.

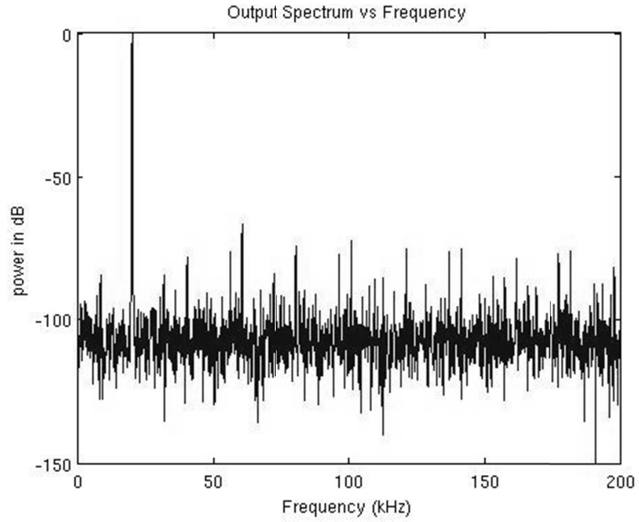

Fig. 9. FFT plot before self-calibration.

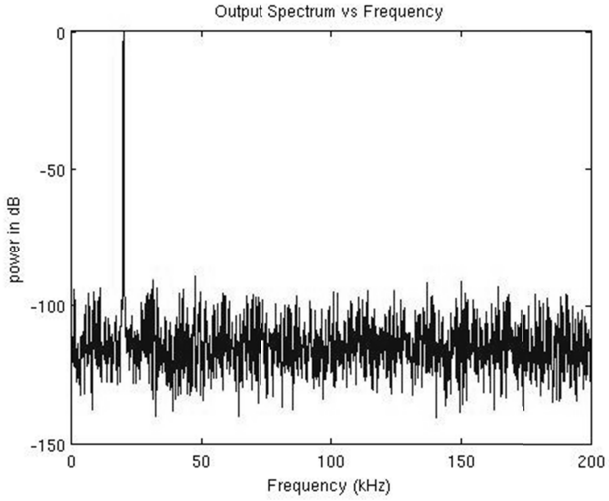

Fig. 10. FFT plot after self-calibration.

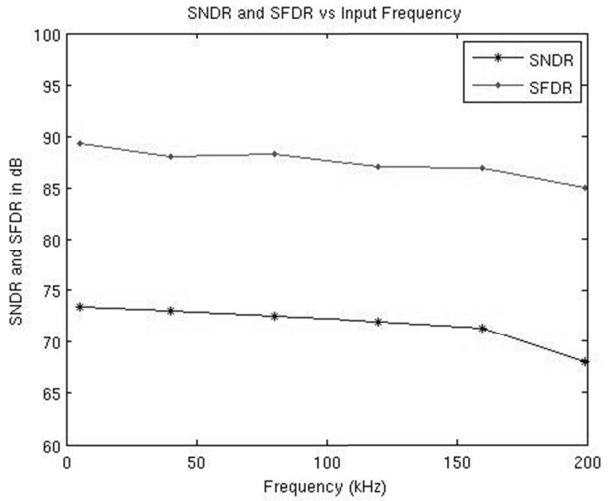

Fig. 11. SNDR and SFDR plot versus input frequency.

and digital logic. A die micrograph is shown in Fig. 6. This SAR-ADC consumes about 90 mW during normal operation from ± 15 V supply. Input capacitance of 40 pF is used in each CDAC and an internal reference of 4.096 V is used in this design. The SAR uses a master clock of 20 MHz, and a differential DEC is performed at bit-6 and bit-12 positions using 256- and 4-LSB capacitors, respectively. Moreover, single-ended DEC is also performed at bit-14 position using 2-LSB capacitor. The density of the poly1-trinitride capacitors used in CDAC array is 0.63 fF/μm^2. The analog and digital circuitry for the proposed technique occupies less than 4% of the total area and consumes less than 3 mA during calibration. The proposed calibration technique has minimum impact on power consumption during normal operation. Self-calibrating the differential array takes just 515 μs on power-up, and digital trimming process does not take any additional time. Fig. 7 compares the DNL before self-calibration and after self-calibration. Similarly, Fig. 8 compares the INL. It was seen that the INL errors in the order of 7 LSBs are reduced to less than 1 LSB after self-calibration at 14-bit level. Figs. 9 and 10 compare the FFT plot of the samples collected at the output of ADC before and after self-calibration. For this case, the ADC is converting an input sine wave of 5.053 kHz while running at a sampling rate of 400 kS/s. As shown in Fig. 9, before self-calibration, the ADC has less than 65-dB total harmonic distortion (THD) due to capacitive mismatch. This THD improves by 24 dB after self-calibration is performed. The signal-to-noise and distortion ratio (SNDR) value before self-calibration is 61.29 dB, and after self-calibration, it is 73.32 dB. Fig. 11 shows the SNDR and SFDR values across different input frequencies. The DEC is used both during normal operation as well as during initial calibration. The DEC improves the INL performance of the order of 0.5 LSB at 400 kS/s. While running at 500 kS/s, it makes a difference of 1 LSB with and without DEC. The overhead being the three extra clock cycles for each conversion, but the clocks now run faster with DEC to compensate for it. Even after accounting for three extra clocks for DEC, the effective conversion speed is much higher for the required INL performance. Table I tabulates the achieved performance with this implementation

TABLE I
SILICON PERFORMANCE

Technology	0.6 um HV CMOS Process
Resolution	14-bit
Conversion Rate	400 KHz
Area	9.76 mm^2
Input Voltage	+/-12 V
Supply Voltage	+/-15 V
SNDR	73.32 dB
THD	89 dB
Total Power Consumption	90 mW
INL	0.95 LSB
DNL	0.92 LSB
Input Capacitance	40pF

TABLE II
COMPARISON WITH THE STATE-OF-THE-ART WORKS AND SPECIFICATION SUMMARY

	Verma, JSSC 2007, [1]	AD7610	ADS8504	This Work
Process	0.18u	NA	0.6u	0.6u
ENOB (bit)	10.5 @ 50kHz	15.2 @ 2kHz	11.8 @ 45kHz	11.9 @ 5kHz
Sampling Frequency (kS/s)	100	250	250	400
Power (mW)	0.025	90	70	90
Area (mm2)	0.63	NA	NA	9.76
Input Range	1-V	+/-10-V	+/-10-V	+/-12-V
Resolution	12	16	12	14

and Table II compares this paper with respect to other state-of-the-art ADCs.

V. CONCLUSION

A power-on self-calibration and digital-trimming algorithm for a 14-bit HV SAR ADC converter is presented. By using the proposed approach, even a larger mismatch of around 261 LSBs can be corrected to improve yield. The algorithm can be adopted for SAR ADCs with both differential CDACs and single-ended ones. This is the only calibration algorithm known in literature to correct for mismatches occurring on any bit capacitance between the P-side and N-side arrays in addition to correcting for mismatches within the binary weighted capacitors inside any array. Also, this algorithm is unique to detect and correct for charge injection-based offset error in self-calibration, and at the same time, it eliminates mismatches occurring between the dynamic error correction capacitors and normal capacitors. This algorithm is also more robust since it finds the errors on capacitors of both P-side and N-side arrays individually and so it could correct a wide range of errors including the mismatch between the arrays. Also, this self-calibration routine could be run on SAR ADCs during each power-on so that the capacitive mismatches that could occur due to environmental conditions, such as temperature and process variations affecting the linearity of the ADCs could be totally eliminated.

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Shankar Thirunakkarasu (M'09) received the B.E. degree in electronics and communication engineering from the College of Engineering at Guindy, Anna University, Chennai, India, in 2002, and the M.S. degree in electrical engineering from Arizona State University, Tempe, AZ, USA, in 2008, where he is currently pursuing the Ph.D. degree.

He was a Design Intern at On-Semiconductor, Phoenix, in 2007. From 2008 to 2013, he was with Nyquist Converter Group and the Advanced Development for Precision Data Converters Group at Texas Instruments, Tucson, AZ, USA, where he was involved in designing high-resolution A/D converters. Since 2013, he has been with Broadcom, Austin, TX, USA, where he is involved in the design of communication receivers for satellite and TV applications. His current research interests include high-performance and high-frequency analog/mixed signal circuit designs.

Bertan Bakkaloglu (M'94–SM'08) received the Ph.D. degree from Oregon State University, Corvallis, OR, USA, in 1995.

He joined the Mixed Signal Wireless Design Group at Texas Instruments Inc., Dallas, TX, USA, where he is involved in analog, RF, and mixed-signal front ends for wireless and wireline communication ICs. He was involved in system-on-chip designs with integrated battery management and analog baseband functionality as a Design Leader. In 2004, he joined the Department of Electrical Engineering at Arizona State University, Tempe, AZ, USA, as an Associate Professor. His current research interests include RF and PA supply regulators, RF synthesizers, biomedical and instrumentation circuits and systems, high-speed RF data converters, and RF built-in-self-test circuits for communication ICs.

Dr. Bakkaloglu has been a Technical Program Chair and Steering Committee Member of the IEEE RFIC Conference, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.