Guest Editorial Selected Papers From IEEE Nordic Circuits and Systems Conference (NorCAS) 2022

THIS special section is composed of substantially extended handpicked papers from the IEEE Nordic Circuits and Systems Conference (NorCAS) 2022 that took place in October 2022 in Oslo, Norway.

IEEE NorCAS is financially cosponsored by the IEEE Circuits and Systems Society, and its roots extend to the 1980s and 1990s when its predecessors *NORCHIP*, the Nordic Microelectronics Conference, and *SoC*, the International Symposium on System-on-Chip were launched, respectively. These traditional IEEE technically cosponsored conferences were merged in 2015 to start the IEEE NorCAS conference series. The annual NorCAS event circulates in Nordic and Baltic countries.

The wide scope of the conference promotes cross-field collaboration not only between academics but also with industry. Peer-reviewed papers of high scientific and technical quality are presented together with keynotes delivered by distinguished speakers from industry and academia. There are three tracks in the conference: analog, digital, and system-on-chip. Also, timely special sessions are organized at the discretion of the steering and organization committees of the conference. The papers in this special section originate from the three regular tracks of IEEE NorCAS 2022. They showcase many recent trends in analog and digital circuits as well as in system-on-chip computing.

In [A1], Huang and Rodriguez present an in-depth noise analysis of biopotential acquisition chopper instrumentation amplifiers with analog dc-servo loops. Biopotential signals such as those present in electrocardiography (ECG), electromyography (EMG), and electroencephalography (EEG) are typically weak, in the order of a few μV to mV. They are vulnerable to low-frequency noise, especially the $1/f$ noise present in CMOS amplifiers. A commonly used circuit design technique to cope with this problem is to employ chopper-stabilized biopotential amplifiers. In addition, the electrode dc offset which is a crucial challenge in biomedical amplifier design, is often compensated through the use of active feedback, known as dc-servo loop. In the article, analytical expressions that predict the noise of different dc-servo loop implementations are found, and a design flow to minimize their noise contribution is proposed. The design methodology is demonstrated with example circuits targeting biopotential recording systems. These circuits are implemented using a standard 180-nm CMOS technology, and their performance is verified through post-layout simulations.

Another paper on biosignal processing, Loh and Gemmeke [A2] address deep neural network (DNN) classifiers for ECG monitoring to identify asymptomatic and critical health conditions. The acceleration of DNN models in application-specific integrated circuits (ASICs) is one method for the integration of such classifiers in the Internet-of-Things (IoT) devices. To that end, the authors use an algorithm-hardware codesign methodology to design ECG accelerators. The goal of the work is to enable handling increasingly complex DNN classifiers for continuous data streams with ultralow-power characteristics. The ultralow-power operation can be traced back to a multitude of possible reasons, e.g., sparse activation, small input frames, and low-complexity classifier. The proposed design methodology leans on providing normalized specifications for continuous ECG monitoring, to reach ultralow-power requirements.

Control-bounded analog-to-digital conversion enables a flexible design framework that promotes co-optimization between the analog and digital domains of an analog-to-digital converter (ADC). In [A3], Feylin et al. present analytical tools for the high-level design of the leapfrog control-bounded A/D converter. Leapfrog is one of the fundamental ADC architectures that consists of a chain of integrators, with leapfrog feedback, where each integrator is individually stabilized by local digital control. The authors derive closed-form design equations for parameterizing the analog system for a target signal-to-noise ratio and bandwidth. Their simulations show that the nominal performance of the leapfrog is similar to that of a continuous-time sigma–delta modulator of the same loop filter order and with the same number of quantization levels. The simple, modular structure, analytical stability guarantee, and single-bit quantizers make the leapfrog an interesting alternative to conventional continuous-time sigma–delta modulators.

Optical interconnects are increasingly needed in data communication applications. Vertical-cavity surface-emitting lasers (VCSELs) are widely used as short-haul optical links in data centers and supercomputers due to their power efficiency, low cost, and high reliability. In [A4], Mowlavi et al. review the state of the art in VCSEL driver design, including choices of semiconductor technology, modulation format, VCSEL configuration, and preemphasis techniques, with an emphasis on the challenges associated with VCSEL bandwidth limitations, nonlinearities, and thermal behavior. There is presently no

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universal choice of implementation technology for VCSEL driver circuits. Pure CMOS is much used and offers integration benefits. On the other hand, SiGe BiCMOS processes can provide currents, voltage swings, and operation frequencies that are difficult to match with pure CMOS. VCSEL temperature dependence further complicates the driver-design problem. The authors conclude that continued efforts are needed in this field.

Nonvolatile storage is needed both in low-energy devices such as the IoT devices and in embedded computing devices for saving energy by powering off the circuitry. Introducing a magnetic tunneling junction (MTJ) into a flip-flop enables nonvolatile power gating but large store energy to MTJ is a critical concern. In [A5], Usami et al. propose a two-step store (TSS) process, with short and long store steps. They implement a software-controlled TSS using a horizontal microprogrammed approach in a coarse-grained reconfigurable array accelerator chip and carry out real measurements for the break-even time, which is the minimum powered-off time to get the gain in energy savings in nonvolatile power gating. As a result, the energy consumption of the MJT-based storage could be reduced to one-third, with sub-ms break-even times.

Compute-in-memory (CIM) is a recent trend in the quest for lower energy consumption, especially in computing tasks requiring a lot of data exchange. In [A6], Lanius and Gemmeke apply CIM on the very intense task of genome sequencing. They build a CIM array using standard cells, to accelerate sorting and searching in memories, both crucial components of genome alignment algorithms. Their solution is unique in enabling arbitrary-sized sorting ON-chip. Their design was fabricated using 22-nm FDSOI technology, yielding a throughput of up to 4.28 GB/s and as low as 4.97-nJ/sort energy consumption.

The scalability of the performance of multiprocessor systems-on-chip (MPSoC) is increasingly limited by the efficiency of interprocess communication mechanisms. In [A7], Nolte et al. address the issue of thread synchronization in MPSoC by proposing a hardware solution for implementing the futex() syscall, that is used to construct blocking synchronization primitives. The authors introduce HW-FUTEX to offload the futex wake functionality to a hardware unit that asynchronously initiates wake-ups of the sleeping threads. This reduces the time required to issue the futex wake functionality by at least 90% to 350 Hz. The proposed approach does not affect the uncontended case and does not require any changes to the kernel's source code.

In fifth-generation (5G) communication systems, high-performance digital transmitter structures are needed. In [A8], Ghosh et al. present an efficient implementation of a highly parameterized circuit generator. The reconfigurable DSP hardware was developed using CHISEL, which uses Scala functional language to support the highly parameterized circuit generator. Multiple architectures for the reconfigurable DSP were synthesized in a 5-nm technology node. The generated hardware for multimodulation DSP achieves an error vector magnitude (EVM) of 0.78% and an adjacent channel leakage ratio (ACLR) of -48 dB for multilevel outphasing modulation with a 200-MHz 5G new radio (NR) baseband signal. We consider the universal design method for a reconfigurable signal processing hardware generator for multiple transmitter architectures to be of high value to the community.

As a conclusion, the conference and this special section managed to showcase a wide range of innovations in circuits and systems, from analog and RF circuitry up to the hardware–software interface.

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APPENDIX: RELATED ARTICLES

[A1] Y.-K. Huang and S. Rodriguez, "Noise analysis and design methodology of chopper amplifiers with analog DC-servo loop for biopotential acquisition applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 32, no. 1, pp. 56–68, Jan. 2024.

[A2] J. Loh and T. Gemmeke, "Stream processing architectures for continuous ECG monitoring using subsampling-based classifiers," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 32, no. 1, pp. 69–79, Jan. 2024.

[A3] F. Feyling, H. Malmberg, C. Wulff, H.-A. Loeliger, and T. Ytterdal, "Design and analysis of the leapfrog control-bounded A/D converter," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 32, no. 1, pp. 80–89, Jan. 2024.

[A4] S. Mowlavi, S. Giannakopoulos, A. Grabowski, and L. Svensson, "A review of IC drivers for VCSELs in datacom applications," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 32, no. 1, pp. 43–55, Jan. 2024.

[A5] K. Usami et al., "Optimized two-step store control for MTJ-based nonvolatile flip-flops to minimize store energy under process and temperature variations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 32, no. 1, pp. 90–103, Jan. 2024.

[A6] C. Lanius and T. Gemmeke, "Fully digital, standard-cell-based multifunction compute-in-memory arrays for genome sequencing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 32, no. 1, pp. 31–42, Jan. 2024.

[A7] L. Nolte et al., "HW-FUTEX: Hardware-assisted futex syscall," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 32, no. 1, pp. 17–30, Jan. 2024.

[A8] A. Ghosh et al., "Reconfigurable signal processing and DSP hardware generator for 5G and beyond transmitters," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 32, no. 1, pp. 5–16, Jan. 2024.

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