Noise Analysis and Design Methodology of Chopper Amplifiers With Analog DC-Servo Loop for Biopotential Acquisition Applications

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***Abstract*— Biopotential acquisition chopper instrumentation amplifiers require a dc-servo loop (DSL) in order to filter electrode dc offsets. However, the noise performance degradation due to the addition of the DSL is often overlooked despite that it can be very detrimental at the frequencies of interest. This article presents an in-depth noise analysis of biopotential acquisition chopper instrumentation amplifiers with analog DSLs. Analytical expressions that predict the noise of different DSL implementations are found and a design flow to minimize their noise contribution is proposed. The design methodology is demonstrated with example circuits targeting biopotential recording systems. These circuits are implemented using a standard 180 nm CMOS technology, and their performance is verified through postlayout simulations. The findings of this work provide a comprehensive understanding of the noise characteristics of a DSL, its impact on noise performance, and design strategies for noise optimization.**

***Index Terms*— Analog front-end, biopotential acquisition, capacitively coupled instrumentation amplifier (CCIA), chopper amplifier, current-balancing instrumentation amplifier (CBIA), dc-servo loop (DSL), low-noise amplifier, noise analysis, noise modeling.**

I. Introduction

BIOPOTENTIAL signals such as those present in electrocardiography (ECG), electromyography (EMG), and electroencephalography (EEG) are typically weak, in the order of a few μV to mV, and mainly distributed in a low-frequency range below 1 kHz as illustrated in Fig. 1 [1], [2]. Accordingly, they are vulnerable to low-frequency noise, especially the $1/f$ noise present in CMOS amplifiers. A commonly used circuit design technique to cope with this problem is to employ chopper-stabilized biopotential amplifiers. This technique has been extensively adopted in biosensing analog front-ends [3], [4], [5], [6], [7] since it provides $1/f$ noise suppression, low-offset, continuous-time operation, and low noise-folding compared to autozeroing technique [8].

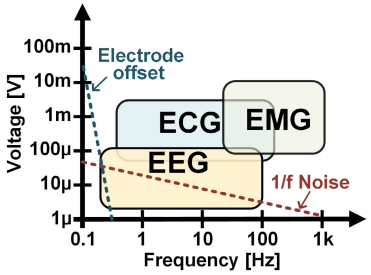

Fig. 1. Characteristics of biopotential signals.

In addition to stringent $1/f$ noise requirements, biopotential amplifiers face an additional challenge in the form of electrode dc offset (EDO). The EDO arises due to the difference in half-cell potentials between the electrode and the electrolyte, which can be as high as tens of millivolts for gel electrodes [9]. The EDO is a crucial consideration in biopotential amplifier design, as it can saturate the amplifier chain and distort the signal. Although commonly treated as a dc offset, in reality, EDO is not constant and exhibits variations over time due to electrode displacement. To address this issue, the biopotential amplifier must have ac-coupling characteristics that eliminate the EDO.

One possible solution is to use capacitively coupled instrumentation amplifiers (CCIAs) which are implemented by placing a series dc-blocking capacitor at the input as illustrated in Fig. 2(a) [10], [11], [12]. Since the amplification factor and the high-pass corner frequency are determined by the ratio between C_F and C_{in} and the time constant of $R_F C_F$, respectively, very large capacitors are commonly required in order to achieve high gain and extremely low cut-off frequencies. This is impractical in multichannel recording applications as a large silicon area would be required. Besides the area penalty, the mismatch between the capacitors makes the CCIA sensitive to large common-mode interference. To mitigate the mismatch between the capacitors, a chopper is commonly placed in front of input capacitors and another chopper is placed at the

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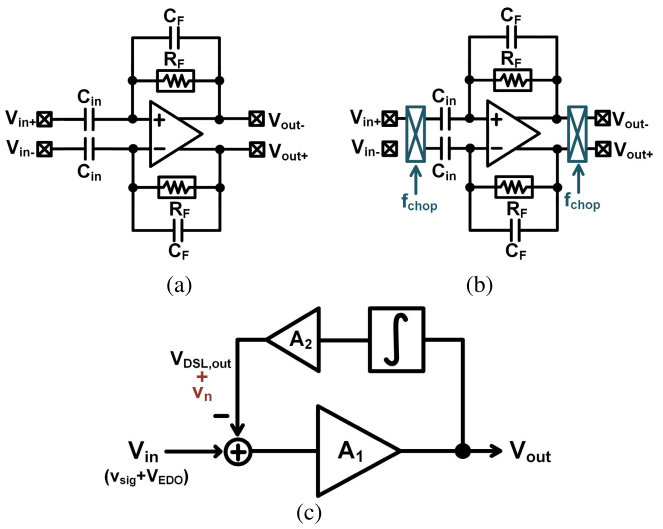


Fig. 2. Architecture of biopotential amplifiers. (a) CCIA. (b) Chopper CCIA. (c) DSL.

output of the amplifier as depicted in Fig. 2(b) [13], [14], [15]. In this way, the common-mode interference that is converted to differential-mode due to mismatches is upconverted to a higher frequency. However, the addition of chopping has the following drawbacks. First, the presence of a switched-capacitor at the input impacts the input impedance. The input impedance of a CCIA is approximately $1/2f_{\text{chop}}C_{\text{in}}$, where f_{chop} represents the chopping frequency and C_{in} refers to the series dc-blocking capacitor [16]. Second, the placement of the chopper before the input capacitors upconverts the EDO, preventing it from being blocked. Consequently, additional circuitry is required to suppress the EDO.

An alternative approach to achieve ac-coupling and filtering the EDO is through the use of active feedback, as demonstrated in Fig. 2(c). This topology, commonly known as a dc-servo loop (DSL), involves an integrator in a negative feedback loop. The integrator extracts the dc component, including the low-frequency offset, from the output signal and feeds it back to the input, where it is subtracted [17]. Through this mechanism, the DSL can eliminate the EDO present in the signal, thereby providing an effective means of achieving ac-coupling characteristics. This approach can be applied to design an EDO-rejection chopper CCIA by utilizing a voltage-mode DSL (VM-DSL) through a capacitor feedback network. Alternatively, this approach can be implemented as a current-mode DSL (CM-DSL) in which the DSL generates a current output that can be subtracted at low-impedance nodes in the amplifier. This method requires fewer capacitors, making it more area-efficient and a preferred solution for integration.

DSL circuits provide an efficient way to remove the EDO, however, they also have drawbacks. One of its major drawbacks is the introduction of additional electronic noise, which can easily become detrimental to low-noise biosensor applications as demonstrated in [4], [17], [18], and [19]. While significant effort has been devoted to the noise analysis and optimization of chopper amplifiers [4], [16], [20], [21], a comprehensive analysis of the noise contribution of the

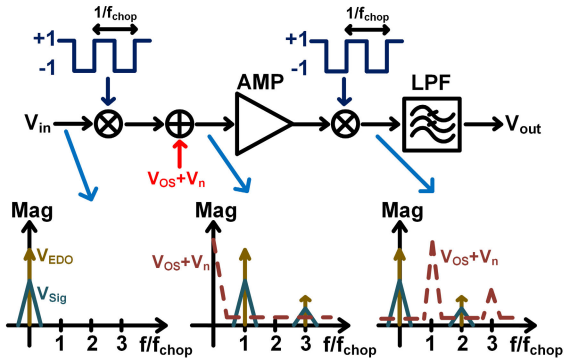


Fig. 3. Conceptual diagram of chopper stabilization [22].

DSL has not been widely investigated. A poorly designed DSL can become the primary source of noise in the amplifier chain, thereby reducing the signal-to-noise ratio (SNR) and compromising the amplifier's performance. Therefore, it is essential to understand its noise characteristics and how it affects the overall noise performance of an amplifier. In this study, we aim to perform a thorough theoretical analysis of the noise contribution of the DSL and propose a design methodology to minimize its impact. By characterizing the DSL's noise, we can optimize its design, mitigate its noise contribution, and improve the overall amplifier's SNR.

This article is structured as follows. Section II provides a brief explanation of the chopper instrumentation amplifier's operating principle and analog DSL circuit architectures that can be configured either in voltage-mode or current-mode. In Section III, the noise analysis of the chopper amplifier is presented, and the impact of the DSL, including its noise modeling and noise contribution, is discussed. Section IV demonstrates transistor-level circuit examples and a design methodology to enhance the noise performance. Finally, Section V presents a discussion followed by conclusions in Section VI.

II. Basic Principle

A. Chopper Stabilization Technique

The basic principle of a chopper-stabilized amplifier is illustrated in Fig. 3. The input signal is upconverted by the input chopper to the chopping frequency f_{chop}. The amplifier's input-referred offset voltage v_{os} and the electronic noise v_n, including $1/f$ noise and thermal noise, are then added to the chopped-modulated signals. Thanks to the upmodulation of the signal before being amplified, $1/f$ noise is not present in the frequency band of interest if the condition of $f_{\text{chop}} > f_c$ is fulfilled, where f_c is the corner frequency of the $1/f$ noise. After amplification, the signal of interest is downconverted to baseband while the unwanted $1/f$ noise and v_{os} are upconverted to f_{chop}. Likewise, common-mode interference that is converted to the differential-mode signal due to mismatches in the amplifier is also upconverted to f_{chop}, resulting in an improvement of the low-frequency common-mode rejection ratio (CMRR). The noise located at odd harmonics of f_{chop} and other upconverted unwanted signals can be suppressed

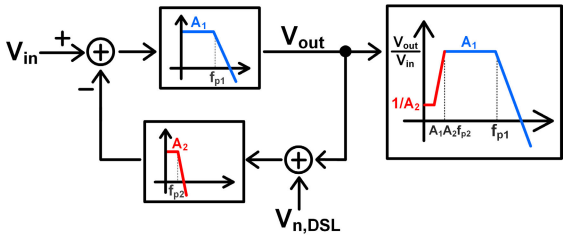


Fig. 4. Signal flow of an amplifier with DSL [22].

by a low-pass filter. The chopper-stabilized amplifier offers very good noise performance within the band of interest for biopotential sensing. However, it still requires additional circuitry to filter the EDO.

B. DC-Servo Loop

The EDO can be filtered by adding a negative feedback DSL as depicted in Fig. 4. The chopper amplifier is modeled as a single-pole system with a gain of A_1 and cut-off frequency f_{p1}. Likewise, the DSL is modeled as a single-pole system with a gain of A_2 and a pole at f_{p2}. Assuming that $f_{p1} \gg f_{p2}$, the overall transfer function is given by

$$\frac{V_{\text{out}}}{V_{\text{in}}}(s) = \frac{1}{A_2}\frac{1+s/2\pi f_{p2}}{1+[(1+s/2\pi f_{p1})(1+s/2\pi f_{p2})]/A_1A_2} \approx \begin{cases} \frac{1}{A_2}\dfrac{1+s/2\pi f_{p2}}{1+s/2\pi A_1A_2 f_{p2}}, & \text{for } f < f_{p2} \\ \dfrac{A_1}{1+s/2\pi f_{p1}}, & \text{for } f > f_{p1}. \end{cases} \quad (1)$$

Accordingly, the cut-off frequency of the high-pass response is $A_1A_2f_{p2}$ and the dc component is suppressed by $20\log(1/A_2)$ dB.

The noise contribution of the DSL can be analyzed by extracting the transfer function from the input-referred noise of the DSL, $V_{n,\text{DSL}}$, to the output of the amplifier V_{out}. For low frequencies, the noise transfer function is

$$\text{NTF}_{\text{DSL}} = \frac{V_{\text{out}}}{V_{n,\text{DSL}}} = -\frac{A_1A_2}{1+A_1A_2} \approx -1. \quad (2)$$

Consequently, the low-frequency noise of the DSL appears at the output without attenuation and it may become a significant noise contributor to the core amplifier. For this reason, it is essential to conduct a meticulous analysis of the noise contribution of a DSL and optimize its design to achieve the desired noise performance.

C. Architecture of Chopper Amplifier With Analog DSL

The voltage-mode DSL (VM-DSL) [7], [14], [15] and the current-mode DSL (CM-DSL) [7], [23], [24] are two distinct analog DSL implementations used for EDO cancellation as demonstrated in Fig. 5. VM-DSL is commonly employed in CCIA design. This topology comprises a core amplifier (A_{V1} and A_{V2}), choppers (CH_{in} and CH_{out}), and a capacitor negative feedback loop, which determines the amplification factor by the ratio between C_{in} and C_f. The VM-DSL loop integrates the output voltage of the core amplifier and directly

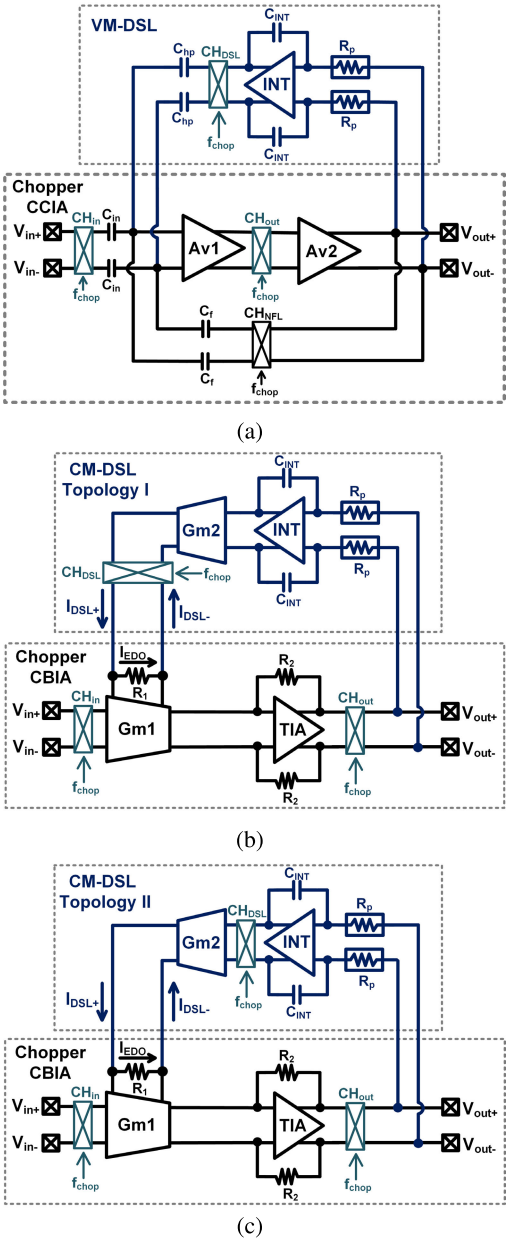


Fig. 5. Block diagram of instrumentation amplifiers with DSL. (a) Voltage-mode DSL. (b) Current-mode DSL topology I. (c) Current-mode DSL topology II.

feeds it back to the input by using the capacitors C_{hp}. Through this mechanism, the VM-DSL can effectively remove the EDO from the input signal. The maximum EDO rejection ($V_{\text{EDO,max}}$) and the high-pass cut-off frequency (f_{hp}) of this architecture are determined by

$$V_{\text{EDO,max}} = \frac{V_{\text{out,max}}C_{\text{hp}}}{C_{\text{in}}} \approx V_{\text{DD}}\frac{C_{\text{hp}}}{C_{\text{in}}} \quad (3)$$

$$f_{\text{hp}} = f_{u,\text{INT}}\frac{C_{\text{hp}}}{C_{\text{in}}}\frac{C_{\text{in}}}{C_f} = f_{u,\text{INT}}\frac{C_{\text{hp}}}{C_f} \quad (4)$$

where the $f_{u,\text{INT}}$ is the unit-gain frequency of the integrator.

The VM-DSL requires only a single integrator in the feedback loop, resulting in reduced power consumption. However, this approach requires the use of several capacitors, which occupy a significant silicon area. Therefore, proper capacitor

sizing is essential to minimize area overhead while also ensuring adequate performance of the amplifier.

An interesting alternative that requires fewer passive components is the CM-DSL. Two CM-DSL topologies are analyzed in this study: CM-DSL topology I [Fig. 5(b)], and CM-DSL topology II [Fig. 5(c)]. The CM-DSL is typically associated with the current-balancing instrumentation amplifier (CBIA) [25]. The CBIA consists of a transconductance amplifier (Gm) and a transimpedance amplifier (TIA). This is a popular architecture for biopotential amplifier design as it offers higher CMRR and lower power consumption compared to the traditional three-OPAMP IA structure [26]. In this architecture, EDO results in a current I_{EDO} flowing through the degeneration resistor R_1, which is compensated by the I_{DSL} generated by the CM-DSL. Compared to VM-DSL, CM-DSL has the advantage of eliminating the need for capacitors, thereby saving silicon area, achieving higher input impedance, and improving the CMRR due to the absence of capacitor mismatch. The maximum EDO rejection and the high-pass cutoff frequency are calculated by

$$V_{\text{EDO,max}} = I_{\text{DSL,max}} R_1 \tag{5}$$

$$f_{\text{hp}} = f_{u,\text{INT}} \text{Gm}_2 R_2 \tag{6}$$

where $I_{\text{DSL,max}}$ is the dc biasing current at the output stage of Gm_2, which is the maximum output current that can be supplied by Gm_2. Hence, there exists a trade-off between maximum EDO rejection and power consumption in the design of this architecture.

As discussed in Section II, the input chopper upconverts the input signal, comprising of biopotentials and unwanted EDO, to f_{chop}. Accordingly, the EDO is modulated from dc to f_{chop} and ultimately becomes a square wave current flowing through R_1. Therefore, the extracted dc component at the DSL requires an upconversion to f_{chop} before the subtraction of EDO can take place. In CM-DSL, the upconversion can be done either by placing a chopper at the output of the loop or at the output of the integrator as depicted in Fig. 5(b) and (c), respectively. Therefore, there is a design choice on where the chopper should be placed.

III. Noise Analysis

Thermal noise and $1/f$ noise are widely recognized as the most critical noise sources in CMOS low-noise amplifiers. In biosensing applications, the noise performance of the first amplifier in the front end plays a significant role in determining the overall system performance. As such, it is essential to accurately characterize and mitigate its noise sources. In this section, we will present a detailed theoretical analysis of noise performance in chopper-stabilized amplifiers which incorporates analog DSLs. We will investigate the effects of the DSL on the amplifier's noise performance and provide insights into design considerations for achieving optimal performance.

A. Effect of Chopping Modulation on the Amplifier's Noise

The noise model of a chopper instrumentation amplifier is depicted in Fig. 6. The noise of the amplifier is equivalently represented by the input-referred voltage source ($\hat{v}_{n,\text{IA}}$)

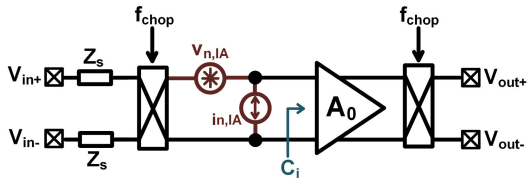


Fig. 6. Noise model of a chopper amplifier.

in series and its input-referred current source ($\hat{i}_{n,\text{IA}} = \hat{v}_{n,\text{IA}}(j\omega C_i)$) in parallel to a noiseless amplifier. The total input-referred noise power spectrum density (PSD) is then calculated by

$$S_{N,\text{in}}(f) = \overline{v_{n,\text{IA}}^2} + 4\,\overline{i_{n,\text{IA}}^2} Z_s^2. \tag{7}$$

Consequently, (7) can be rewritten as follows:

$$S_{N,\text{in}}(f) = \overline{v_{n,\text{IA}}^2}\left(1 + \omega^2 C_i^2 Z_s^2\right) \tag{8}$$

$$= S_{N0}\left(1 + \frac{f_c}{f}\right), \quad \text{for } f \ll 1/C_i Z_s \tag{9}$$

where Z_s is the source's impedance and C_i is the input capacitance of the amplifier. At low frequencies, the first term in (7) dominates. Therefore, the input-referred noise PSD at low frequencies, where the noise contribution from the current noise $i_{n,\text{IA}}$ is negligible, can be rearranged to a thermal noise term S_{N0} added to a low-frequency $1/f$ noise term as given in (9) where f_c denotes the noise corner frequency. The equivalent input noise is then amplified by the voltage gain, A_0, and modulated with the output chopper. The output noise PSD is the summation of the replicas of the noise spectrum located at odd harmonic frequencies of f_{chop}

$$S_{N,\text{out}}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{k=-\infty \\ k \text{ is odd}}}^{+\infty} \frac{1}{k^2} A_0^2 S_{N,\text{in}}(f - k f_{\text{chop}}). \tag{10}$$

After chopping demodulation, the output signal spectrum is transposed to the baseband. Accordingly, the output noise at the baseband is crucial to the design. At the frequency band where $f \le 0.5 f_{\text{chop}}$, (10) is nearly constant and can be approximated by a white-noise PSD [8]

$$S_{N,\text{out,BB}}(f) \approx A_0^2 S_{N0}\left(1 + \frac{17 f_c}{2\pi^2 f_{\text{chop}}}\right) \quad \text{for } f_{-3\,\text{dB}} \gg f_{\text{chop}} \tag{11}$$

where $f_{-3\,\text{dB}}$ denotes the 3-dB bandwidth of the amplifier. From (11), it can be observed that the baseband noise level is approximately equal to the thermal noise, S_{N0}, when $f_{-3\,\text{dB}}$ is greater than the f_{chop}. As a result, the chopper stabilization technique efficiently suppresses $1/f$ noise. However, it comes with the trade-off of requiring a larger amplifier bandwidth, consequently leading to higher power consumption.

B. Effect of DSL on Noise Contribution

Fig. 7(a) shows the noise model of the VM-DSL employed on a chopper CCIA. In this architecture, the input-referred noise of the integrator, $v_{n,\text{INT}}$, is the only noise contributor from the DSL loop. It can be observed that the chopper

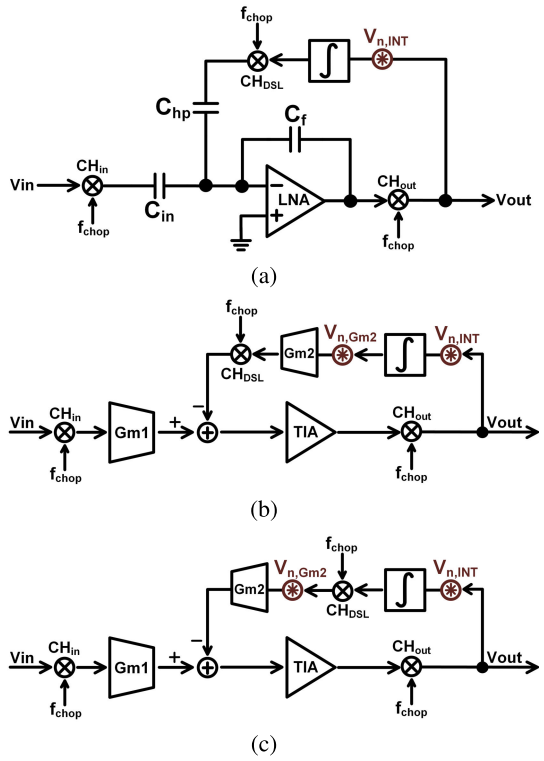


Fig. 7. Noise models of a chopper IA with analog DSL. (a) VM-DSL. (b) CM-DSL topology I. (c) CM-DSL topology II.

modulation is ineffective in suppressing $1/f$ noise from $v_{n,\mathrm{INT}}$ as it is upconverted by $\mathrm{CH_{DSL}}$ and downconverted again by $\mathrm{CH_{out}}$. Therefore, the derivation of output noise does not need to take the frequency modulation of choppers into account. By solving the KCL expression at the input node of the amplifier, the additional output noise resulting from $v_{n,\mathrm{INT}}$ can be derived as follows:

$$\left(v_{\mathrm{out}}(s)+v_{n,\mathrm{INT}}(s)\right)\frac{1}{s\tau}sC_{\mathrm{hp}}+v_{\mathrm{out}}(s)sC_f=0$$
$$\Rightarrow\sqrt{\overline{v_{\mathrm{out}}^2(s)}}=\sqrt{\overline{v_{n,\mathrm{INT}}^2(s)}}\frac{1}{1+s\tau\frac{C_f}{C_{\mathrm{hp}}}} \quad (12)$$

where τ is the time constant of the integrator. The output noise can be referred to the input by dividing it by the voltage gain of the core amplifier, which is proportional to C_{in}/C_f. Consequently, the input signal is susceptible to the $1/f$ noise generated by the integrator, and the extent of its impact depends on capacitor sizing.

Fig. 7 also depicts the noise model of the CM-DSL in which the dc offset-induced current is compensated by the output current of the $\mathrm{Gm_2}$ stage. As explained in Section II, the upconversion in the DSL can potentially occur at two locations as shown in Fig. 7(b) and (c), respectively. In topology I, the chopper is located at the output of the $\mathrm{Gm_2}$ stage. The input-referred noise ($v_{n,\mathrm{in}}$) of the integrator and the $\mathrm{Gm_2}$ stage can be directly calculated by

$$v_{n,\mathrm{in}}(s)=v_{n,\mathrm{INT}}(s)+(s\tau)v_{n,\mathrm{Gm_2}}(s) \quad (13)$$

$v_{n,\mathrm{in}}$ is then upconverted by $\mathrm{CH_{DSL}}$ and downconverted by $\mathrm{CH_{out}}$, resulting in $v_{n,\mathrm{in}}$ appearing at the output of the amplifier almost without attenuation at low frequencies. Consequently, $1/f$ noise from both the integrator and the $\mathrm{Gm_2}$ stage remains at low frequencies, resulting in a significant degradation in noise performance.

Alternatively, the chopper can be placed between the integrator and the $\mathrm{Gm_2}$ stage as shown in Fig. 7(c). Compared to CM-DSL topology I, the noise of the $\mathrm{Gm_2}$ stage is only upconverted once by $\mathrm{CH_{out}}$ in this topology. The equivalent input-referred noise of the integrator, the intermediate chopper, and the $\mathrm{Gm_2}$ stage is derived by

$$v_{n,\mathrm{in}}(s)=\left(\frac{\pi}{2}\right)\frac{s\tau\cdot i_{n,\mathrm{out,DSL}}}{\mathrm{Gm_2}(s)}$$
$$=\sum_{\substack{k=-\infty\\ k\text{ is odd}}}^{+\infty}\frac{1}{k}v_{n,\mathrm{INT}}(f-kf_{\mathrm{chop}})+\left(\frac{s\tau\pi}{2}\right)v_{n,\mathrm{Gm_2}}(f) \quad (14)$$

$v_{n,\mathrm{in}}$ passes through the loop as described in (2), and its contribution to the output noise PSD is derived by modulating (14) with $\mathrm{CH_{out}}$ and multiplying its NTF as follows:

$$S_{n,\mathrm{out}}(f)=\left(\frac{2}{\pi}\right)^2\mathrm{NTF_{DSL}^2}\sum_{\substack{k=-\infty\\ k\text{ is odd}}}^{+\infty}\frac{1}{k^2}S_{n,\mathrm{DSL}}(f-kf_{\mathrm{chop}}). \quad (15)$$

Similar to the chopper amplifier, $\mathrm{CH_{out}}$ transposes the noise of the $\mathrm{Gm_2}$ stage to the odd harmonics of f_{chop}. As a result, the $1/f$ noise is upconverted and not visible at baseband. Consequently, the noise of the $\mathrm{Gm_2}$ stage at the frequencies of interest is mainly white noise. However, the integrator's noise is both upconverted and downconverted, resulting in the $1/f$ noise and the dc offset of the integrator being present at baseband. The output PSD at baseband is approximated by

$$S_{n,\mathrm{BB}}(f)\approx\left[(s\tau)^2S_{N0,\mathrm{Gm_2}}\left(1+\frac{17f_c}{2\pi^2f_{\mathrm{chop}}}\right)+\left(\frac{2}{\pi}\right)^2S_{n,\mathrm{INT}}(f)\right]\left(\frac{1}{\frac{s\tau}{\mathrm{Gm_2}Z_{\mathrm{TIA}}}+1}\right)^2 \quad (16)$$

where Z_{TIA} is the effective transimpedance of the TIA stage. It is worth noting that the noise below the cut-off frequency of the DSL loop, which is $\mathrm{Gm_2}Z_{\mathrm{TIA}}/\tau$, is nearly unattenuated. Fig. 8 shows the comparison between CM-DSL topology I and II. Topology II takes advantage of the chopper for improving noise performance, especially the low-frequency noise. Nevertheless, according to the noise analyses of these two topologies, we can draw a conclusion that a CBIA cannot be fully free from $1/f$ noise if a DSL is present. However, the noise can be reduced by the proper selection of circuit architecture, sizing of components, and biasing.

So far, the noise contribution of the CM-DSL to the output noise PSD has been identified. For further noise optimization, we are interested in the contribution of the DSL's noise to the input-referred noise of the amplifier, especially at low frequencies where the $1/f$ noise of the integrator dominates. The input-referred noise PSD is calculated as $S_{n,\mathrm{out}}^2(s)/H(s)^2$, where $H(s)$ is the transfer function of the CBIA with DSL. At low frequencies where the loop gain of the DSL is much greater than 1, $H(s)$ is inversely proportional to the gain of

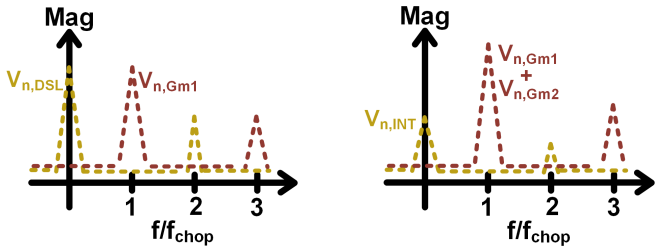


Fig. 8. Output noise spectrum of CM-DSL. (a) Topology I. (b) Topology II.

TABLE I
TARGET SPECIFICATIONS

Parameters	Target Specifications
Technology	Standard 180 nm CMOS process
Gain	40 dB
Bandwidth	1 Hz to 1 kHz
Total Input-referred Noise	$<1\,\mu$Vrms
Electrode Offset Tolerance	>50 mV
CMRR	>80 dB
Input Impedance	$>10\,\mathrm{M}\Omega$
Area	as small as possible
Power	as low as possible

the DSL as we have derived in (1). Accordingly, the $1/f$ noise components of the input-referred noise can then be calculated by

$$S_{1/f,\mathrm{CBIA}}(f) \approx S_{1/f,\mathrm{INT}}(f)\left(\frac{\mathrm{Gm}_2}{s\tau \mathrm{Gm}_1}\right)^2. \tag{17}$$

The contribution of $1/f$ noise is directly proportional to the ratio of $\mathrm{Gm}_2/\mathrm{Gm}_1$. Thus, it is desirable to minimize this ratio to optimize noise performance. However, Gm_2 is related to the loop gain of DSL and hence the attenuation of the EDO as given in (1). On the other hand, power consumption can be traded off for maximizing Gm_1. It can be concluded that there are two design considerations for the design of CBIA with CM-DSL: 1) trade-off between noise and EDO attenuation and 2) trade-off between noise and power consumption.

IV. Circuit Design

To validate the analytical expressions and showcase the impacts of analog DSL on the noise performance of a chopper IA, the circuit architectures shown in Fig. 5 are implemented at transistor level in Cadence[1] Virtuoso[1] ADE. The circuits are implemented using a standard 180 nm CMOS process and are designed to fulfill typical specifications for biopotential acquisition systems while maintaining a low noise level. The circuit architectures and design methodology are presented to demonstrate a systematic design flow for noise optimization. Periodic steady-state (PSS) simulation and periodic noise analysis (Pnoise) are used to obtain the ac response and noise performance. All the simulation results are based on the same PSS analysis setup (shooting method with $f_{\mathrm{beat}} = f_{\mathrm{chop}}$ and maxsideband $= 20$) for a fair comparison.

A. Design Specifications

Biopotential amplifiers must fulfill strict low-noise requirements and incorporate ac coupling characteristics in order to maintain the integrity of weak biopotential signals and to mitigate the EDO, which is on the order of tens of millivolt. Additionally, biopotential amplifiers need to meet certain criteria to avoid corrupting the signal. First, the amplifiers should provide sufficient voltage gain such that biopotential signals are at a measurable level. Second, biopotential signals are weak in comparison to unwanted common-mode signals such as power line interference and motion artifacts. These ones can overwhelm the desired signal, and therefore, high CMRR is a critical performance metric. The amplifiers should also present high input impedance to minimize the loading effect on the electrode and skin–electrode interface. For instance, the impedance of wet Ag/AgCl electrodes can be 350 k$\Omega\|$25 nF, while metal plate electrodes can have an impedance as high as 1.3 k$\Omega\|$12 nF [27]. From the system point of view, high input impedance helps mitigate the effect of electrode impedance imbalances (ΔZ_e), thereby improving the overall CMRR which is given by [28]

$$\mathrm{CMRR}_{\mathrm{sys}} \approx -20\log\left(\frac{\Delta Z_e}{Z_{\mathrm{in,CM}}} + \frac{1}{\mathrm{CMRR}_{\mathrm{Amp}}}\right) \tag{18}$$

where $Z_{\mathrm{in,CM}}$ and $\mathrm{CMRR}_{\mathrm{Amp}}$ represent the common-mode input impedance and amplifier's CMRR, respectively. Last but not least, the design requires low power consumption and small size in order to be amenable for wearable and portable applications that feature multichannel signal recording. Table I summarizes the general specifications of biopotential recording systems [29], [30], which also serve as the design target for implementing the above-mentioned circuit architectures.

B. Design Considerations

Based on the theoretical analysis conducted in Sections II and III, it has been shown that an analog DSL improves the EDO tolerance and rejects low-frequency varying offset by creating an ac-coupling characteristic. However, it requires additional hardware which takes up silicon area, consumes power, and can also become a considerable noise contributor. An analog design octagon [31] as shown in Fig. 9, which is specific for the design of the biopotential chopper IA with DSL, is used to cope with all the design trade-offs.

C. Circuit Design of a Chopper CCIA With VM-DSL

The circuit implementation of a chopper CCIA with a VM-DSL comprising a core amplifier, choppers, a capacitor negative feedback loop, and a DSL is shown in Fig. 10. Detailed device parameters and transistor dimensions are available in Table II. The core amplifier is implemented using a folded-cascode amplifier, which is followed by a common-source output stage. The design of the folded-cascode amplifier focuses on noise optimization as it provides the first-stage amplification. On the other hand, the output stage aims for handling a large voltage swing. The noise of this

[1]Registered trademark.

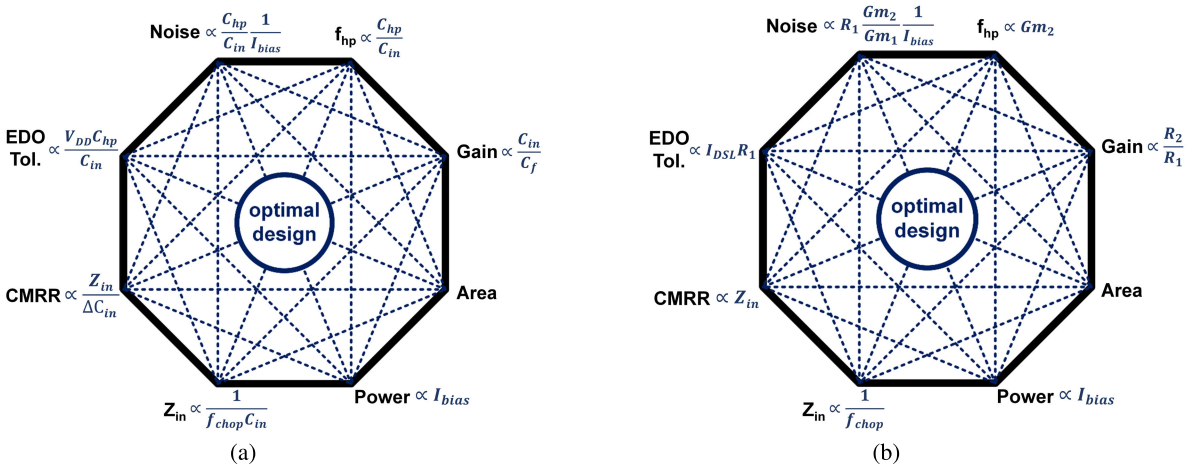


Fig. 9. Design octagon that illustrates the trade-offs in the design of chopper IA with analog DSL. (a) Chopper CCIA with VM-DSL. (b) Chopper CBIA with CM-DSL.

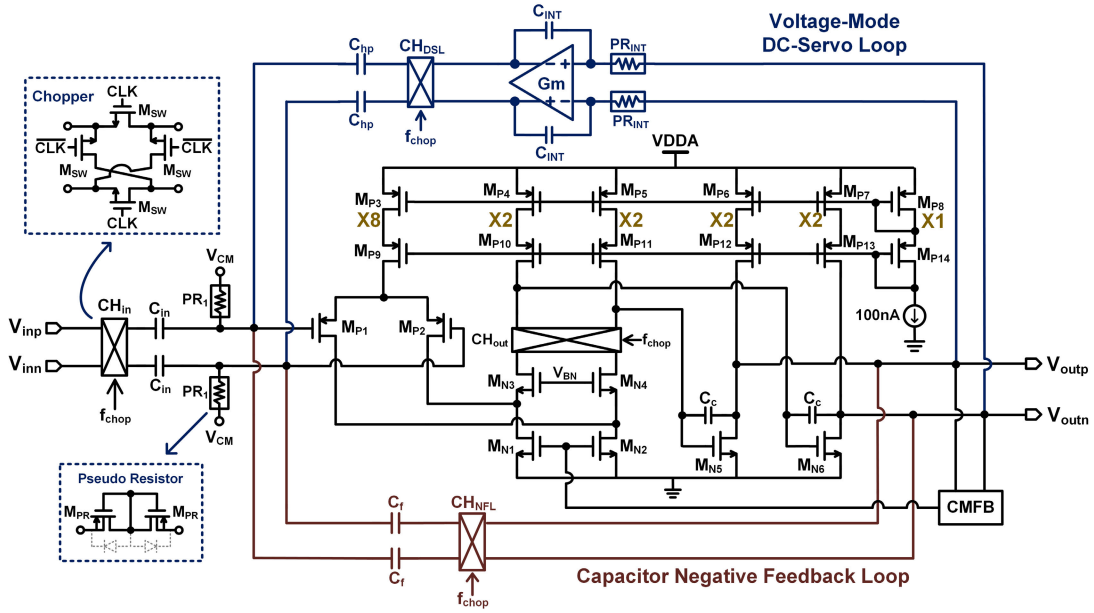


Fig. 10. Schematic of the chopper CCIA with VM-DSL.

TABLE II
DEVICE PARAMETERS AND DIMENSIONS OF TRANSISTORS IN FIG. 10

Transistor	M_{P1}, M_{P2}	M_{N1}, M_{N2}	M_{P4}, M_{P5}	M_{N5}, M_{N6}	M_{SW}	M_{PR}	Capacitors	C_{in}	C_f	C_{hp}	C_c	C_{INT}
W/L (μm/μm)	120/3	15/5	20/3	30/1.5	5/0.18	2/4	Value	9 pF	90 fF	500 fF	12 pF	8 pF

stage is mainly coming from M_{P1}–M_{P2}, M_{N1}–M_{N2}, and M_{P4}–M_{P5}. The cascode transistors do not contribute to noise. The input-referred noise can be calculated by

$$\overline{v_{n,\text{in}}^2} \approx 2\left(\overline{v_{n,p1}^2} + \frac{g_{m,n1}^2}{g_{m,p1}^2}\overline{v_{n,n1}^2} + \frac{g_{m,p4}^2}{g_{m,p1}^2}\overline{v_{n,p4}^2}\right) \tag{19}$$

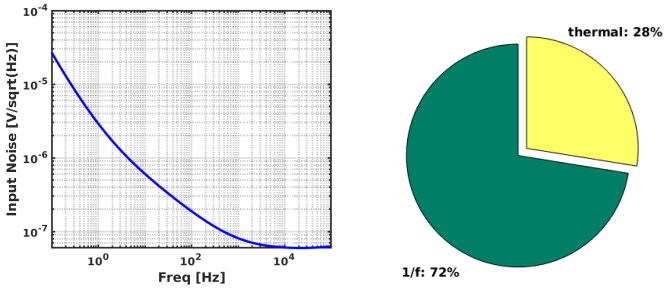
where $\overline{v_n^2}$ is the input-referred noise power spectral density of a MOSFET as given by [32]:

$$\overline{v_n^2} = \frac{4kT\gamma}{g_m}\left(1 + \frac{f_c}{f}\right) \tag{20}$$

for transistors in strong inversion, and

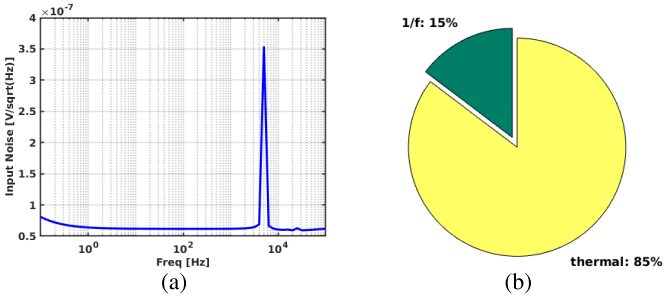
$$\overline{v_n^2} = \frac{2qI_D}{g_m^2} = \frac{2q}{I_D}(nV_T)^2\left(1 + \frac{f_c}{f}\right) \tag{21}$$

for transistors in weak inversion, where $\gamma \approx 2/3$ is the noise coefficient in strong inversion, f_c is the noise corner frequency, q is the electron charge, I_D is the drain current, V_T is the thermal voltage ($V_T \approx 26$ mV at room temperature), and $n \approx 1.5 - 2$ is the subthreshold slope factor. $\overline{v_n^2}$ contains a bias-dependent thermal noise and area-dependent flicker noise, resulting in design trade-offs between noise and power/area. According to (19), the input differential pair is crucial for noise optimization. In this design, input transistors M_{P1} and M_{P2}



(a) (b)

Fig. 11. Simulated noise performance of CCIA. (a) Input-referred noise. (b) Noise breakdown.



(a) (b)

Fig. 13. Simulated noise performance of chopper CCIA. (a) Input-referred noise. (b) Noise breakdown.

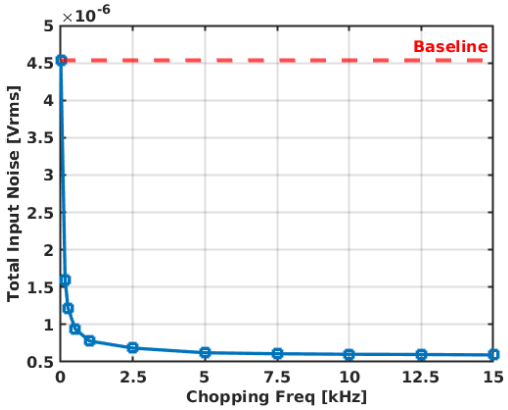


Fig. 12. Relationship between total input noise and f_{chop}.

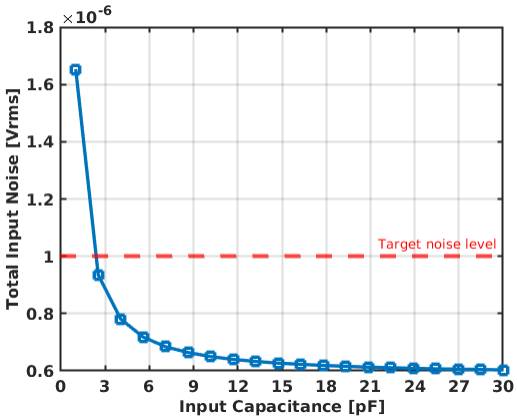


Fig. 14. Relationship between total input noise and C_{in}.

operate in the weak-inversion in order to achieve low-power consumption while maximizing g_m/I_{DS} ratio. M_{N1}–M_{N2} and M_{P4}–M_{P5} operate in strong inversion in order to minimize $g_{m,p4}/g_{m,p1}$ and $g_{m,n1}/g_{m,p1}$ ratios. A detailed design strategy of noise optimization for folded-cascode OTA is out of the scope of this study and has been thoroughly discussed in [33].

The actual noise corner frequency f_c of the core amplifier is obtained through a noise simulation. Fig. 11 shows that f_c is around 1 kHz and the amplifiers achieve an input referred noise of 65 nV/$\sqrt{\text{Hz}}$ while consuming only 1.6 μA from VDDA. The $1/f$ noise is the primary noise contributor within the bandwidth from 1 to 100 Hz as shown in the noise breakdown. To effectively transpose the $1/f$ noise to high frequencies, choppers (CH_{in} and CH_{out}) are applied to the CCIA and the relationship between the simulated integrated input-referred noise and the chopping frequency is shown in Fig. 12. A chopping frequency of 5 kHz is selected as only very modest improvement is achieved for higher frequencies at the expense of much higher power consumption. The simulated noise level and the noise breakdown that corresponds to a chopper CCIA with a chopping frequency of 5 kHz are presented in Fig. 13.

As described in Section III, the noise contribution of VM-DSL is inversely proportional to the value of C_{in}. Fig. 14 presents a circuit simulation result that demonstrates the relationship between total noise and C_{in}. Consequently, a large C_{in} is desirable for noise optimization. In addition, large capacitors are less prone to mismatches, resulting in a higher CMRR. However, these capacitors require considerable silicon area and also degrade the input impedance. In this design, C_{in} is 9 pF so that an input impedance higher than 10 MΩ is achieved with enough margins while achieving the target noise level and CMRR. The value of feedback capacitors is then calculated as 90 fF to provide a 40 dB amplification. The selected value of C_{hp} is 500 fF in order to provide a maximum EDO tolerance of around 100 mV. The high-pass and low-pass cutoff frequencies are determined by the unit-gain bandwidth of the integrator and the value of Miller capacitor C_c, respectively. The integrator is implemented using an area-efficient pseudoresistor-based active RC integrator to achieve a very large time constant, and therefore, an extremely low high-pass cutoff frequency while allowing on-chip integration [34]. Fig. 15 shows the layout implementation of the chopper CCIA with VM-DSL. Fig. 16(a) and (b) presents simulation results of ac characteristics and CMRR, respectively. This design meets the specifications by providing 40 dB amplification within the 1 Hz to 1 kHz range, while also maintaining a low noise level and achieving a CMRR of 106 dB.

D. Circuit Design of a Chopper CBIA With CM-DSL

Fig. 17 presents the circuit implementation of a chopper CBIA with CM-DSL. The core amplifier is composed of a transconductance stage and a transimpedance stage. Detailed device parameters and transistor dimensions are available in Table III. The input differential signal is sensed by the source degeneration resistor R_1, resulting in a signal-dependent current that is translated to output voltage through the impedance $R_2||C_1$. Therefore, the voltage gain of the core amplifier is

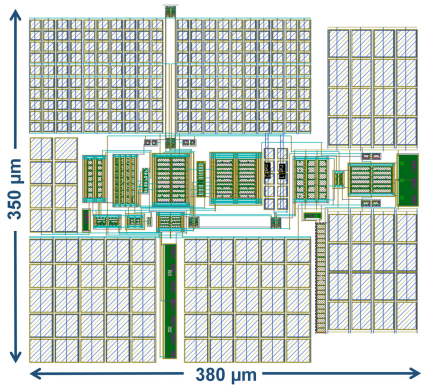


Fig. 15. Layout of chopper CCIA with VM-DSL.

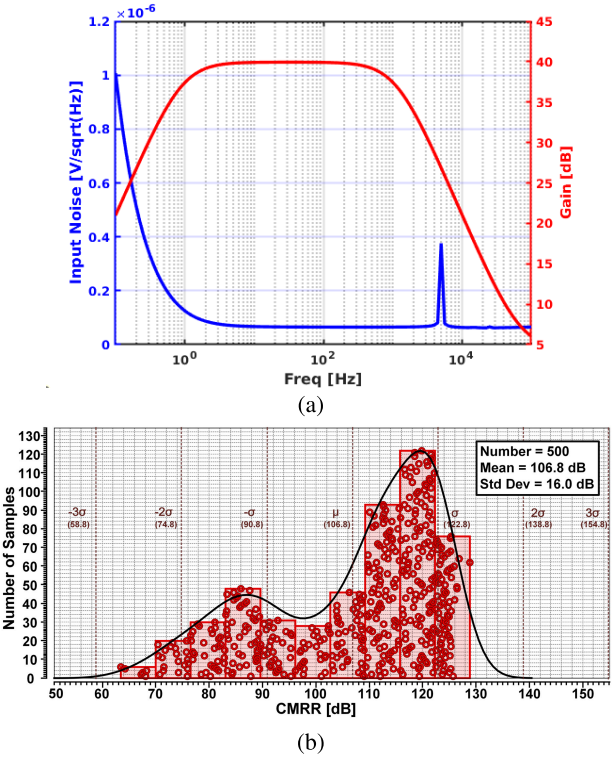


Fig. 16. Simulation results of chopper CCIA with VM-DSL. (a) Input-referred noise and ac response. (b) Histogram of the CMRR over process and device mismatch.

accurately defined by

$$A_{V,\mathrm{CBIA}}(s) \approx K_1 \frac{R_2}{R_1} \frac{1}{1+sR_2C_1} \tag{22}$$

where K_1 is the current mirror ratio, which is 0.4 in this design to reduce the current consumption. The input-referred noise of this circuit architecture is derived by

$$\overline{v_{n,\mathrm{in}}^2} \approx 2\overline{v_{n,p1}^2} + 4KT\left(R_1 + \frac{R_1^2}{R_2}\right) + 2\frac{g_{m,n2}^2}{g_{m,p1}^2}\overline{v_{n,n2}^2} + 2\frac{g_{m,p3}^2}{g_{m,p1}^2} \times \left(\overline{v_{n,p3}^2} + \overline{v_{n,p4}^2} + \overline{v_{n,p5}^2} + \frac{g_{m,n5}^2}{g_{m,p5}^2}\overline{v_{n,n5}^2} + \frac{g_{m,p9}^2}{g_{m,p4}^2}\overline{v_{n,p9}^2}\right). \tag{23}$$

The noise level is mainly dominated by the input differential pair and the thermal noise of R_1. To minimize the noise contributed by other devices, the trade-off can be made between current consumption and $g_{m,p1}$. From a noise performance point of view, the value of R_1 should be minimized. However, R_1 is also related to the maximum EDO tolerance as calculated in (5). Consequently, the choice of R_1 requires a compromise with power consumption. In this implementation, the value of R_1 and the biasing current for the input pair are chosen as 25 kΩ and 2.5 μA such that they approximately have the same thermal noise contribution as calculated by

$$2\frac{2qI_D}{g_{m,p1}{}^2} = \frac{4q}{I_D\left(\frac{g_{m,p1}}{I_D}\right)^2} = 4KTR_1. \tag{24}$$

The value of g_m/I_{DS} is around 21 when the pMOS is working in the weak-inversion region in this CMOS technology. To provide a 40 dB amplification, the value of R_2 is then determined to 6.25 MΩ.

Next, a noise simulation is conducted in order to find the $1/f$ corner frequency f_c and select the chopping frequency. The chopping frequency is selected as 5 kHz to make the $1/f$ noise negligible within the signal bandwidth.

The CM-DSL contains an integrator to extract the dc component of the output and a transconductance stage to perform the current-to-voltage conversion. The design of CM-DSL is critical to define the high-pass cutoff frequency, EDO tolerance, and also noise performance. The implementation of the integrator is the same as the one used previously in the VM-DSL. The transconductance stage is implemented using a source-degenerated differential amplifier to accurately define its equivalent G_m by the choice of R_3. Its output stage is designed to provide a maximum I_{DSL} of 2 μA to achieve around 50 mV EDO tolerance. In this architecture, the high-pass cut-off frequency is determined by

$$f_{\mathrm{hp}} = K_1K_2\frac{R_2}{R_3}\frac{1}{2\pi R_{\mathrm{PR}}C_{\mathrm{INT}}}. \tag{25}$$

Therefore, the time constant of the integrator and the value of R_3 require proper sizing in order to reach very low cut-off frequencies.

As described in Section II, there are two possible topologies that can be implemented: topology I by placing $\mathrm{CH}_{\mathrm{DSL}}$ at the output of the DSL (green chopper), or topology II by placing $\mathrm{CH}_{\mathrm{DSL}}$ at the intermediate point between the integrator and the transconductance (brown chopper) as shown in Fig. 17. To demonstrate the impact of the placement of the chopper, Fig. 18(a) shows three different Pnoise simulations that were performed on this amplifier: first the chopper was totally deactivated, then chopper was connected as in topology I, and finally the chopper was connected as in topology II. Fig. 18(b) presents the total input-referred noise within 1 to 100 Hz bandwidth of each topology and also compares the corresponding noise breakdown. The noise of the amplifier without chopping modulation is relatively high in the low-frequency range due to the $1/f$ noise from both the CBIA and the CM-DSL. In this design, the noise can be reduced by around 36% when the chopping technique is applied to the CBIA and the CM-DSL is

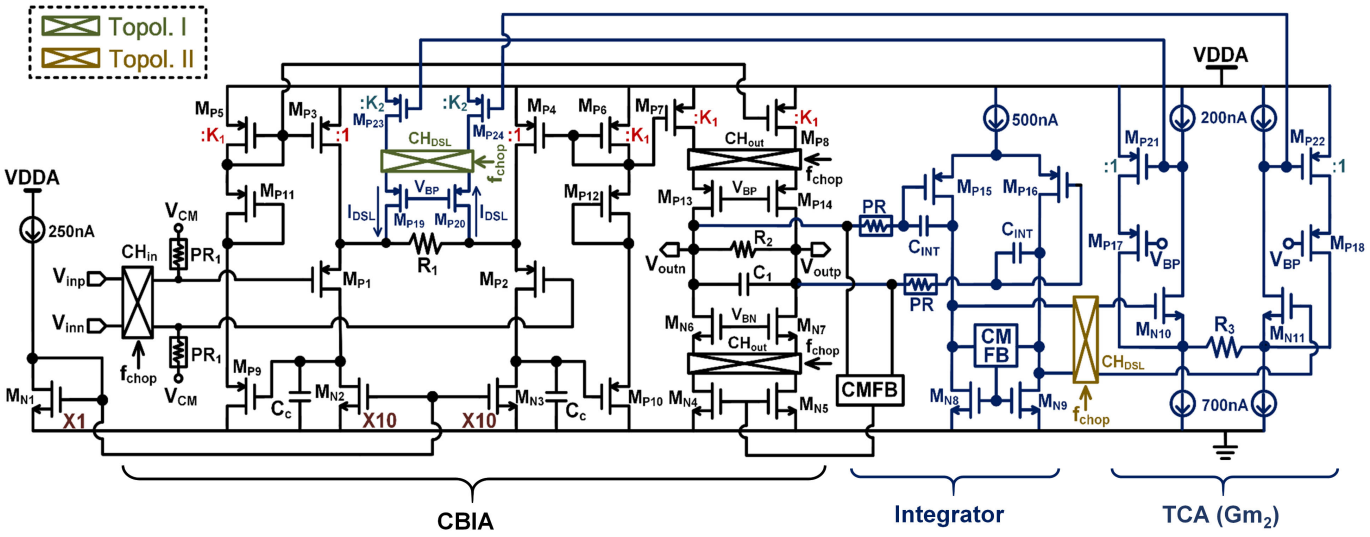
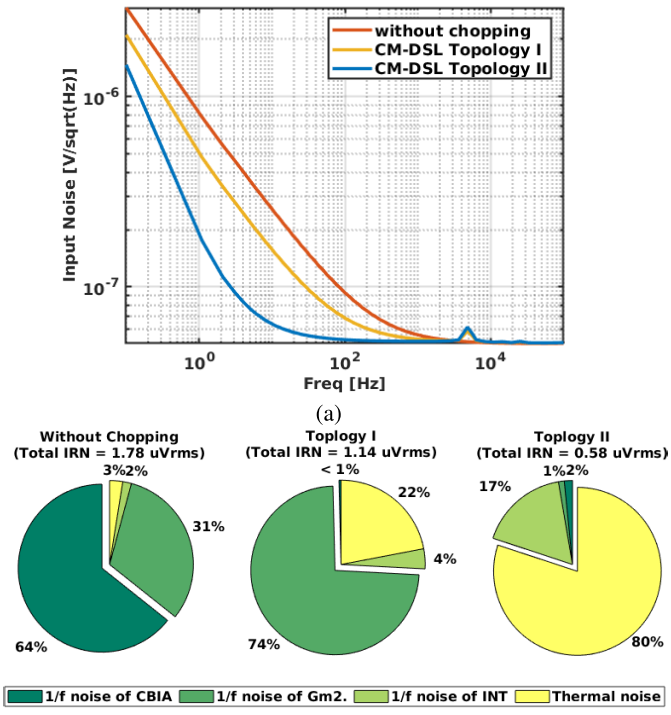


Fig. 17. Schematic of chopper CBIA with CM-DSL topology I (green chopper)/topology II (brown chopper).

TABLE III
DEVICE PARAMETERS AND DIMENSIONS OF TRANSISTORS IN FIG. 17

Transistors	M_{P1}, M_{P2}	M_{P3}, M_{P4}	$M_{P5} - M_{P8}$	M_{P9}, M_{P10}	M_{P15}, M_{P16}	M_{P21}, M_{P22}	M_{P23}, M_{P24}	M_{N2}, M_{N3}	M_{N10}, M_{N11}
W/L (μm/μm)	120/3	50/5	25/5	40/2	150/3	20/3	80/3	80/12	80/2
Passives	R_1	R_2	R_3	C_c	C_1	C_{INT}			
Value	25 kΩ	6.25 MΩ	60 kΩ	1 pF	20 pF	10 pF			



(a)

(b)

Fig. 18. Simulated noise performance of CBIA with CM-DSL implemented using different topology. (a) Input-referred noise. (b) Total input-referred noise and noise breakdown.

configured as topology I. In this topology, the $1/f$ noise of the CBIA is suppressed significantly because of the upmodulation process, but the $1/f$ noise of the Gm_2 stage and the integrator within the feedback loop still remain at low frequencies. In order to further improve the noise performance, the chopper in the DSL is placed in front of the Gm_2 stage as shown in the circuit topology II. As we have derived in (16), the $1/f$ noise of the Gm_2 stage is not visible at baseband by using topology II, and therefore the major $1/f$ noise contributor is from the integrator. The primary noise contributor is the thermal noise, which can be further reduced by increasing biasing current. As a result, an additional 49% reduction in total integrated noise is reached under the condition that identical circuit blocks are used. According to this comparison, topology II is chosen in this design as it offers the lowest noise level.

It can be observed from the noise breakdown that the $1/f$ noise of the integrator becomes a critical noise contributor in topology II. For further noise optimization, it is of great importance to understand how this noise source affects the overall noise level. As we have derived in (17), the extent of the impact of the integrator's noise on the total noise is related to the transconductance of the Gm_2 stage. Fig. 19 presents a circuit simulation result that shows the relationship between the total input-referred noise and Gm_2 by sweeping the value of R_3. Due to the fact that $Gm_2 = K_2/R_3$, it is desired to maximize the value of R_3 for better noise performance at the expense of area. However, in this case, only marginal improvement can be obtained when the Gm_2 is less than 10 μS. Considering the area-noise design trade-off, the Gm_2 stage is designed to offer a transconductance of 10 μS for reaching a better area efficiency. Fig. 20 shows the layout implementation of a chopper CBIA with CM-DSL. Finally, Fig. 21 presents the ac response, noise performance and CMRR, respectively. It can be seen that this architecture also offers

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART BIOPOTENTIAL AMPLIFIERS

	Example Designs*		TCAS-II'22 [6]	JSSC'18 [15]	TIM'21 [17]	SSCL'18 [23]
CMOS Technology (nm)	180		180	65	180	65
Supply Voltage (V)	1.8		1	1.2	1.8	0.6
Current Consumption (μA)	2.1	7.7	1.85	4.5	7.6	5.3
DSL Method	VM-DSL	CM-DSL	VM-DSL	VM-DSL	CM-DSL	CM-DSL
Input Capacitor (pF)	9	none	10	32	none	none
Electrode Offset Tolerance (mV)	100	50	90	300	250	50
Voltage Gain (dB)	40	40	40	40	40	N/A
3dB-Bandwidth (Hz)	1 - 1000	1 - 1000	1 - 640	0.5 - 250	0.45 - 170	500
Total Input-referred Noise (μVrms)	0.66 (1-100Hz)	0.59 (1-100Hz)	1.16 (0.5-100Hz)	0.44 (0.5-100Hz)	3.8 (0.45 - 100Hz)	2.2 (1-500Hz)
Noise Efficiency Factor	3.75	6.42	6.18	3.59	39	8.7
CMRR (dB) @ 50/60Hz	106	120	>95	>110	120	77
Input Impedance (Ω)	10.02M @60Hz	64.34M @60Hz	250M @10Hz	1G @60Hz	>100M @60Hz	500M @100Hz
Area (mm^2)	0.13	0.085	0.183†	N/A	0.074	0.08

* Simulation results. † The area is estimated from the chip micrography.

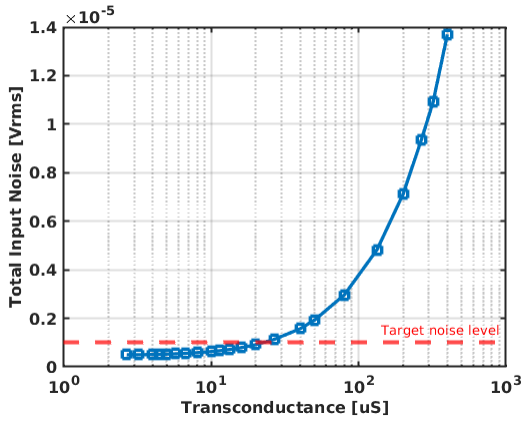


Fig. 19. Relationship between total input noise and Gm_2.

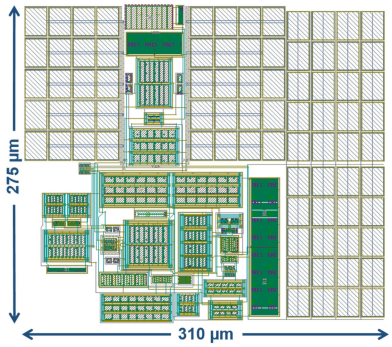


Fig. 20. Layout of chopper CBIA with CM-DSL.

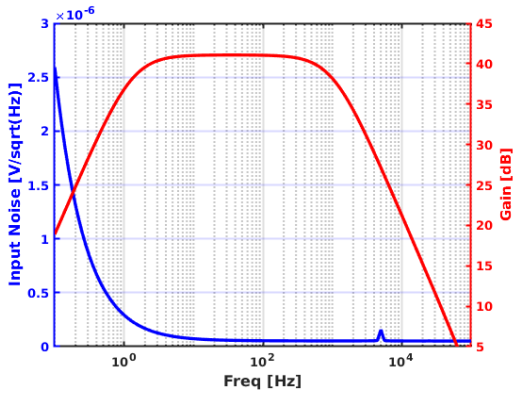


Fig. 21. Simulation results of chopper CBIA with CM-DSL. (a) Input-referred noise and ac response. (b) Histogram of the CMRR over process and device mismatch.

desired ac-coupling characteristics while maintaining a low noise level and achieving a CMRR of 121 dB.

V. DISCUSSION

Table IV summarizes the performance of the example biopotential chopper amplifiers with VM-DSL or CM-DSL and also makes a comparison with prior art biopotential amplifiers. Typically, the noise efficiency factor (NEF) is used as a performance metric to compare the noise performance of an amplifier. NEF is defined as [25]

$$\mathrm{NEF} = v_{\mathrm{rms,in}}\sqrt{\frac{2 \cdot I_{\mathrm{tot}}}{\pi \cdot V_T \cdot 4KT \cdot \mathrm{BW}}} \tag{26}$$

where $V_{\mathrm{rms,in}}$ is the total input-referred noise rms value within the bandwidth, I_{tot} is the total current consumption, V_T is the thermal voltage, K is Boltzmann's constant, T is the absolute temperature, and BW is the 3 dB-bandwidth of an amplifier. This factor reflects how closely the amplifier

approaches an ideal BJT, which has a NEF of 1. Compared to CM-DSL, VM-DSL implementations generally exhibit higher NEF since they do not require an additional transconductance stage for EDO subtraction. The additional transconductance adds current consumption which is proportional to the amplitude of the EDO. For this reason, the EDO tolerance is typically limited to tens of millivolt. To address this issue, a dual-branch current-feedback CBIA [35] has been proposed to offer a wider range of EDO tolerance.

The major drawback of the VM-DSL is the necessity of a relatively large capacitor which is not amenable to integration in systems that require multiple recording channels. For this reason, the number of channels is commonly less than eight in system-on-chip (SoC) designs unless special multichannel multiplexing techniques such as digitally assisted time-division multiple access (TDMA) [36] and dual-channel charge recycled (DCCR) [37] are utilized to share hardware.

Although chopping helps attenuate $1/f$ noise, it effectively reduces Z_{in} owing to the switched-capacitor resistor formed by the input chopper and the large-value input capacitors. As a result, Z_{in} is commonly less than 10 MΩ in chopper VM-DSL architecture, which is acceptable for general biosensing applications over the skin where relatively large electrodes are used, but it may not be acceptable in deep brain recording implants [38]. Consequently, additional circuit techniques that boost the input impedance may need to be applied in order to mitigate the loading effect and also achieve the required CMRR performance [3], [4], [5], [6], [13], [14], [15].

In contrast, CM-DSL can easily achieve higher CMRR and be more robust against device mismatch due to the fact that it does not depend on the matching of passive devices. Additionally, the input impedance is not severely affected by the chopper, therefore making it suitable as an interface with a broad type of electrodes without the need for an additional input impedance boosting circuitry. However, it is crucial to investigate the noise contribution from the DSL as it may have a considerable contribution to the total noise at low frequencies. Therefore, its noise modeling and mitigation strategies are important for circuit design. In particular, the exact placement of the chopper within the DSL is of paramount importance as significant noise reduction can be achieved.

VI. Conclusion

This article has presented a comprehensive noise analysis and modeling of two circuit architectures extensively used in biopotential acquisition front-ends: the chopper-based charge-balancing IA with current-mode DSL and the chopper-based capacitively coupled IA with voltage-mode DSL. Our investigation has specifically focused on the impact of analog DSL implementations on noise performance, and we have presented and discussed the associated design considerations and trade-offs. Furthermore, we have proposed a design methodology for noise optimization, which we have successfully applied in two example circuits designed in 180 nm CMOS. The simulation results, after parasitic extraction, show that these circuits have the potential to achieve similar or even better performance than the prior art. These results provide strong evidence that the proposed noise modeling and design methodology can be effectively employed in the development of fully integrated, low-power, low-noise biopotential amplifiers.

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