

# Corrections to “Hybrid Signed Convolution Module With Unsigned Divide-and-Conquer Multiplier for Energy-Efficient STT-MRAM-Based AI Accelerator”

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**I**N THE above article [1], the reference numbers [10], [11], [12], and [13] in Table II were not correct and should be changed to [11], [12], [13], and [14]. The correct Table II is illustrated as follows.

TABLE II  
COMPARISON WITH THE STATE-OF-THE-ART ACCELERATORS II

Parameters	This Work		[11]	[12]	[13]	[14]	
Process (nm)	55		65	65	65	65	
Voltage (V)	1.2		1.2	0.9	1.0	1.2	
Frequency (MHz)	200		200	204	250	200	
Power (mW)	25.86		165.3	274	278	88.6	
$N_{mul}$	9	18	36	64	256	168	64
$L_W$	16	16	8	16	16	16	16
$L_F$	16	8	8	16	16	16	16
Average Power (mW)	2.87	1.44	0.72	2.58	1.07	1.65	1.38
Core Area (mm <sup>2</sup> )	0.04	0.04	0.04	8	2.4	12.25	10.56
Average Area (mm <sup>2</sup> )	0.0044	0.0022	0.0011	0.125	0.009375	0.0729	0.165

note:  $N_{mul}$ —number of multiplication,  $L_W$ ,  $L_F$ —bit length of weight and feature map

## REFERENCES

- [1] T. Li, Y. Ma, K. Yoshikawa, and T. Endoh, “Hybrid signed convolution module with unsigned divide-and-conquer multiplier for energy-efficient STT-MRAM-based AI accelerator,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, early access, Feb. 22, 2023, doi: [10.1109/TVLSI.2023.3245099](https://doi.org/10.1109/TVLSI.2023.3245099).

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