IEEE Journal of Microwaves

Received 13 June 2022; revised 11 August 2022; accepted 24 August 2022. Date of publication 15 September 2022; date of current version 7 October 2022.

Digital Object Identifier 10.1109/JMW.2022.3202854

High Power InP/Ga(In)AsSb DHBTs for Millimeter-Wave PAs: 14.5 dBm Output Power and 10.4 mw/μm^2 Power Density at 94 GHz

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(Regular Paper)

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ABSTRACT We report the 94 GHz large-signal load-pull performance of (0.3 × 9) μm^2 InP/Ga(In)AsSb double heterojunction bipolar transistors (DHBTs) in the common-emitter (CE) and common-base (CB) configurations. Both configurations were implemented side-by-side on either 20-nm-thick graded GaAsSb- or GaInAsSb-base layers. A measured record saturated output power $P_{OUT,SAT}$ = 14.5 dBm with a corresponding power density 10.4 mW/μm^2 were achieved in the GaInAsSb-base CB configuration. The performance follows from *i*) the higher power gain in the CB topology and, *ii*) the superior BV_{CEO} and BV_{CBO} breakdown voltages obtained with the quaternary base which allow degradation-free operation at higher voltages. Load-pull contours show a combination of high output power and power gain in the proximity of 50 Ω for a wide range of load impedances. In contrast, CB InP/GaAsSb DHBTs deliver $P_{OUT,SAT}$ = 10.6 dBm and 4.3 mW/μm^2. For all devices considered here, CB operation improves transistor robustness against high-power device degradation. The present work provides the first report on the power performance of quaternary InP/GaInAsSb DHBTs in CE/CB topologies, with comparison to ternary InP/GaAsSb DHBTs.

INDEX TERMS InP/Ga(In)AsSb, double heterojunction bipolar transistors (DHBTs), common-emitter (CE), common-base (CB), load-pull measurements, maximum output power, power gain, power density.

I. INTRODUCTION

Interest in millimeter-wave frequencies for high data rate wireless communication, high-resolution imaging, and radar applications grows rapidly. Transistor technologies featuring high cut-off frequencies and high output power levels are required to successfully exploit this frequency regime.

III-V compound semiconductors such as GaAs, GaN, and InP offer high power handling capabilities as well as rising cut-off frequencies thanks to continued R&D activities. Among compound transistor technologies, "Type-II" double heterojunction bipolar transistors (DHBTs) based on the InP-Ga(In)AsSb material system provide the highest $f_T \times BV_{CEO}$ and $f_{MAX} \times BV_{CEO}$ products, as well as the highest f_{MAX} in a bipolar transistor [1], [2]. Quaternary InP/GaInAsSb DHBTs also achieved the highest f_T ever realized in a transistor [3]. The "Type-II" band alignment eliminates the need for grading at the base collector heterojunction [4], allowing the use of a pure InP collector which increases the breakdown voltage and collector thermal conductivity.

The attractive combination of high cut-off frequency and high breakdown voltage in suggests "Type-II" DHBTs should be well-suited to the development of power amplifiers (PAs) operating at very high frequencies. The bias conditions conducive to peak small-signal performance metrics (f_T/f_{MAX}) are however generally not the same as those used in PA applications.

The characterization of DHBT variants under large-signal excitation (generally, via load-pull measurements) is then essential to accurately model transistor behavior in

TABLE 1. Epitaxial Layer Structure of InP/GaAsSb DHBT

Material	Doping (cm^{-3})	Thickness
$Ga_{0.25}In_{0.75}As$	Si: 3.8×10^{19}	5 nm
$Ga_{0.47}In_{0.53}As \rightarrow Ga_{0.25}In_{0.75}As$	Si: 3.8×10^{19}	10 nm
$Ga_{0.47}In_{0.53}As$	Si: 3.8×10^{19}	20 nm
InP	Si: 1.5×10^{19}	130 nm
InP	Si: 2.5×10^{16}	5 nm
$Ga_{0.22}In_{0.78}P \rightarrow InP$	Si: 2.5×10^{16}	10 nm
$Ga_{0.22}In_{0.78}P$	Si: 2.5×10^{16}	5 nm
$GaAs_{0.41}Sb_{0.59} \rightarrow GaAs_{0.58}Sb_{0.42}$	C: 8.6×10^{19}	20 nm
InP	Si: 9.1×10^{16}	125 nm
InP	Si: 2.8×10^{19}	50 nm
$Ga_{0.47}In_{0.53}As$	Si: 3.0×10^{19}	20 nm
InP	Si: 2.8×10^{19}	300 nm
InP semi-insulating substrate		350 μm

TABLE 2. Epitaxial Layer Structure of InP/GaInAsSb DHBT

Material	Doping (cm^{-3})	Thickness
	Si: 3.8×10^{19}	5 nm
$Ga_{0.47}In_{0.53}As \rightarrow Ga_{0.25}In_{0.75}As$	Si: 3.8×10^{19}	10 nm
$Ga_{0.47}In_{0.53}As$	Si: 3.8×10^{19}	20 nm
InP	Si: 1.5×10^{19}	130 nm
InP	Si: 2.5×10^{16}	5 nm
$Ga_{0.20}In_{0.80}P \rightarrow InP$	Si: 2.5×10^{16}	10 nm
$Ga_{0.20}In_{0.80}P$	Si: 2.5×10^{16}	5 nm
$Ga_{0.83}In_{0.17}As_{0.62}Sb_{0.38} \rightarrow Ga_{0.94}In_{0.06}As_{0.70}Sb_{0.30}$	C: 5.6×10^{19}	20 nm
InP	Si: 9.1×10^{16}	125 nm
InP	Si: 2.8×10^{19}	50 nm
$Ga_{0.47}In_{0.53}As$	Si: 3.0×10^{19}	20 nm
InP	Si: 2.8×10^{19}	300 nm
InP semi-insulating substrate		350 μm

high-frequency PA circuit design. However, the literature provides relatively few reports of load-pull characterization at frequencies of 94 GHz and higher [5], [6], [7], [8]. While circuits are also desired at frequencies much above W-band, 94 GHz load-pull measurements provide an excellent opportunity to validate device models for PA design.

Whereas InP/GaAsSb DHBTs have already demonstrated attractive power performances [2], [9], the large-signal properties of quaternary-based InP/GaInAsSb DHBTs have not previously been studied: the present work characterizes quaternary (0.3×9) μm^2 DHBTs in the common-emitter (CE) and common-base (CB) configurations, and contrasts them to those of conventional InP/GaAsSb DHBTs with a ternary base.

Among other findings, we report GaInAsSb-based DHBTs with a record maximum saturation output power $P_{OUT,\,SAT} =$ 14.5 dBm and a 10.4 mW/μm^2 power density at 94 GHz. To the best of our knowledge, these are the highest *measured* $P_{OUT,SAT}$ and output power density reported for InP bipolar transistors at W-band. We emphasize that the present results were obtained without thermal management techniques (*e.g.*, heatsinking or substrate thinning/transfer), and that further improvements can be expected with the application of backside processing techniques.

II. DEVICE TECHNOLOGY AND FABRICATION

The present DHBT epitaxial layers were grown by Metal-Organic Vapor-Phase Epitaxy (MOVPE). The epitaxial layer stacks are detailed in Tables 1 and 2. In both cases the emitter region consists of a lightly doped graded InP/GaInP composite structure that eliminates the conduction band offset at the E/B interface. DHBTs with GaAsSb- and GaInAsSb- base layers are contrasted in this work. Both maintain a "Type-II" band alignment with the InP collector although, as described below, only marginally so for the GaInAsSb base.

A. INP/GAASSB DHBT TECHNOLOGY

The epitaxial layer structure is described in Table 1. The 20-nm-thick $GaAs_xSb_{1-x}$ base incorporates both compositional and dopant gradings to accelerate electron transport in the base. The As-mole fraction is graded from $x = 0.58$ at the emitter side to $x = 0.41$ at the collector side.

The *p*-doping is graded linearly with an average of 8.6×10^{19} cm^{-3}. Both gradings produce an aiding drift field to assist electron transport across the base layer. The $GaAs_{0.41}Sb_{0.59}$ composition at the base-collector junction results in Type-II alignment with the base conduction band edge $\Delta E_C \approx 0.16$ eV higher than the InP conduction band [10].

B. INP/GAINASSB DHBT TECHNOLOGY

The electron minority carrier mobility in *p*-type GaAsSb is lower than in GaInAs due to the population of its L-valley [11]. The base transport properties of InP/GaAsSb DHBTs can be improved by adding In- to the GaAsSb alloy to form a quaternary GaInAsSb base with an increased Γ-L valley separation. Recent work demonstrated that GaInAsSb indeed shows higher 300 K electron mobilities than GaAsSb at a given electron concentration [12]. The use of a compositionally graded GaInAsSb base in DHBTs was shown to improve electron injection efficiency into the InP collector [13].

The epitaxial layer structure is detailed in Table 2. The 20-nm-thick $Ga_{1-x}In_xAs_ySb_{1-y}$ base is compositionally graded from $(x, y) = (0.06, 0.70)$ on the on the emitter side to (0.17, 0.62) on the collector side of the base. The base layer is carbon *p*-doped with a linear grading from 3.1×10^{19} cm^{-3} on the collector side to 8.1×10^{19} cm^{-3} on the emitter side, for an average of 5.6×10^{19} cm^{-3}. Our calculations show that for these compositions the GaInAsSb conduction band is nearly aligned to that of InP (*i.e.*, $\Delta E_C \sim 0$ eV) at the base-collector junction. Because the GaInAsSb energy gap is essentially independent of composition when lattice-matched to InP [14], the energetic separation between the GaInAsSb valence band and the InP conduction band is increased in contrast to the GaAsSb/InP case. This leads to significantly higher

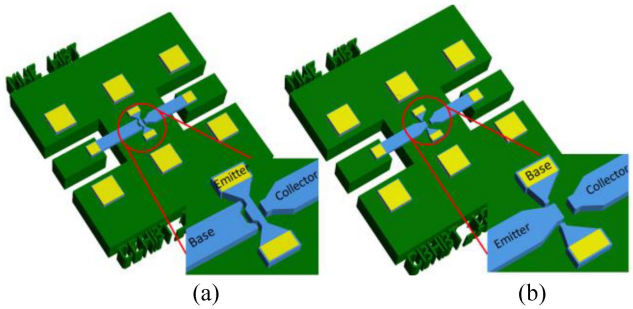

FIGURE 1. GSG co-planar probe pad layout of a DHBT with (a) common-emitter and (b) common-base configuration.

breakdown voltages in InP/GaInAsSb DHBTs by reducing interband tunneling at the base/collector heterojunction.

C. DEVICE FABRICATION

DHBTs with a (0.3 × 9) μm^2 emitter-base area were fabricated side-by-side in a self-aligned standard triple mesa process where the emitter and base contacts are patterned by electron beam lithography. The base contact metallization consists of an e-beam evaporated refractory Pt/Ta/Pt/Au stack intended to minimize metal diffusion into the base in the high temperature curing cycle of the benzo-cyclo-butene (BCB) planarization.

The self-aligned emitter and base mesas were formed by a combination of dry and wet etching. The collector contact was next defined by photolithography, and deposited by electron beam evaporation. Two GaInAs/InP wet etching cycles were performed to isolate transistors. A 250 °C BCB based etch-back planarization completes device fabrication and supports the electron-beam evaporated co-planar ground-signal-ground (GSG) probing pads.

D. COMMON-BASE & COMMON-EMITTER CONFIGURATIONS

DHBTs were fabricated with common-emitter (CE) and common-base (CB) probe pad layouts. Fig. 1(a)) shows the GSG pad layout of a CE structure with a grounded emitter and the base and collector as the input and output ports, respectively. The CB structure is formed using the pad layout of Fig. 1(b)) with a grounded base, and emitter and collector as the input and output ports, respectively.

III. DEVICE CHARACTERIZATION

A. DC AND SMALL-SIGNAL MEASUREMENTS

The emitter-base junction area of (0.3 × 9) μm^2 in the present DHBTs was verified by electron microscopy. The device static performance was measured on an HP4156B parameter analyzer. Typical common-emitter I_C-V_{CE} and Gummel characteristics of InP/GaAsSb and InP/GaInAsSb DHBTs are shown in Fig. 2. The open-base common-emitter and the open-emitter collector-base breakdown characteristics were measured to determine the BV_{CEO} and BV_{CBO} for each technology, respectively.

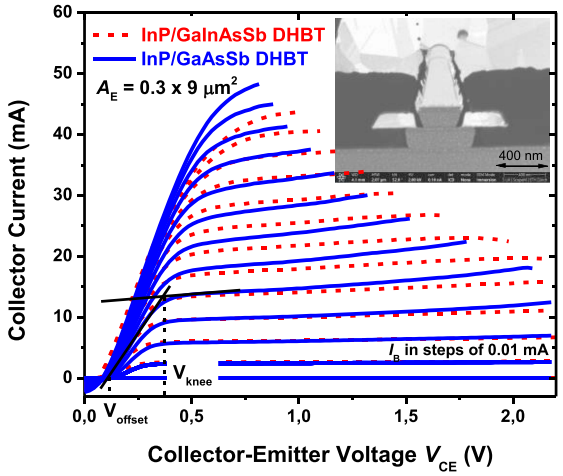

FIGURE 2. DHBT common-emitter *I-V* curves for GaAsSb- (solid line) and GaInAsSb- (dashed line) based technologies. The emitter-base junction area is (0.3 × 9) μm^2 in both cases.

TABLE 3. Static Parameters of (0.3 x 9) μm^2 GaAsSb- and GaInAsSb-Based DHBT

Quantity	InP/GaAsSb	InP/GaInAsSb
Offset Voltage [a] (V)	0.1	0.1
Knee Voltage [b] (V)	0.37	0.4
BV_{CEO} [c] (V)	4.4	5.3
BV_{CBO} [d] (V)	5.1	7.3
Maximum Current Gain (β)	22	25

[a] the voltage at which I_C becomes positive
[b] the intersection of linear fits to I_C in the active region and the saturation region
[c] defined at J_C = 1 kA/cm^2 with the base open-circuited
[d] defined at J_C = 1 kA/cm^2 with the emitter open-circuited

The RF small-signal performance was measured from 0.2 to 50 GHz using a PNA-X vector network analyzer with off-wafer line-reflect-reflect-match (LRRM) calibrations using an impedance standard substrate (ISS). Using the open-short de-embedding technique, Mason's unilateral power gain U, MAG/MSG, and the common-emitter short-circuit current gain $|h_{21}|^2$ (only for the CE configuration) were extracted from the measured *S*-parameters.

B. LARGE-SIGNAL MEASUREMENTS

Power measurements were conducted using the 94 GHz active load-pull system described in [15], where the load impedance is generated by an active loop exploiting frequency conversion techniques. The input is a single tone continuous wave (CW) signal.

IV. RESULTS AND DISSCUSION

A. DC PERFORMANCE

Representative common-emitter *I-V* characteristics for 9 μm long devices in both technologies are plotted in Fig. 2. The offset and knee voltages are listed in Table 3: both the ternary and quaternary DHBTs show similar knee and offset voltages. Fig. 3 shows Gummel characteristics measured with V_{CB} =

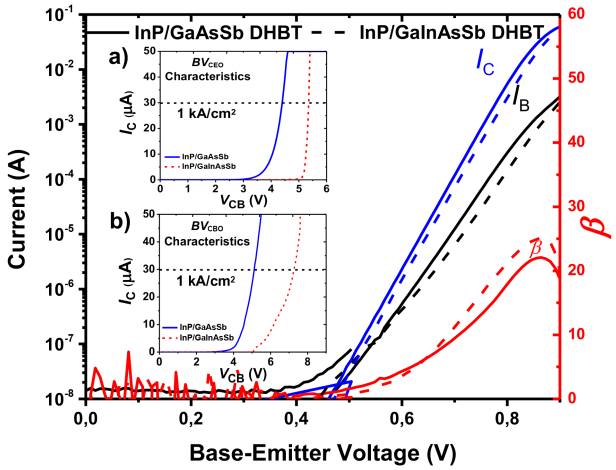

FIGURE 3. Gummel characteristics at $V_{CB} = 0$ V for a DHBT with an emitter-base junction area of (0.3 × 9) μm² for GaAsSb- and GaInAsSb-based technology. Inset: (a) corresponding open-base common-emitter breakdown characteristics for BV_{CEO} measurement and (b) corresponding open-emitter collector-base breakdown characteristics for BV_{CBO} measurement.

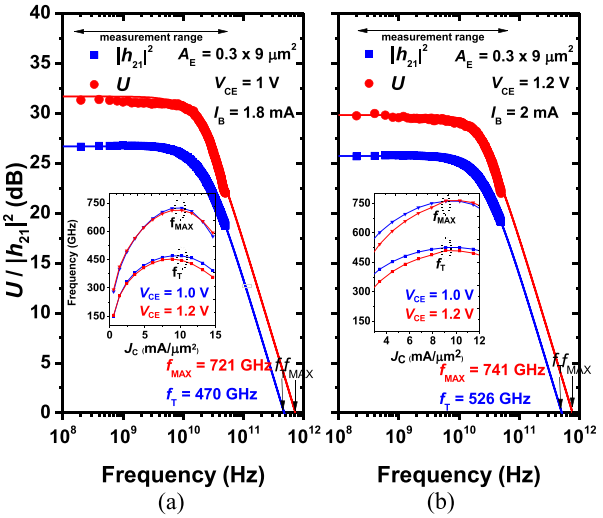

FIGURE 4. Short-circuit current gain $|h_{21}|^2$ and Mason's unilateral gain U measured between 0.2 and 50 GHz for (a) InP/GaInAsSb DHBT and (b) InP/GaAsSb DHBT. f_T and f_{MAX} are extrapolated from single pole transfer function fits. (Inset) dependence of f_T and f_{MAX} on the collector current density at $V_{CE} = 1$ and 1.2 V.

0 V. The maximum common-emitter current gains for the ternary and quaternary base are $\beta = 22$ and 25, respectively. In the Fig. 3. inset, the open-base collector breakdown is determined at $J_C = 1$ kA/cm² to define BV_{CEO}. The resulting values are reported in Table 3, along with the corresponding collector-base breakdown voltages BV_{CBO}.

Significant differences between the breakdown voltages of GaAsSb- and GaInAsSb-based DHBTs are observed. As both GaAsSb and GaInAsSb DHBTs show similar gains, the BV_{CEO} improvement observed with GaInAsSb does not arise from gain (β being slightly higher for GaInAsSb). The 43% improvement in BV_{CBO} with GaInAsSb is consistent with reduced interband tunneling associated with the smaller ΔE_C at the GaInAsSb-InP heterojunction as described in [16]. The higher breakdown voltages of InP/GaInAsSb DHBTs are shown to improve large-signal performance below.

B. SMALL-SIGNAL PERFORMANCE

The DHBT small-signal cut-off frequencies were determined using the open-short de-embedding procedure and single-pole fits to $|h_{21}|^2$ and $U(f)$. Fig. 4 shows measured data and fits (using the entire measurement frequency range) and resulting extrapolations to f_T/f_{MAX} for both technologies in the CE configuration. The short-circuit CE current gain $|h_{21}|^2$ and Mason's unilateral gain U determined between 0.2 and 50 GHz for (a) InP/GaInAsSb and (b) InP/GaAsSb DHBTs.

A simultaneous peak $f_T/f_{MAX} = 470/721$ and 526/741 GHz for 9-μm-long GaAsSb- and GaInAsSb-based DHBTs are achieved, respectively. The current density at peak f_T/f_{MAX} is 9 and 10 mA/μm² for GaAsSb- and GaInAsSb- based DHBTs, respectively. The collector current dependence of f_T and f_{MAX} for $V_{CE} = 1$ and 1.2 V is shown in the insets of Fig. 4(a)) and (b)).

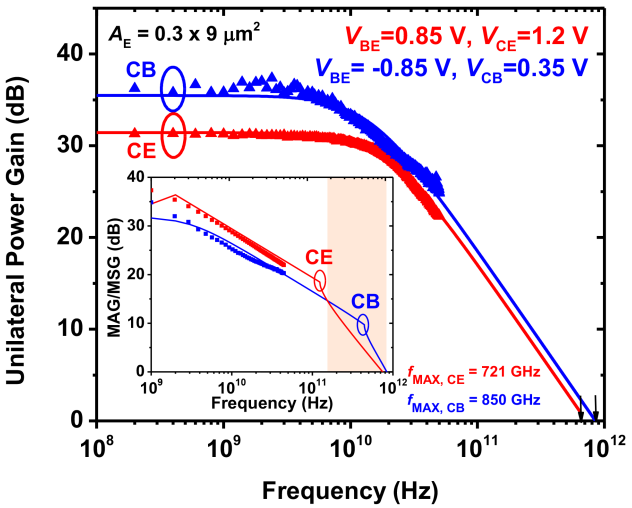

FIGURE 5. Mason's unilateral gain U measured between 0.2 and 50 GHz in CE InP/GaAsSb DHBT at a bias of $V_{BE} = 0.85$ V and $V_{CE} = 1.2$ V and CB at a bias of $V_{BE} = -0.85$ V and $V_{CB} = 0.35$ V. f_{MAX} is extrapolated from single pole transfer function fit. (Inset) simulated MAG/MSG for the corresponding devices based on HiCuM/L2 InP/GaAsSb HBT model.

The f_T improvement for InP/GaInAsSb DHBTs was described [13]. The use of GaInAsSb quaternary base alloys was shown to improve the transport in the base layer and increase the percentage of electrons that quickly leave the base layer by reducing L-valley population effects [13].

Fig. 5 plots the unilateral power gain of CE and CB ternary DHBTs at the same collector current density. Peak f_{MAX} values of 721 and 850 GHz for 9-μm-long GaAsSb-based CE and CB DHBTs are extracted by single-pole fits and extrapolation at –20 dB/dec, respectively. Small-signal simulations based on the scalable InP/GaAsSb HiCuM/L2 model from [17] for the CE and CB configurations provide

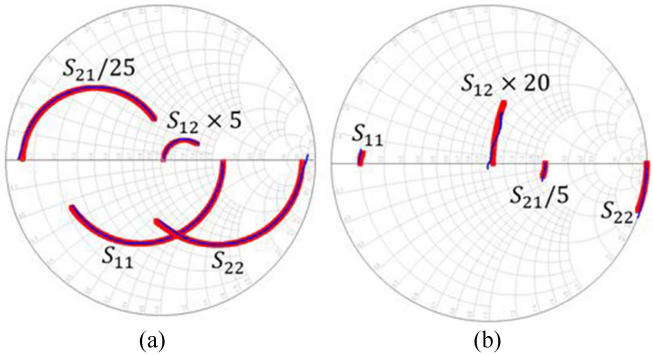

FIGURE 6. Measured (blue) and simulated (red) S-parameters of (0.3 × 9) μm^2 for (a) GaAsSb-based CEHBT at $V_{BE} = 0.85$ V and $V_{CE} = 1.2$ V; and (b) GaAsSb-based CBHBT at $V_{BE} = -0.85$ V and $V_{CB} = 0.35$ V. Simulations are based on the HiCuM/L2 InP/GaAsSb HBT model.

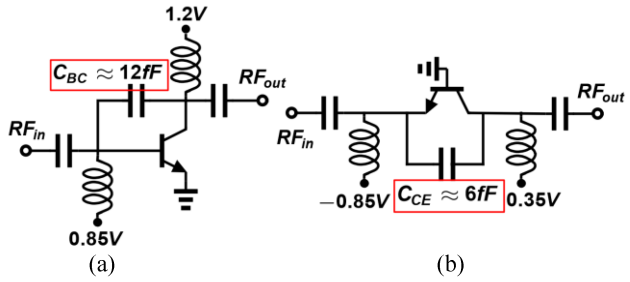

FIGURE 7. (a) Common-emitter; and (b) Common-base configuration with their corresponding parasitic feedback capacitors.

excellent agreement between simulations and measured data. The measured/simulated *S*-parameters are plotted in Fig. 6. The HiCuM/L2 simulated maximum available and stable gains (MAG/MSG) of CE and CB InP/GaAsSb DHBTs are shown in the of Fig. 5 inset. Extrapolations of the modeled MAG/MSG up to $f \leq 1$ THz confirm the experimentally determined $f_{MAX} = 721$ and 850 GHz for CE and CB configurations. For $f > 140$ GHz, the CB topology provides a higher MAG/MSG than the CE topology. The power gain improvement largely arises because the parasitic feedback capacitance C_{CE} is lower in the CB in comparison to C_{BC} in the CE (as represented in Fig. 7) because of the vertical triple-mesa structure with a topside emitter contact. Consequently, the input reflected current is lower in the CB DHBT at high frequencies. For the pad layout in Fig. 1 for the CB topology, the transistor base is directly connected to a ground plane, minimizing the base resistance and inductance, and increasing the transistor stability [18]. The lower base resistance in CB thus accounts for its higher f_{MAX}.

C. LARGE-SIGNAL PERFORMANCE

Initial power measurements were conducted at 94 GHz to characterize the large-signal properties of the present DHBTs. In a first step, according to the *I-V* characteristics of the devices, power sweeps with 50 Ω load were performed under various class-A bias points to determine the most appropriate bias for load-pull characterization. The measurements indicated that power performance generally improves with higher V_{CE}. The transistors eventually experience self-heating induced degradation beyond certain voltages because of the lack of thermal management methods in the present work. Further improvements can be expected since various works demonstrate the improvement in the junction temperature and thermal resistance of InP HBTs when heat sinking or substrate transfer methods (with *no* changes in the epitaxial layer structure) are used [19], [20].

Extensive load-pull characterization was performed at lower voltages and lower input powers to maintain reliable device operation ($V_{BE} = 0.84$ V, $I_{E\,or\,C} \approx 24$ mA, and $V_{CE} =$ 1.2 V, and –3dB back-off input power).

Next, load-pull measurements were carried out for all transistor types (GaAsSb-based CE/CB, and GaInAsSb-based CE/CB). Fig. 8 shows P_{OUT} and gain contours in class-A operation for 9-μm-long devices. The optimum load for maximum P_{OUT} in the GaAsSb-based CE configuration is $Z_L =$ $(32.1 - j1.1)$ Ω and $(33.8 + j5.1)$ Ω in the CB configuration. The optimum load for maximum P_{OUT} in the GaInAsSb-based CE configuration is $Z_L = (31.8 - j17)$ Ω and $(27.6 + j5.9)$ Ω in the CB configuration. High power output and high gain domains overlap well in the Smith chart for both topologies. More importantly, the domains of high output power extend close to the center of the Smith chart, thus providing a low impedance transformation ratio to a 50 Ω system that favors low-loss output matching network realizations. Fig. 9 shows load-pull simulation results using the HiCuM/L2 model for the InP/GaAsSb CE and CB configurations. The simulated peak power output occurs for similar matching conditions to those measured for the CE configuration. The optimum load for the CB configuration however occurs at a different position in the Smith chart. We believe the principal reason for the discrepancy is that the HiCuM/L2 model for InP/GaAsSb HBTs was developed and optimized based on the measurements on a common-emitter device. A complete model extraction based on CB-DHBT devices is needed to obtain better agreement. Simulated peak output power levels agree with the experimental results for both the CE and CB configurations.

After determining the optimum load for the DHBTs, single tone CW power sweeps with a matched load were performed at higher bias conditions to determine the maximum achievable output power for each technology. Fig. 10 shows the change in P_{OUT}, power gain, and *PAE* as V_{CE} increases for a 9–μm–long CE InP/GaAsSb DHBT. The output power P_{OUT} increases from 10.4 dBm at $V_{CE} = 1.3$ V to 11.7 dBm at V_{CE} $= 1.6$ V while V_{BE} (and consequently I_C) remains constant (*i.e.*, 24 mA). This improvement can also be observed in the gain and PAE where the gain at $P_{OUT,SAT}$ increases from 6.3 to 7.6 dB and PAE at $P_{OUT,\,SAT}$ increases from 23.7 to 27.2 % by increasing V_{CE} from 1.3 to 1.6 V. The use of higher V_{CE} biases degrades device performance of InP/GaAsSb DHBTs because of self-heating.

The same procedure was followed for InP/GaInAsSb CE and CB DHBTs to determine the maximum bias voltages that

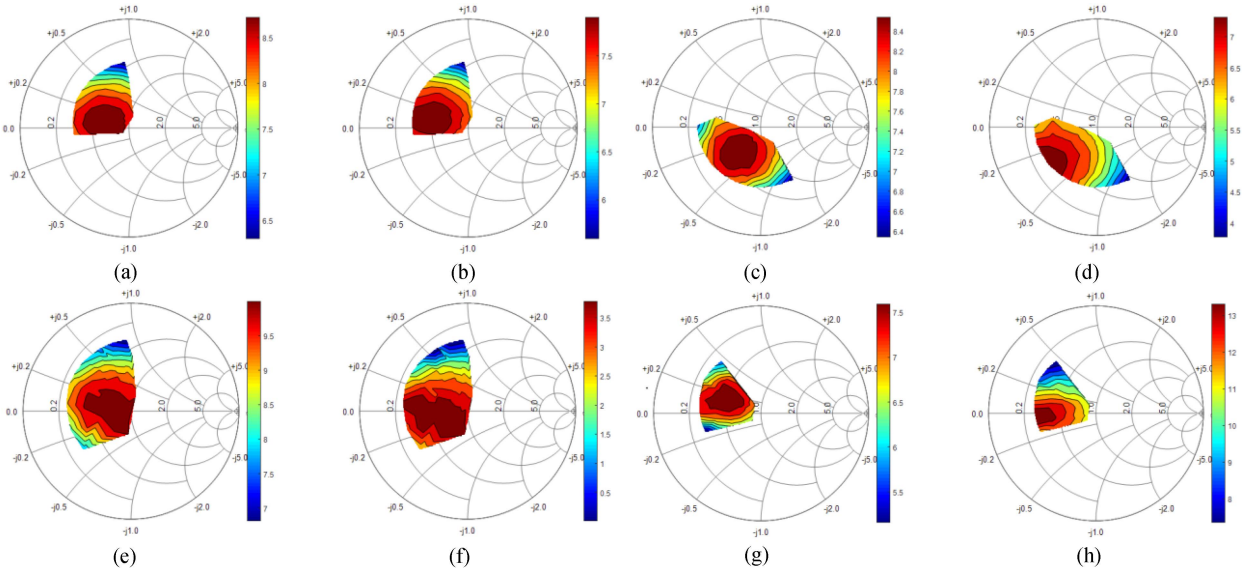

FIGURE 8. 94 GHz load-pull contours of a (0.3 x 9) μm^2 DHBT for (a) P_{OUT} and (b) gain in the common-emitter InP/GaAsSb topology, (c) P_{OUT} and (d) gain in the common-emitter InP/GaInAsSb topology, (e) P_{OUT} and (f) gain in the common-base InP/GaAsSb topology, and (g) P_{OUT} and (h) gain in the common-base InP/GaInAsSb topology all biased at $I_{E\text{ or }C} \approx 24$ mA and $V_{CE} = 1.2$ V with –3dB -back-off P_{IN}.

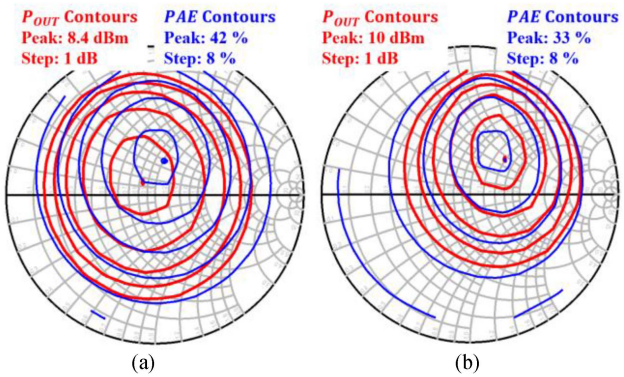

FIGURE 9. Load-pull HiCuM/L2-based simulations for a (0.3 × 9) μm^2 in (a) common-emitter and (b) common-base configurations. The simulations are carried out under the same bias and input power conditions as the measurements.

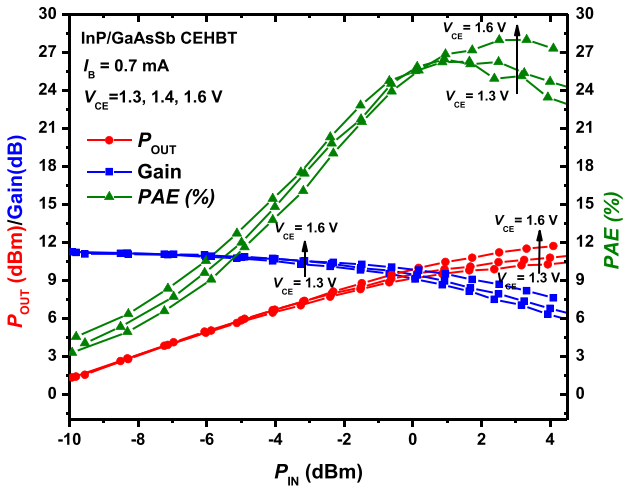

FIGURE 10. 94 GHz power characteristics of a (0.3 × 9) μm^2 common-emitter InP/GaAsSb DHBT with different bias conditions and an optimally matched load.

TABLE 4. Maximum Tolerable Bias Conditions in Class-A of (0.3 × 9) μm^2 DHBTs for Maximum P_{OUT}

	V_{CE} (V)	I_C or I_E (mA)	$P_{OUT,SAT}$ (dBm)
InP/GaAsSb CE-DHBT	1.6	24	11.3
InP/GaAsSb CB-DHBT	2.4	24	10.6
InP/GaInAsSb CE-DHBT	1.8	24	11.4
InP/GaInAsSb CB-DHBT	2.8	24	14.5

allow degradation-free operation. Table 4 shows the class-A operating points of the four different technologies. A power sweep at these bias conditions was then conducted and is reported in Fig. 11. The GaInAsSb-based CB DHBT delivers the highest P_{OUT}. Its superior class-A performance arises because of the higher breakdown voltages in InP/GaInAsSb DHBTs: they enable a larger swing between BV_{CEO} and the knee voltage V_{knee} in CE operation, as well as a significantly higher BV_{CBO} in CB operation. As discussed in [21], in class-A where the transistor is always in the active forward region, the maximum output power is generated by signals sweeping between V_{knee} at maximum I_C and BV_{CEO} (BV_{CBO} for the CB configuration) at $I_C = 0$, leading to an optimum load impedance

$$R_L = \frac{BV_{CEO} - V_{knee}}{I_{C,MAX}} \tag{1}$$

resulting in a peak linear output power

$$P_{OUT,max} = \frac{1}{8}\frac{(BV_{CEO} - V_{knee})^2}{R_L} \tag{2}$$

TABLE 5. Reported Power Performance of InP DHBTs

Ref.	Technology	Topology	*freq.* (GHz)	OP_{1dB} (dBm)	$P_{OUT,sat}$ (dBm)	Bias Conditions	Linear Gain (dB)	Gain at P_{SAT} (dB)	DHBT P_{OUT}/Length (W/mm)	DHBT P_{OUT}/Area (mW/μm²)	Area (μm²)
[24]	InP/GaAsSb DHBT	CE, 1 Finger	40	9	10.5	V_{BE} = 0.8 V, V_{CE}=1.5 V	11	5	0.975	1.6	0.6×11.5
[25]	TS InP/InGaAs HBT	CE, 2 Finger	77	NA	14.2	I_B = 1.1 mA, V_{CE}=2.6 V	5.8	5.8	3	3.2	2×4
[26]	TS InP/InGaAs HBT	CE, 1 Finger	77	8	9	I_C = 22.7 mA, V_{CE}=1.4 V	10	7	1,3	1.6	0.8×6
	TS InP/InGaAs HBT	CE, 2 Finger	77	9	10	I_C = 29.6 mA, V_{CE}=1.4 V	7	4	0.83	1.0	0.8×12
[27]	InP/InGaAs HBT	CE, 4 Finger	30	10*	15.5	I_C = 60 mA, V_{CE}=2 V	11	6	0.89	1.3	0.7×10×4
[28]	InP/InGaAs HBT	CE, Multi Finger	90	NA	13.7**	I_C = 60 mA, V_{CE}=2 V	15**	NA	0.97**	3.9**	0.25×24
	InP/InGaAs HBT	CB, Multi Finger	140	NA	13.8**	I_C = 60 mA, V_{CE}=2 V	12**	NA	1**	4**	0.25×24
[29]	InP/InGaAs HBT	CE, Multi Finger	94	NA	NA	I_C = 128 mA, V_{CE}=2.7 V	9-10	NA	1.88	7.52	0.25×48× 2
[30]	SiGe:C HBT	CE. 1 Finger	94	NA	11	**V_{BE} = 0.86 V, V_{CE}=1.9 V**	NA	4.8	6.0	30.1	0.2×5.56
[31]	InP DHBT on BiCMOS	CE, 1 Finger	96	13.3	14	I_C = 23.7 mA, V_{CE}=2.4 V	5	2.5	5.26	6.5	0.8×5
[32]	InP/GaAsSb DHBT	CE, 1 Finger	94	11.5	12.8	I_B = 2.6 mA, V_{CE}=2.8 V	8	4.5	2.05	10	0.2×9.5
[9]	InP/GaAsSb DHBT	CE, 1 Finger	94	9	11	I_C = 20 mA, V_{CE}=1.6 V	10	6.5	1.38	4.6	0.3×9
[2]	InP/GaAsSb DHBT	CE, 1 Finger	94	10	10.4	V_{BE} = 0.83 V, V_{CE}=1.9 V	11.8	9.1	1.17	6.67	0.175×9.4
This Work	**InP/GaAsSb DHBT**	**CE, 1 Finger**	**94**	**10.4**	**11.3**	**V_{BE} = 0.84 V, V_{CE}=1.6 V**	**11**	**4**	**1.50**	**5.0**	**0.3×9**
	InP/GaAsSb DHBT	**CB, 1 Finger**	**94**	**9.5**	**10.6**	**V_{BE} = 0.84 V, V_{CE}=2.4 V**	**13.6**	**4.2**	**1.3**	**4.3**	**0.3×9**
	InP/GaInAsSb DHBT	**CE, 1 Finger**	**94**	**10.4**	**11.4**	**V_{BE} = -0.84 V, V_{CE}=1.8 V**	**11.9**	**4**	**1.5**	**5.0**	**0.3×9**
	InP/GaInAsSb DHBT	**CB, 1 Finger**	**94**	**13.5**	**14.5**	**V_{BE} = -0.84 V, V_{CE}=2.8 V**	**12.1**	**5.2**	**3.13**	**10.4**	**0.3×9**

*read from the graph
**simulation results

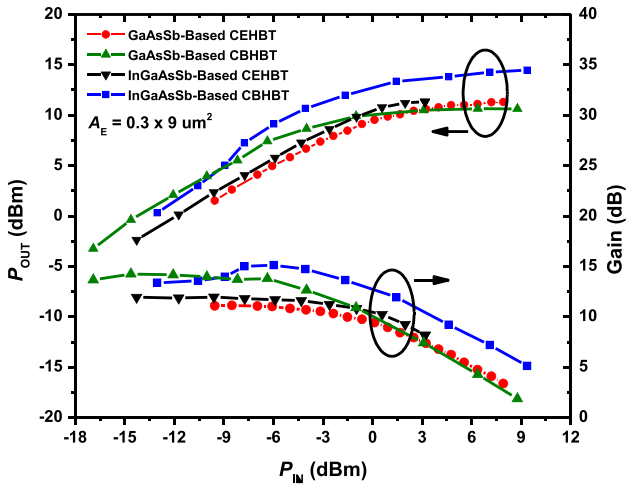

FIGURE 11. 94 GHz power characteristics of a (0.3 × 9) μm2 DHBT for different topologies biased for maximum power at matched load.

for a V_{CE} supply voltage equal $1/2(BV_{CEO}+V_{knee})$. Table 2 shows that $BV_{CEO} - V_{knee}$ is highest for GaInAsSb-based DHBTs. However, in the CE configuration, device degradation occurs for $V_{CE} < 1/2(BV_{CEO}+V_{knee})$. In contrast, $1/2(BV_{CEO}+V_{knee})$ can almost be achieved in the CB structure: CB DHBTs degrade far later than CE devices. Fig. 12 shows the reconstructed dynamic load-line at $P_{OUT,SAT}$ superposed on the common-emitter and common-base *I-V* curves for CE and CB DHBTs, respectively. In both configurations, the quaternary-based device is showing a higher voltage swing, as expected from the higher breakdown voltages in GaInAsSb-based DHBTs. The high-voltage load-line endpoints for zero collector current are lower than the breakdown voltages in both technologies because significant collector current flows near maximum voltage points as shown in the dynamic load-lines of Fig. 12. Textbook load-lines extending to the breakdown (determined at 1 kA/cm² *i.e.*, currents of 27 μA without significant heating) do not consider heating effects. The dynamic load-line trajectories in Fig. 12(c)) and (d)) show currents ∼10 and 20 mA which give rise to heating effects. The introduction of heat management techniques will alleviate device self-heating and allow wider signal swings over a greater fraction of DC breakdown voltages and lead to higher output power levels. For example, better thermal management in SiGe HBTs lowered the collector junction temperature by ∼10 K and enabled a 67 % rise in output power at 94 GHz [30].

Another large-signal figure-of-merit (FoM) is the output power density, *i.e.*, the saturated P_{OUT} per emitter unit area. The importance of this FoM arises when the device high cut-off frequencies have to be traded-off against the high-power properties, such as in sub-mm-wave power amplifier applications. For example, longer emitter fingers tend to deliver higher output powers, whereas f_{MAX} reduces for large-area

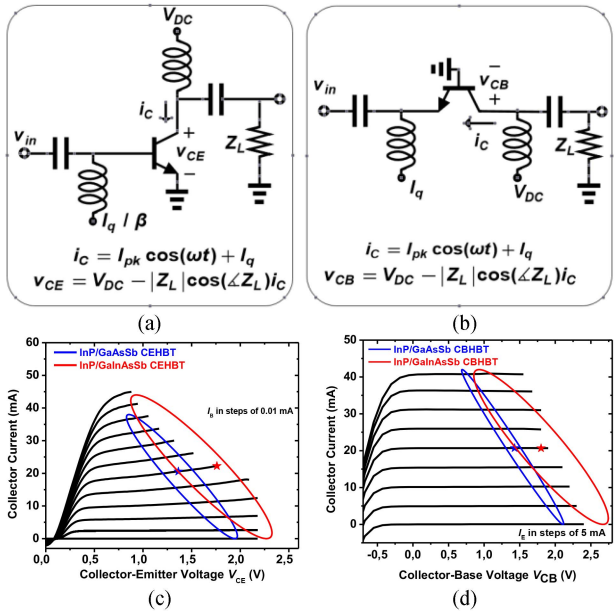

FIGURE 12. Reconstruction of dynamic load-line for (a) common-emitter; and (b) common-base configurations. (c) Reconstructed 94 GHz dynamic load-line at peak output power superposed on the (c) common-emitter; and (d) common-base I-V curves.

devices [22]. A high power density is thus advantageous in order to secure optimal performance in power amplifiers operating at sub-mm-wave frequencies. P_{OUT} per area of a single transistor for all the four topologies are reported and compared to the published InP DHBTs in Table 5. A state-of-the-art power density of 10.4 mW/μm^2 (or 3.13 W/mm) is measured for the CB quaternary-base DHBTs. Similarly, the saturated P_{OUT} of this topology is the highest measured reported output power for any single InP DHBT at 94 GHz.

V. CONCLUSION

(0.3 × 9) μm^2 GaAsSb- and GaInAsSb-based InP DHBTs were fabricated and characterized by load-pull measurements at 94 GHz. Quaternary CB DHBTs offer the best performance with a record $P_{\mathrm{OUT,SAT}} = 14.5$ dBm with simultaneous 10.4 mW/μm^2 (or 3.13 W/mm) power density when matched for the highest output power. This performance largely arises because of the high breakdown voltages ($BV_{\mathrm{CEO}}/BV_{\mathrm{CBO}} =$ 5.3/7.3 V) in the GaInAsSb technology, which allow higher biasing voltages and output powers. Additionally, the high gain of the CB topology at mm-wave frequencies makes it a suitable core for PA cells. The power performance superiority of the CB configuration over CE DHBTs appears to confirm the analysis of Qin et al. [23]. Whereas InP/GaAsSb CB DHBTs perform better than CE devices for low P_{IN} (and conversely for high P_{IN}, as for SiGe HBTs in [23]), InP/GaInAsSb CB DHBTs are superior to CE devices for all input power levels (Fig. 11). Furthermore, CB operation increased the robustness of both ternary- and quaternary-based DHBTs against degradation during high-power operation. The load-pull contours show the highest gain and P_{OUT} occur in the vicinity of the center of the Smith chart. This feature is especially interesting when designing amplifier output matching networks. Work is currently proceeding toward the implementation of CB InP/GaInAsSb DHBT PA cells at sub-mm-wave frequencies.

ACKNOWLEDGMENT

The authors would like to thank the staff of FIRST lab at ETH Zurich, Zurich, Switzerland, for their support in the fabrication process of this work.

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