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Silicon Micromachined Waveguide Circuit for a 2 THz Schottky Receiver: Progress and Challenges

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ABSTRACT Space instruments that operate in the THz range can enable unique measurements for a better understanding of the chemical and physical processes taking place in our Universe. One such application of this technology is a compact 2.06 THz receiver that can measure the ionized oxygen line to determine wind velocity in Earth's upper atmosphere. Metal machined waveguide circuits have long been utilized to build and demonstrate functional receivers in the submillimeter-wave range. However, as the operational frequency is increased, extremely challenging requirements are placed on metal machining in terms of the required precision, surface roughness, and alignment tolerance. This work describes the design and implementation of the first-of-its-kind, vertically-integrated, 2-THz Schottky diode mixer using precise silicon micromachine technology. A traditional e-plane split waveguide package is re-designed to utilize the three-dimensional (3-D) capability of stacking silicon micromachined parts. The silicon microfabrication process has been optimized to produce smooth and precise features for packaging a 2 THz subharmonic GaAs Schottky diode mixer, providing surface roughness better than 1-micron rms with less than 5% variation on critical dimensions. The subharmonic mixer and a fully solid-state local oscillator (LO) chain is currently being implemented to validate silicon micromachining for THz packaging. The impact of micromachining variation on mixer performance is explored through simulations over a range of dimensions on the most sensitive regions of the Si module.

INDEX TERMS THz technology, heterodyne receivers, Schottky diode mixer.

I. INTRODUCTION

As frequency scales into the several THz regime, fabrication and integration of precise metal waveguides becomes challenging, resulting in design considerations to pre-compensate for minute offsets, matching mechanical strain on all interfaces, and including alignment verification as part of the development process. Traditional computer numerical controlled (CNC) milling machine requires skilled machining techniques to reduce burrs at the interface, which can result in slight misalignment and resultant strain between two component pieces. Detailed 3-D electromagnetic (EM) simulations have shown that even a 2-μm misalignment of the integrated diode chip or a few microns of misalignment between the waveguide halves can drastically reduce circuit performance [1]. In order to address this issue, we turn to Si micromachining as a possible solution. Considerations arise and are addressed that are unique to developing this condense Si module. In this work, we report on the progress made for the first ever Schottky diode mixer waveguide circuit at 2 THz with bulk silicon micromachining technology.

By using Si bulk processing techniques with optimized process recipes, Si blocks can be fabricated and then sputtered with gold to meet the requirements of THz packaging and allow for the expansion of integrated circuitry to more complex circuit and system topologies, including array receivers [2]. Our team has previously developed advanced silicon

processes [3] and used them to demonstrate Schottky components in the 500-750 GHz range [4], as well as micro-lens antenna at 1.9 THz [5], emphasizing the potential to deploy Si blocks for supporting Schottky diode mixers. In this work we report on the challenges encompassed by construction of a 2 THz subharmonic mixer waveguide circuit based on silicon micromachining technology. In particular, this design space incorporates many of the existing THz technologies in order to achieve some aspects of backward compatibility.

In this work, a traditional e-plane split waveguide packaging approach is baselined, implemented through nontraditional, 3-D stacking of thin silicon wafers comprising the waveguide circuit. As part of this process, the implementation of the DC bias circuitry and the matching circuitry for the down-converted intermediate frequency (IF) line were both embedded within the Si stack, contributing to the compactness of the package. This development focused on adapting an interface between the metal LO chain and the 2 THz Si package that considers mechanical and alignment constraints. Then, through wafer-level fabrication, the Si module production and process are characterized, exhibiting that tight tolerances are achieved. Complementing these results are simulations to show the tolerance needed to achieve desired mixer performance. Process tolerance and corresponding percentages deviating from achievable performance is also shown through simulations with specific attention paid to various combinations of offsets in fabrication and assembly that allow for performance optimization. Understanding tolerance to this degree is necessary for the purposes of fine molecule detection.

The 2 THz GaAs Schottky diode mixer will enable detection of the OI line, which occurs at 2.06 THz [6]. Metal based Schottky receivers operating at close to and above 2 THz have been demonstrated by several groups [7]–[10]. Scientific instruments operating in this wavelength regime are of interest to NASA for the capability they provide in modelling thermospheric dynamics in the Earth's atmosphere. Measurements will contribute to insight into the energy being coupled from the sun. Besides the 2 THz mixer, the receiver will also need an advanced LO chain that can provide sufficient power to pump the subharmonic mixer. As part of this investigation, a 1.03 THz LO chain has been built to pump the Si-based subharmonic mixer and will be discussed. The LO chain, however, still uses conventional split-waveguide, fully metal blocks and part of the challenge in this work was to implement a metal-to-silicon interface between the LO chain and the mixer.

II. DESIGN AND SIMULATION OF 2 THZ SILICON MICROMACHINED WAVEGUIDE MODULE

This section presents the concepts behind designing a 2 THz waveguide block through Si micromachining for integration with a metal block [11]. Visualization of this process can be seen in Fig. 2.

An E-plane split waveguide block has been designed for the mixer housing. One-half of the block with the carefully matched waveguide features is shown in Fig. 1. The RF signal couples through the page while the LO signal is fed via the waveguide. Since the LO chain is based on a metal block, one of the first hurdles is to design a robust interface between the metal LO block and the silicon-based mixer block.

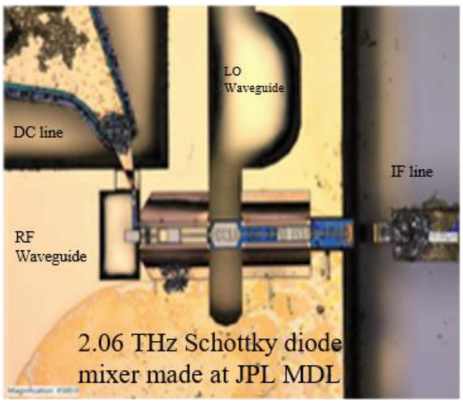

FIGURE 1. The diode is mounted in the channel, and centered to the RF input.

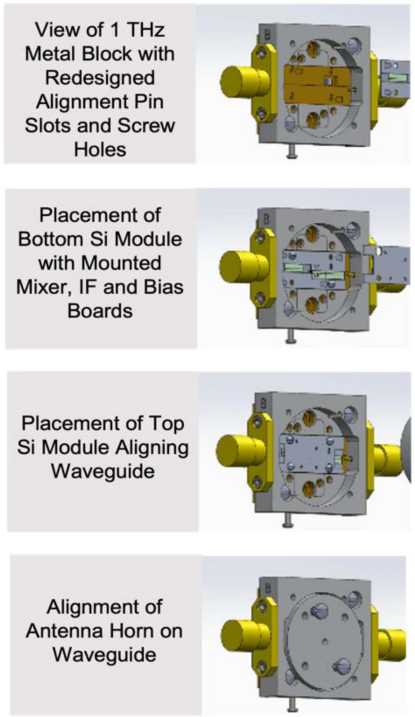

FIGURE 2. Visualization of assembly process utilizing a model of the 1 THz block secured with metal interface, where several of the main parts of the extended process is shown from top to bottom.

A. DESIGN AND DEVELOPMENT OF SI MODULE

Among other considerations, keeping the module compact was a key driver of its design in Si, particularly in comparison with metal machined blocks for reducing waveguide losses, especially in the RF coupling waveguide. For instance, the thickness of the two pieces that comprise the Si waveguide is 700 μm, whereas the analogous metal block, as used in [12], is

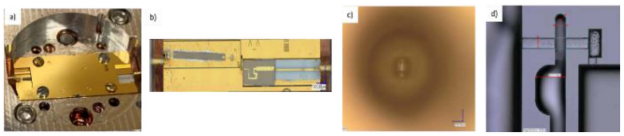

FIGURE 3. **(a) The entire module is mounted in the hybrid assembly. (b) The Si block is opened, showing the pockets for I/O board placements and the waveguide feature in the center. (c) The microscope image shows the circular antenna aperture. The focus is on the probe, centered to the waveguide, which is also centered in the aperture. (d) Lateral dimensions of interest are verified using the microscope.**

approximately 2 cm. This reduction in thickness reduces the total path length, minimizing waveguide losses. To enable a module of this reduced thickness, other adaptions also needed to be made.

The Si module design includes waveguide features, structures for alignment, as well as circuitry within a singular closed platform. It should be noted that the RF and LO signals are fed directly into the silicon waveguides.

Precise fabrication both laterally and vertically are important for an optimized design. The Si block houses two boards, which can be seen enclosed from the top down in Fig. 3(a). The bias board is sitting in the left pocket of Fig. 3(b), and the IF board is placed in the right pocket, both in the bottom Si piece. The top Si block includes pockets in matching areas to accommodate for wire bonding clearance.

In order to enable a module of this reduced length, the IF board was redesigned in quartz material. Quartz was selected as a material that could be utilized for supporting impedance matching at this much reduced thickness. Islands of gold strips were also made for wire bonding contacts to the bias board, made to within the dimension of the pockets housing the bias board.

The vertical waveguide, seen from the top-down in Fig. 3(d), supports a 1 THz to 2 THz transition and is equally divided between the top and bottom Si piece, with each piece having a thickness of 350 μm. Since the Schottky diode sits in this channel divide, fabrication accuracy is an important element of successful coupling. By design, the diode beam lead is aligned in the waveguide by centering it both vertically and horizontally. The height of the strip line mounted in the pockets holding the boards must lie below the beam lead for good contact. The specific pocket depth must also coincide with a subset of the vertical waveguide depths that are micromachined, as will be discussed further in the section on fabrication.

B. SIMULATIONS

In order to enhance comprehension of this new process, detailed simulations of the proposed design were carried out to gain a better understanding of expected performance and acceptable variations that arise during fabrication.

The graph seen in Fig. 4 is the simulated performance from the fabricated block.

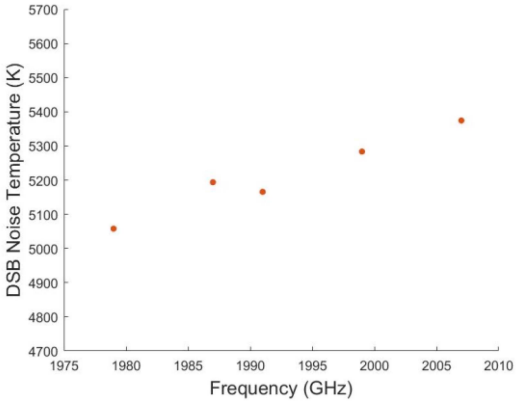

FIGURE 4. **The graph shows the simulated performance of the fabricated mixer in the Si module across operational frequency range.**

TABLE 1. **Shows Measurement Results of Etched Depths, Reflecting < 5% Error Margin, Well Within Margin of < 10% Being Acceptable of 14 Si Pieces of Top and Bottom Stack**

Channels	Average Percentage Error
Critical Channel Top	5.00%
Critical Channel Bottom	4.11%
First Step	3.95%
Second Step	4.59%

Using Ansys HFSS, the output responses were generated by performing scans of the dimensions of the channel where the device sits, and fed into the ADS tool assisting in this parametric analysis. This parametric study highlights regions of the module to focus on when developing a high-tolerance process for supporting the high-frequency mixer. These simulations also accounted for the average fabrication deviation measured in this work and described in Table 1.

In the electromagnetic modelling environment, the mixer device sits in the channel as it does in the actual configuration, placed between the top and bottom piece.

Variations in these first two sets of simulations were balanced. For the first set of simulation, this meant that the over- or under-etching were simulated to be equal for the top and bottom pieces. It was found that the channel has little difference in performance when simulated up to 0.5 to 1 μm of under-etch and over-etch.

The second set of simulations performed is of the condition where the channel width is wider or narrower than by design. Varying worst case channel width to 20% from design resulted in DSB noise temperature variation by up to 5% in the frequency range of interest from 1.98 to 2.06 THz. Variations in channel width are seen to have a low effect on performance.

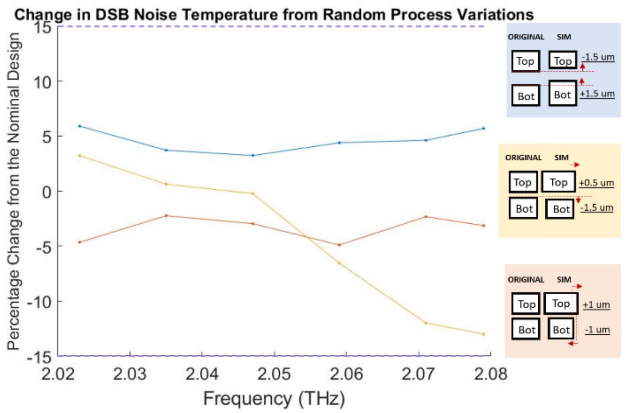

FIGURE 5. These simulation results are generated from the scenarios shown on the right, whereby a subset of non-symmetrical channel variations is considered with each plotted line corresponding to its adjacent diagram. The plot shows the percentage difference in performance from design. These values indicate that the design is robust against uncertainties from the silicon micromachining process.

The next area examined considers non-symmetrical variations. Combinations of channel width and channel height variations that are non-symmetrical are simulated and represented by Fig. 5. It can be seen that the impact due to non-symmetrical channel height increases to 15% in the wider frequency range than shown, whilst channel width in the same range of variation has less of an impact.

Included in Fig. 5 is the final set of simulations performed for the following cases: when there is both an over- and under-etched channel, both a wider and an over-etched channel, and both a wider and a narrower channel. Simulations in these cases included channel height deviating by 8% and channel width deviating by 20% from design. The DSB noise temperature is $<$ 15% difference from design, illustrating that various combinations of modules with variations from design have reasonable resulting performance.

It is significant that not only can this tight coverage be achieved in silicon fabrication, when it is comparably more challenging to achieve this level of resolution in metal machining, but incorporating dimensional analysis towards symmetrical offsets can also play an integral part in optimizing DSB noise performance. Understanding variations in tolerance can then be incorporated into part of the process to enable optimized performance for a high-frequency mixer.

III. FABRICATION OF SILICON MODULE AND ASSEMBLY

Si micromachining is utilized to fabricate the designed module. In particular, waveguide structures, passive couplers, and features like precise pinhole alignment pockets supporting operability from the 100 GHz to 750 GHz frequency range have been realized through Si micromachining [4].

Multi-step deep reactive ion etching (DRIE) using SiO_2 as the mask provides the capability to finely control etch depth and formulate a structure's design with consistency. Here, Si micromachining capability is extended to 2.06 THz. Multi-step waveguides with smooth walls of $<$ 300 nm surface roughness, as seen in Table 2, and precise alignment between wafers on the same order of magnitude are fabricated and verified across wafers.

TABLE 2. Shows Root Mean Square (RMS) Roughness and Arithmetic Average of Absolute Roughness for a 1 THz Waveguide Using the Si Micromachining Process, As Well As for the Cases Without the Final Smoothing Step, Both with and Without Metallization

Characteristic	RMS Roughness	R_a: Average of Absolute Roughness
Smoothed Surface Post-Sputter (μm)	0.286 μm	0.182 μm
Not Smoothed Post-Sputter (um)	0.489 μm	0.369 μm
Not Smoothed Pre-Sputter (um)	0.444 μm	0.372 μm

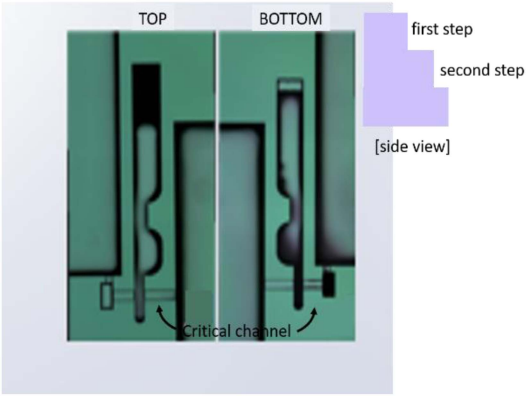

FIGURE 6. The waveguide structure and its critical dimensions, including various etch depths, are shown in this diagram. This image is taken from the top-down, but a side profile of the waveguide, at the top end of the feature, is included in the inset.

A. FABRICATION PROCESS

To illustrate the uniformity and scale of the process, two wafers comprised of the Si modules were fabricated. Each wafer consisted of fourteen sets of top and bottom pieces.

The following steps are taken for each wafer run. First, the oxide mask is created via i-line stepper lithography, followed by a pre-etching step using Fluorine-based inductively coupled plasma (ICP) to create the masks for the fine vertical waveguide heights seen from the top-down in Fig. 6.

Then, DRIE is performed. Multi-step DRIE allows for Si micromachining of multiple depths with precision and smoothness. All etched features in the module are patterned such that each layer of mask will cumulatively sum up to the deepest etch. This is achieved by growing the mask oxide thickness to cover the depth of all the patterns required by the design. The specific oxide thickness is determined by the

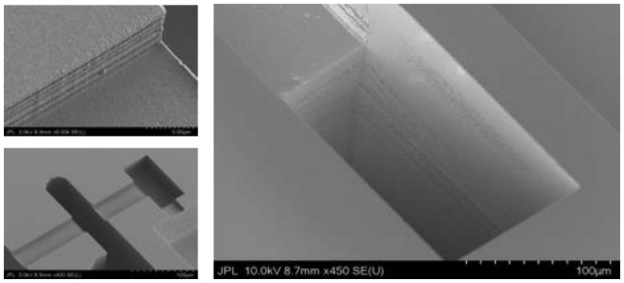

FIGURE 7. The SEM images of the waveguide features: The upper left is the channel where the Si piece will sit. The lower left is a zoomed-out image, and on the right is the diagram of the vertical Si waveguide. These SEMs show the smoothness of the side walls, as well as the sharp angles of the waveguide features.

selectivity between oxide and Si. This fabrication process was adapted from recipes previously developed at Jet Propulsion Laboratory [3].

B. FABRICATION VERIFICATION

Two variables are measured to verify fabrication uniformity and functionality: the depth of features, as well as the smoothness of the waveguide sidewalls.

The depths are measured using the Dektak profilometer, which is shown to have step height repeatability of < 10 Å with 1 sigma [13]. These measured dimensions are displayed in Table 1, illustrating the average variability measured for critical features on the utilized wafer. In particular, the channel depth is later simulated across the range of variations resulting from fabrication.

Wafer-to-wafer variation is also characterized. The wafer-to-wafer variation has a Prob $> |t|$ that is < 0.001 for all of the relevant depths. JMP Statistical Software was used for the statistical calculations.

Accurate dimensions for the heights displayed from the waveguide to the channel specifications are important to achieve desired mixing performance. While the two most crucial steps going into the 2 THz waveguide regime were measured using the profilometer, the third step was measured using imaging with an Olympus microscope, since the etch was too deep for the probe tip to reach.

Less critical dimensions were measured as well to validate that the process could achieve rendering of desired heights across different regional dimensions. These areas were created for holding the IF boards, and for bringing out the DC bias lines as well as for alignment pin pockets. The values were 116 μm with deviation of 3.06% from designed value, and 183.2 μm with 2% deviation from designed value, respectively.

Fig. 7 shows the top-down microscope image of the waveguide structure taken using the scanning electron microscope (SEM). As mentioned, side wall roughness is an important metric to monitor. Smooth vertical sidewalls reduce ohmic losses in the Si stack [14]. From the top left image in the figure, it can be seen that the side wall roughness is < 1 μm, whereas exact measurements follow.

1-THz waveguides, fabricated in a separate instance, were characterized with the Veeco surface profiler in order to measure the surface roughness. The profiler has sub-nanometer vertical resolution [15], allowing for the surface roughness displayed in Table 2 to be measured. The measurement is represented in two ways. While the root mean square (RMS) roughness is the square root of the mean difference between peaks and valleys, the average of absolute roughness (R_a) is the mean difference of peaks and valleys.

These waveguides were smoothed by using buffered oxide etch (BOE) followed by a thin oxide growth, and a repeated BOE process. This step removes some of the surface roughness introduced throughout the process steps. Then, Au is sputtered on the surface of the Si. As can be seen, any large peak or valley would have a greater effect on the outcome of the RMS calculation. The relative roughness is shown to have decreased by > 1.5x with this smoothing process.

C. ASSEMBLY AND ALIGNMENT

Key considerations to this design are retaining good co-alignment between multiple interfaces and maintaining compatibility with existing metal platforms.

The first alignment and interface consideration during integration resides between the 1 THz metal LO block and the Si-based mixer block. Pockets that house pins for aligning the frontside of the metal block to the backside of the Si module are machined in the quadrants of the 1 THz multiplier block. The combination of the fabrication precision of these pockets and its pins can provide fine alignment on the order of 1 μm [4].

The second alignment consideration is between the two pieces of Si that sandwich the Schottky diode mixer chip. These two pieces have similar pockets fabricated on mirrored sides of the Si to support alignment between the two silicon halves.

Finally, a metal horn is visually aligned with a microscope and affixed to the mixer module.

To hold each sector in place, the 1 THz metal block, seen as the base of the block rendering in Fig. 2, was re-designed to accommodate for screws that attach a CNC milled metallic backbone structure. This CNC milled metallic backbone structure yields a >10x reduction in volume compared to including another metallic block along the chain. This backbone structure preserves coarse alignment for mounting the 2 THz antenna horn, as well as houses screws for both the bottom and top pieces of the Si module, and accommodates the SMA output for the IF signal. Surface Mount Device (SMD) IF connectors were also considered as a potential method for an even more compact I/O integration. However, mechanical considerations for the cable and higher loss introduced to the path are barriers that must be overcome before choosing this more compact option. Many of the other key features of the 1 THz block, like the waveguide design wherein the 1 THz multiplier is seated, remained unchanged from the existing design, as did the remainder of the LO chain, comprised of

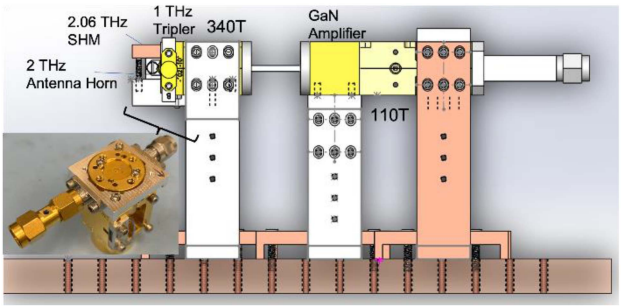

FIGURE 8. Model of LO chain where the metallic LO chain consists of the following: 110 GHz tripler, GaN amplifier, 340 GHz tripler, and 1 THz triper. The assembled module from 340 GHz tripler block onwards, including the designed module interface, is inset to the left of the figure.

metal blocks housing Schottky diode multipliers. These components, embedded within the full LO chain, are displayed in Fig. 8. The shift of supporting the highest frequency component to Si also transfers the tolerance requirements away from metal, filling an essential need as frequency scales.

In metal machining, much of the THz-level machining requires specific milling bits and precise tooling [16]. The sharpness of waveguide corners is dependent on both of these factors. Meanwhile, with Si micromachining, precise lithography followed by specific etching processes preserves the sharpness of waveguide corners.

Mechanical design of the modules is also significant, since unnecessary stress may continue to reside in the body of the diode as parasitic effects [17]. The points where the diode beam leads lay on the block will inevitably have mechanical stress when enclosed. Similar to a micro-cantilever structure experiencing stresses on the structural micro-component of the diode, the sandwiched position will respond to bending, torsion, and axial loading [17]. Correct placement of all designed parts and minimal stress loading during secure block closures are therefore necessary design considerations.

Once the metal to Si waveguide alignment is completed, the antenna horn is aligned to the 2 THz output waveguide. This is made possible with a microscope having sufficient working distance covering the summative height of the antenna feedhorn and half of the width of a full Si block. The Keyence VHX-7000 microscope is used to take the image shown in Fig. 3(c). Specialized screws are tightened while maintaining visual alignment of the waveguide and beam lead through the antenna horn.

Through visualization, the waveguide is verified to be fully encompassed in the center of the antenna horn. The waveguide structure was located approximately 1.5 μm to the left of center, well within the center of the field [18].

IV. EXPERIMENTAL RESULTS

A. STATE OF THE ART LO

Fig. 9(a) depicts the scheme for the 1.03 THz LO. A W-band GaN amplifier is used to boost the input power to the submillimeter-wave tripler and the final tripler of the source. All of the multipliers used in LO chain have been developed

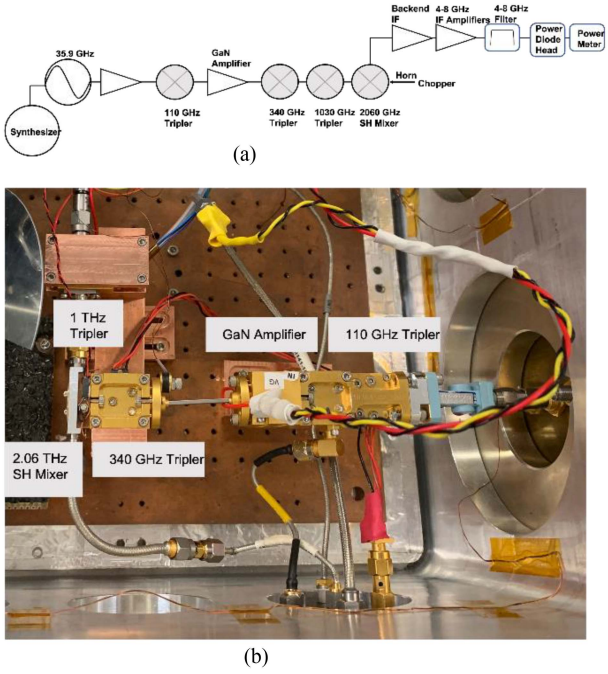

FIGURE 9. (a) Block diagram of experimental setup in room temperature (b) Top-down picture of setup for measurements, with the synthesizer and power amplifier outside of the chamber.

by our team at JPL (i.e., 110 GHz, 340 GHz, and 1030 GHz triplers).

The commercial GaN amplifier (Quinstar LLC) is characterized and measured performance is shown in Fig. 10(a). At the frequency range of interest, the small signal gain is 19 dB, and the 1 dB compression point is 23 dB. The output signal from the GaN amplifier is then sent into the 340 GHz tripler.

Its output, which is also included in Fig. 10(b), drives the following 1 THz tripler. Since a subharmonic mixer is being driven, the LO is at half the frequency of operation. The output level is shown in Fig. 10(c).

After mixing, the signal is observed at the center frequency of the IF chain, which consists of a cascade of low-noise amplifiers (LNA) and band pass filter (BPF). The detector head is calibrated with an Agilent Low-Noise Synthesizer source with its resultant fit covering the range of power measured. The picture of the full setup, with the chain resting on copper stands designed to provide good contact between the LO chain and the bottom cold plate, is displayed in Fig. 9(b).

B. MEASUREMENTS

The 2 THz receiver was assembled with the LO and mixer described above. The mixer device available has not been optimized and had an unusually high series resistance, as gauged by DC characterization of the device under test (DUT). As a result, doping concentration and epi layer optimization is being performed on the device to reduce access resistance. The use of the silicon waveguide places no additional requirements on the Schottky diode chip. However, the viability of using the proposed architecture is demonstrated by the measurement

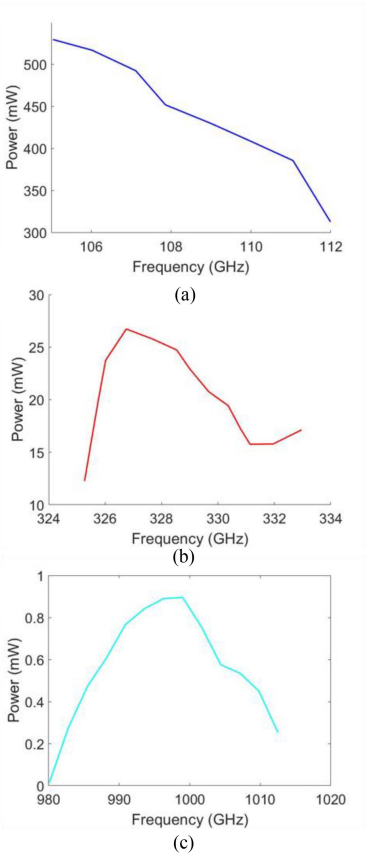

FIGURE 10. (a) Output of GaN Amplifier (b) LO Output from 340 GHz Tripler (c) 1 THz tripler output. These are all measured at room temperature.

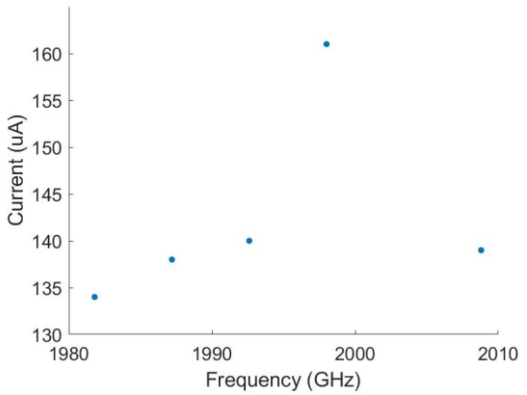

FIGURE 11. Mixer is verified by measuring the rectified current in the device with LO turned on, as captured by the graph shown here. An optimized device will be required to measure the receiver sensitivity.

shown in Fig. 11 of rectified current in the mixer diode. A future run will produce optimized chips to be reliably verified in this modular Si interface.

V. CONCLUSION

Development of a silicon micromachined module package for a 2 THz subharmonic Schottky diode mixer to perform THz limb sounding in the lower earth atmosphere has been described, from the design to the Si fabrication process, intricate assembly, and preliminary testing. This approach is found to be suitable for THz components and provides a viable path towards multipixel THz receivers.

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