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A Broadband 77/79 GHz Transmitter With Dual VCOs and Third Harmonic Signal Extraction in a 28 nm CMOS Technology

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ABSTRACT A broadband 77/79 GHz transmitter (TX) front-end for automotive long range radar (LRR) and short range radar (SRR) applications is presented in this paper. To achieve the best system performance one new TX architecture with two specifically designed voltage controlled oscillators (VCOs) is implemented in a 28 nm CMOS technology. Furthermore, the degradation of the VCO phase noise due to the TX integration is analyzed in detail and solutions to minimize the impacts are proposed and verified. Experimental results of a 20 GHz push-push VCO1 measured at the 77 GHz TX output show a continuous tuning range of 4.75 GHz, a coarse tuning range of 3.2 GHz and an average phase noise of −100 dBc/Hz @ 1 MHz, while a 26 GHz VCO2 with third harmonic signal extraction achieves a continuous and coarse tuning range of 7.5 GHz and 4.2 GHz with an average phase noise of −96 dBc/Hz @ 1 MHz at 79 GHz TX output. Moreover, a record pushing performance of $<\pm$ 100 MHz/V at 77/79 GHz TX output has been achieved according to the authors' best knowledge. The whole TX chip consumes about 860 mW from a single 2.1 V supply while providing more than 16 dBm output power over the whole frequency band.

INDEX TERMS Millimeter-wave radar, voltage-controlled oscillator, transmitter, 28 nm CMOS.

I. INTRODUCTION

The trend towards sophisticated Advanced Driver Assistance Systems (ADAS) and Autonomous Driving (AD) has gathered momentum in the automotive industry. The current 77/79 GHz radar products are still dominated by SiGe Bipolar technologies because of their superior noise and millimeter-wave performance [1], [2]. However, it is now very popular to design/implement radar chips in advanced CMOS nodes for higher integration level and even lower costs [3]–[5].

In a radar system on chip (SOC), the isolation between the TX and RX channels is limited due to the on-chip substrate- and metal-layer coupling and it could be even worse for a packaged transceiver (TRX). Therefore, the TX phase and amplitude noise will increase the noise floor of the RX IF signal which degrade the overall Signal-to-Noise-Ratio (SNR). Additionally a high TX phase noise could hide signals of small targets under the sideband of a large target spectrum when the large target is close to the radar sensor as described in [6]. Because of that one of the most challenging tasks for the implementation of a radar chip is to generate a 77/79 GHz signal source with low phase noise[1] and wide frequency tuning range by taking into account of the chip area, power consumption and also the system scalability [1], [2], [6].

It is well known that the 1/f noise of bipolar transistors is much low and the 1/f noise corner frequency is well below 100 kHz [7]. Therefore, the VCO phase noise realized with bipolar devices is good enough at 40 GHz and 80 GHz for

[1]For a LRR system a typical phase noise of about −95 dBc/Hz @ 1 MHz is strongly recommended [1].

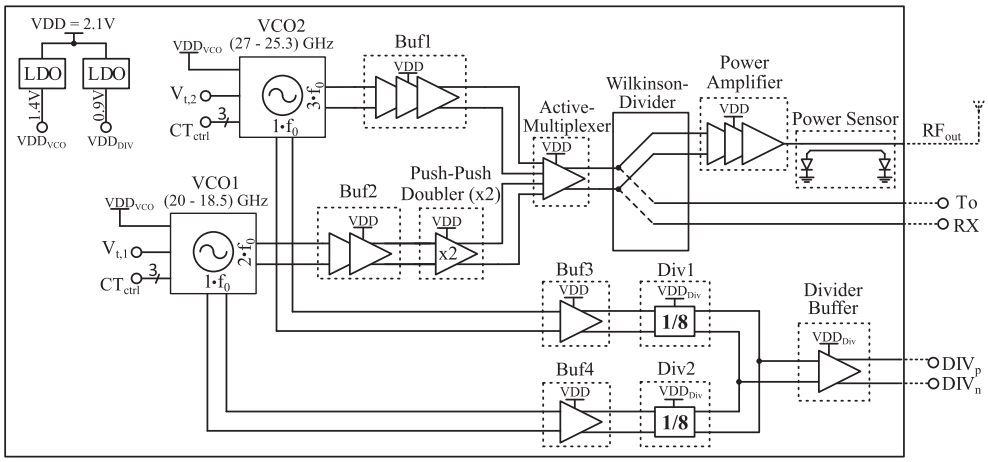

FIGURE 1. Block diagram of the proposed transmitter chip.

radar applications [1], [8], [9]. On the other hand, it is required to have the CMOS VCOs to operate at lower oscillation frequency in order to achieve robust VCO designs[2] and good phase noise [3]–[5]. Then the wanted 77/79 GHz signals needed in applications could be generated by following frequency multipliers. The main reasons to have the CMOS VCO operating at low oscillation frequencies are:

- a low transconductance of the MOSFET devices together with a decreasing quality factor of the varactor for higher oscillation frequencies result in a lower oscillation amplitude and also a lower loaded quality factor, thus a higher phase noise;
- the minimization of the 1/f noise up-conversion with different approaches, e.g., waveform-shaping of the drain voltage [10] or 1/f noise filtering techniques [10], [11], can only be effectively applied in the VCO circuits at lower oscillation frequencies.

In order to achieve the best VCO phase noise performance, the simple and intuitive considerations are minimizing the noise sources in the VCO core circuits, e.g., replacing the active current source circuit with a digitally controlled passive network to control the VCO core current over PVT [10], [11] and implementation of a digitally controlled oscillator[3] [10], [12] instead of an analog voltage controlled oscillator to avoid any AM-FM conversion of the varactor. In such oscillator circuit architecture the differential pair transistors are the main remaining noise sources in the oscillator core except the noise sources from the resonator losses. Therefore the minimizing of 1/f noise conversion to oscillator phase noise and improvement of the quality factors of the resonator elements are the last most critical steps to achieve the lowest oscillator phase noise.

The paper in [6] has shown a TX architecture with two VCOs which are operating at different center frequencies of 77 and 79 GHz. The two implemented VCOs are realized with same VCO design by optimizing mainly the VCO resonators in order to meet the VCO performance requirements from different applications.

It should be also mentioned that an extraction of the harmonic signals from the VCO core is feasible in a strong non-linear CMOS VCO circuit. Paper [13] has demonstrated a signal extraction at third harmonic of 20 GHz. Since the extraction is directly at the VCO resonator, the loaded quality factor of the VCO tank could be degraded by the following buffers[4] and thus also the phase noise.

It is observed in the authors' first monolithic integrated transmitter front-end chip, that the noise generated by the integrated high output power amplifier (PA) could degrade the VCO phase noise via the power supply. The root cause for it is analyzed in Section III-D and the corresponding solution is also proposed.

A new signal source architecture, shown in Fig. 1, is proposed by the authors' and the details will be presented in Section II. The implemented VCO design and the TX integration considerations will be discussed in Section III. Finally the experiment results and also the conclusions will be presented in Sections IV and V.

II. TRANSMITTER ARCHITECTURE

The proposed transmitter architecture is shown in Fig. 1 and the main difference to conventional TX architectures [1], [2] is the implementation of two different types of voltage controlled oscillators (VCO1: 20 GHz push-push VCO and VCO2: 26 GHz VCO with 3rd harmonic signal extraction) with different requirements on the center frequency and the VCO performance.

The implementation of two different VCOs offers the possibility to optimize the oscillator performance intended for

[2]A robust VCO should always oscillate over the defined process, voltage and temperature (PVT) variation ranges in applications and have a large enough oscillation amplitude.

[3]It should be mentioned that the DCO could achieve the best phase noise, but it is not feasible to be used in a conventional fractional $\Delta\Sigma$ analog PLL architecture which is the mostly popular PLL architectures in radar applications.

[4]The input impedance of the buffer consists not only capacitive loading, but also resistive loading at microwave and mmWave frequencies.

different applications, e.g., a VCO with smaller frequency tuning range, but lower phase noise for the long range radar (LRR) application or a VCO with larger frequency tuning range, but higher phase noise for short range radar (SRR) application.[5] Furthermore this architecture makes it possible to compare the performance of two different VCO implementations in a simple and cost-effective way. The first oscillator, VCO1, is designed as a push-push VCO at a fundamental frequency of 20 GHz optimized for low phase noise (e.g., −100 dBc/Hz @ 1 MHz at the 77/79 GHz output), while the second oscillator, VCO2, is developed at a fundamental frequency of 26 GHz including the direct extraction of the third harmonic signal from the VCO core and offering a very large total tuning range (e.g., >11 GHz at the 77/79 GHz output).

For the first LO signal chain starting with VCO1, the signal at the push-push output (at 40 GHz) of the 20 GHz VCO drives a two stage cascode buffer (Buf2) which generates a large enough signal in order to drive a push-push frequency doubler in a strong saturation operation. In this way a large 2nd harmonic signal at 80 GHz is available at the output of the push-push doubler. For the second LO signal chain starting with VCO2, the 3rd harmonic signal directly extracted from the 26 GHz VCO is fed into a three stage cascode buffer (Buf1) which amplifies the VCO signal to a high enough input power for a signal multiplexer. The 80 GHz signals of the two signal chains are then connected to an active signal multiplexer and the signal chain can be selected via a digital bit. The selected signal is then split to the input of a TX chain and also to an LO input of a RX chain by an implemented Wilkinson power divider for the best radar system performance.[6]

The TX chain, which provides the signal for the TX antenna, consists of a power amplifier (PA) with an implemented on-chip power sensors. The power sensor consists of a transmission line based directional coupler, which is capable to separate the reflected signal from the transmitted signal. On both ports at the directional coupler (coupled and isolated ports), a diode based detector is placed to measure the power of the signal. The implementation of the diode based detector is similar to the presented detector in [15] but uses a MOSFET configured diode instead of the bipolar diode. With this configuration the forward TX output power and also the reflected signal power from the antenna can be measured and therefore it is feasible to monitor the matching performance at the interface plane of the chip [15]. The implemented power amplifier is similar to that in our previous published paper [16].

There are several buffers used in the complete TX architecture for signal amplifications and improvement of the isolation between the different circuit blocks. Each stage of Buf1 (three stage buffer) consists of a cascode architecture and the schematic of this cascode stage is similar to that of the active multiplexer shown in Fig. 2(b), but with only a single input (V_{in1p} and V_{in1n}). Therefore, the buffer stage contains a common-source transistor pair ($M_{1p/n}$), a common-gate transistor pair ($M_{3p/n}$), a neutralization capacitance (M_n) and a current source (I_0). Furthermore, the inter-stage matching of Buf1 is performed with transformers as shown at the outputs of Fig. 2(b). The remaining buffers (Buf2, Buf3 and Buf4) are designed with the same circuit architecture as Buf1. Since these buffers are working at about 40 GHz (Buf2), 26 GHz (Buf3) and 20 GHz (Buf4), the inter-stage matching is implemented with a simple LC matching network instead of the transformers as in Buf1.

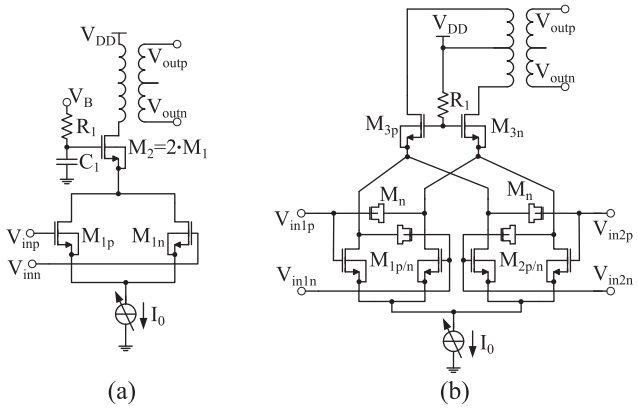

FIGURE 2. Schematic of the (a) push-push frequency doubler. (b) Active signal multiplexer.

Additionally two frequency divider chains are implemented, due to different input frequencies, to facilitate the PLL locking of the VCO frequency and improvement of the signal phase noise. Each divider chain consists of three low power static frequency dividers, while the whole divider chain consumes only 6 mA from a 0.9 V on-chip supply. To ensure a correct divider operation, the required input differential peak to peak signal amplitude $V_{pp} > 460\,mV$ is derived from a divider sensitivity simulation. The outputs of both frequency divider chains are then connected to the input of a common output buffer (Divider Buffer) and then to an output pad (DIV_p and DIV_n). Since the output buffer of the divider (Divider Buffer) is working below 3.5 GHz, it is designed as a single common-source stage with resistive loading. Furthermore some low noise LDO circuits are implemented on-chip in order to provide different voltages for all the building blocks from one common supply and to minimize the influence of the supply voltages (variations and noise) on the circuit performance.

A. 77 GHZ SIGNAL SOURCES GENERATION

As mentioned in Section I, it is common to implement a lower frequency VCO and then multiply this frequency to the desired frequency [3], [4], [5], [13]. With this frequency multiplication together with the above mentioned VCO architectures, a low CMOS VCO phase noise is achieved which is

[5]The SRR application can tolerate higher phase noise due to stronger phase noise cancellation of the transmit and receive signals in the radar system [14].

[6]In a radar transceiver, the correlated noise of the TX and RX signals could be canceled out in a RX mixer, while the un-correlated noise could degrade the system performance [14]. Therefore, to have the best radar system noise performance, it is required to minimize the un-correlated noise of the TX/RX chains as much as possible. This is achievable, if any signal amplification of the LO signal in the TX and RX chains, which will generate un-correlated noises separately, is avoided and realized before the power divider.

comparable to that of SiGe HBT VCOs (even at lower phase noise offset frequency range) [13], [17], [18]. But such architectures with frequency multiplication result in larger chip area, higher power consumption and also an increased difficulty of the harmonic spurs suppression (e.g., at $4 \cdot f_0 \pm f_0$) which could degrades the system performance.

On the other hand, all VCOs are working in a strong non-linear operating mode due to the self-limiting behavior. Therefore signals rich of harmonics are available in the VCO core and this gives several signal extraction possibilities for the higher harmonic signal generations:

- the fundamental oscillation frequency signal could be directly extracted from the VCO core;
- the second harmonic signal could be extracted at the common mode nodes (concept of a push-push VCO) due to a high available second harmonic signal at these nodes (the fundamental signal or any odd harmonic at this node is canceled out due to the implemented differential VCO circuits); and
- a third harmonic signal could also be directly extracted from the VCO core, especially for class-F VCOs which are optimized to have the higher harmonic signals in the VCO core for improving the VCO phase noise. The detailed analysis will be given in Section III A/C.

B. PUSH-PUSH FREQUENCY DOUBLER AND ACTIVE MULTIPLEXER

For the 20 GHz push-push VCO which delivers a signal at 40 GHz, a frequency doubler is required to generate the desired 80 GHz signal. A circuit architecture of a cascode push-push doubler as shown in Fig. 2(a) is chosen for the frequency doubler due to its simplicity and ease of implementation. The input impedance of the doubler is matched at 40 GHz to the output impedance of the driving buffer (Buf2) via a LC matching network to operate the differential common-source stage in strong saturation. The differential 80 GHz output signal is realized by extracting the second harmonic signal at the drains of the differential pair through a common-gate buffer stage and a transformer. This common-gate buffer improves mainly the isolation between doubler input and output and also the voltage gain. The transistors M_1 and M_2 are triple-well devices which makes it possible to tie the bulk directly to the source and therefore enables transistor stacking in a bulk CMOS technology [16]. The gate of the common gate transistor M_2 is connected to the bias circuit via a resistor R_1 to ensure the common mode stability and in addition the capacitance C_1 facilitates a low impedance for the second harmonic, to avoid any modulation of the gate voltage of M_2. The simulated output power (at 76 and 81 GHz) versus the input power (at 38 and 40.5 GHz) of the doubler is shown in Fig. 3(a). The frequency doubler goes into saturation at around $P_{in} = -5$ dBm and delivers a saturated output power of 4.5 dBm and 4 dBm at 76 GHz and 81 GHz, respectively. The fundamental and third harmonic signal at the frequency doubler outputs shown in Fig. 3(b) is lower than −20 dBm and this means a first and third harmonic suppression of about

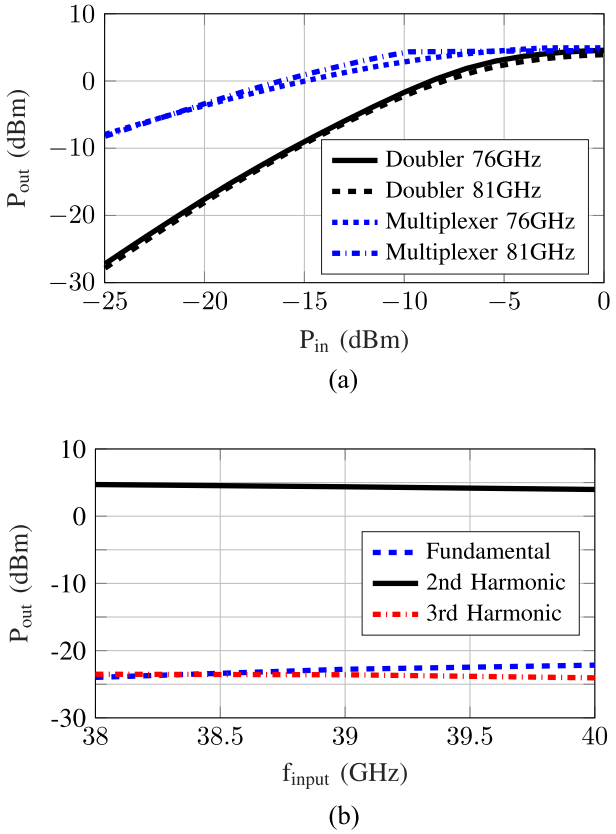

FIGURE 3. Simulated (a) output power vs. input power of the frequency doubler and the active multiplexer. (b) Harmonic suppression of the frequency doubler vs. the input frequency.

25 dB is achieved over the frequency range,[7] while the wanted second harmonic signal is in the range between 4 and 4.5 dBm over the complete frequency range.

The schematic of the active signal multiplexer is shown in Fig. 2(b). The circuit uses a cascode architecture with two common-source transistor pairs M_1/M_2 for two differential input signals V_{in1}/V_{in2} where the drain is connected to the source of one common-gate transistor pair M_3 with a common output V_{out}. The benefits of this active signal multiplexer in comparison to a passive power combiner is a much smaller chip area and also a possible signal amplification. The transistors M_1 and M_2 are again triple-well devices and the output of the common gate stage is matched to a differential 70 Ω transmission line (TLine) by a transformer, where the differential Tline is used to distribute the LO signal inside the chip (e.g., to the TX and RX channels). Furthermore, a neutralization capacitance M_n is implemented to improve the stability of the buffer and also the amplifier gain [19]. The four source nodes of the two differential input stages (M_1 and M_2) are connected to one common adjustable current source and the gate of M_3 is connected via a resistor R_1 to the supply voltage. To enable

[7]It should be mentioned that the suppression value of the first and third harmonics will be further improved by the bandpass behavior of the following stages.

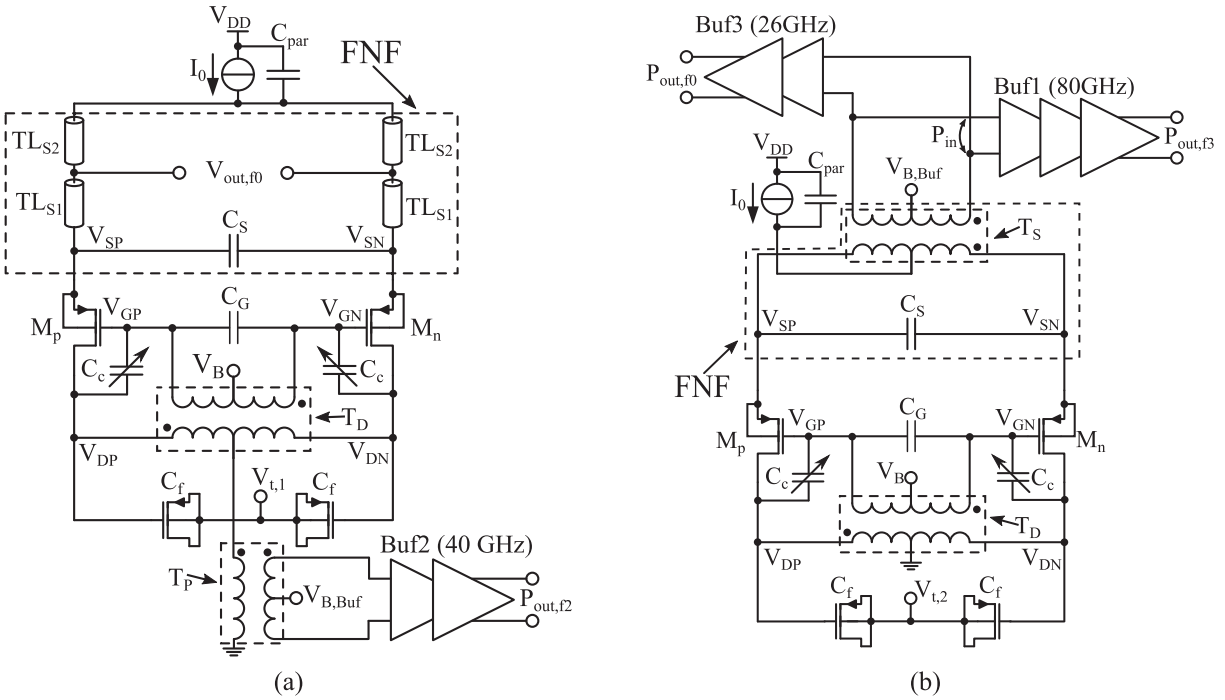

FIGURE 4. **Schematic of the implemented (a) 20 GHz push-push VCO (VCO1). (b) The 26 GHz VCO with 3rd harmonic extraction (VCO2).**

the input stage at port V_{in1}, the gates of M_1 are connected to the fixed bias voltage and the gates of M_2 are connected to VSS via transmission gates (which are not shown in Fig. 2(b) due to simplicity), while for enabling the input stage at port V_{in2}, the gates are controlled vice versa. In Fig. 3(a) the output power versus the input power for the multiplexer at 76 GHz and 81 GHz is shown and the saturated output power is about 4.5 dBm. A small signal gain of about 15 dB can be also extracted from the plot.

III. IMPLEMENTED VCO DESIGN AND TX INTEGRATION

A. 20 GHZ PUSH-PUSH VCO

The schematic of the implemented and manufactured 20 GHz push-push VCO (VCO1) is shown in Fig. 4(a). In comparison to the VCO of authors' previous publication [18], the performance of the new implemented VCO has been improved mainly by a new varactor design and thus the phase noise degradation at higher tuning voltages is solved [18]. Furthermore the design is extended by a second harmonic signal extraction at the common mode node by using an additional transformer (T_P).

The implemented VCO design uses pMOS transistors in the VCO core (M_p and M_n) because of a lower flicker noise and also a better reliability [20] while its RF performance is similar to the nMOS transistors. The tank of the VCO is built out of a transformer T_D, a varactor C_f, a switchable capacitance C_c and a fixed capacitance C_G. A transformer (T_D) coupled VCO architecture is implemented, because this architecture improves the loop-gain in the VCO core and therefore a higher oscillation amplitude and shorter commutation time is achieved, which results in a better phase noise [21]. Moreover, with the capacitance C_G, a second resonance in the VCO tank is generated, which creates a sharper pseudo-square oscillation voltage in the tank, thus improves the phase noise [21].

The varactor C_f, which is used for the fine tuning, is placed between the drain of M_p (V_{DP}) and the drain of M_n (V_{DN}). Furthermore the digital capacitor bank C_c, as second tuning possibility, which is used for the coarse tuning, is connected in parallel to the gate and the drain of the transistors M_p and M_n to further increase the overall tuning range [22]. This capacitor bank offers a coarse tuning possibility to compensate process and temperature variations whereas the FMCW (frequency modulated continuous wave) modulation is performed via the varactor C_f. An additional benefit of the digital capacitor bank in parallel to the gate and drain is making the implementation of a symmetric layout possible, since each bank could be placed directly on the left or right of M_p and M_n. It should be mentioned that the size of a digital capacitor bank is much larger in comparison to the analog varactor.

Furthermore, a flicker noise filter (FNF), as proposed by [11], [23], is implemented in our VCO to suppress the 1/f noise up-conversion to phase noise. The FNF structure is realized with the capacitance C_S and the transmission lines (TLines) TL_{S1} and TL_{S2}.

A second harmonic frequency signal is extracted from the VCO core via a transformer T_P, which is connected between the center tap of T_D and VSS. This 40 GHz signal is then amplified by Buf2 and fed to the input of a push-push frequency doubler. The fundamental signal ($V_{out,f0}$), which is needed for the divider chain (Buf4 and Div2), is extracted between the TLines TL_{S1} and TL_{S2}.

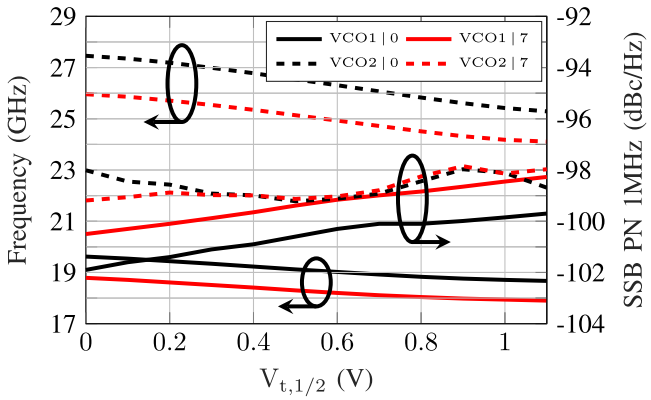

FIGURE 5. Simulated tuning range at the VCO core outputs and phase noise at 1 MHz offset frequency (normalized to 80 GHz) of the final implemented VCO1 and VCO2 vs. tuning voltage ($V_{t,1/2}$) at CT_{ctrl} of 0 and 7.

In order to improve the VCO pushing performance several approaches are implemented to minimize the VDD influence on the oscillation frequency, which is ensured by keeping the voltage at each node of the VCO core and also the VCO DC current independent on VDD variations. At the source of M_p and M_n, a current source for the VCO biasing is used which stabilizes the operation current of the VCO core and also the voltage potential at the source nodes. Moreover, the drain of M_p and M_n is connected to VSS via the transformers T_D and T_P and the gate bias voltage V_B is obtained via a resistor following a current, which is generated by a bandgap circuit, thus makes these nodes independent of VDD variations. Furthermore, the bulk voltage of M_p and M_n is directly tied to the source instead of VDD and the bulk of the varactor C_f is then directly connected to the tuning voltage $V_{t,1}$, which is mainly beneficial for low phase noise, but also for the pushing performance.[8]

Simulation Results of the phase noise, normalized to 80 GHz, at an offset frequency of 1 MHz versus the tuning range of the implemented VCO1 are shown in Fig. 5. A best phase noise of −101.9 dBc/Hz are simulated at $V_{t,1} = 0\,V$ and coarse tuning setting (CT_{ctrl}) of 0. The worst simulated phase noise is −98.2 dBc/Hz at $V_{t,1} = 1.1\,V$ and $CT_{ctrl} = 7$. The simulated overall frequency tuning range is about 1.73 GHz at the fundamental output and shown in Fig. 5. A maximum frequency of 19.62 GHz for a tuning setting of $V_{t,1} = 0\,V$, $CT_{ctrl} = 0$ and a minimum frequency of 17.90 GHz for a tuning setting of $V_{t,1} = 1.1\,V$, $CT_{ctrl} = 7$ are achieved.

B. 26 GHZ VCO WITH 3RD HARMONIC SIGNAL EXTRACTION

Similar to VCO1, a second 26 GHz VCO (VCO2) with a 3rd harmonic signal extraction and a larger fine tuning range is realized and the schematic is shown in Fig. 4(b). In comparison to VCO1, VCO2 features a similar VCO core, including the same oscillation transistors M_p and M_n, adjusted resonator elements T_D, C_f, C_c and C_G for the higher oscillation frequency and larger tuning range, but a new signal extraction method for the fundamental and harmonic frequencies.

In a magnetically coupled VCO, the 3rd harmonic signal could be directly extracted from the tank, since a strong third harmonic drain and source currents are available as mentioned in II II-A. A signal extraction between the drain nodes, as presented in [13], [17], [24], suffers from the degradation of the VCO performance due to the additional loading of the VCO tank (degrading the loaded quality factor of the tank). This degradation could be minimized by implementing a small buffer and thus less resistive loading on the VCO tank, but it limits the driving capability of the buffer. This means that a further buffer is needed to generate a large enough LO signal.

In VCO2 a new third harmonic extraction is presented, where the signal is extracted at the source nodes V_{SP} and V_{SN} instead of at the two drain nodes. To achieve this, a new FNF circuit with 3rd harmonic signal extraction is implemented and shown in Fig. 4(b), where the transmission lines (TL_{S1} and TL_{S2} in Fig. 4(a)) of the FNF structure is replaced with a transformer (T_S) and then a buffer connected to the secondary side of T_S. The transformer is optimized to generate a second high impedance at the third harmonic frequency while still providing a high enough input impedance at the fundamental to ensure the flicker noise filtering. The impedance at the third harmonic will then convert together with the third harmonic current of the core transistors (M_p and M_n) to a third harmonic voltage swing at the buffer input P_{in}. The output of the buffer (Buf1) in Fig. 4(b) is matched at 80 GHz to drive the following buffer.

With this extraction method, the oscillator tank (mainly located at the drains of the oscillation transistors) and the FNF with the signal extraction (connected to the source of the oscillation transistors) could be optimized independently, since the quality factor of the transformer (T_S) has a little impact on the VCO core performance only. It means, that the buffer-size or buffer-current in this new circuit structure has only a small impact on the oscillator performance and this enables the possibility to have a buffer with large operation current in order to deliver a large output signal. Fig. 6 shows the simulated input and output power level of Buf1 (e.g., with a tail current of 16 mA). Although the 1st and 3rd harmonic signal level at the input is almost the same, at the output the 3rd harmonic signal is about 55 dB higher.

Simulation Results of the phase noise, normalized to 80 GHz, at an offset frequency of 1 MHz versus the tuning range of the implemented VCO2 are also shown in Fig. 5. A best phase noise of −99.1 dBc/Hz are simulated at $V_{t,1} = 0\,V$ and $CT_{ctrl} = 7$. The worst simulated phase noise is −97.9 dBc/Hz at $V_{t,1} = 1.1\,V$ and $CT_{ctrl} = 7$. The simulated frequency tuning range is also shown in Fig. 5 and varies between 27.5 GHz and 24.1 GHz for a tuning setting of $V_{t,1} = 0\,V$, $CT_{ctrl} = 0$ and another tuning setting of $V_{t,1} = 1.1\,V$, $CT_{ctrl} = 7$. Due to the higher tuning range and

[8]It should be mentioned that the tuning range is reduces by this connection (details in Section III-C).

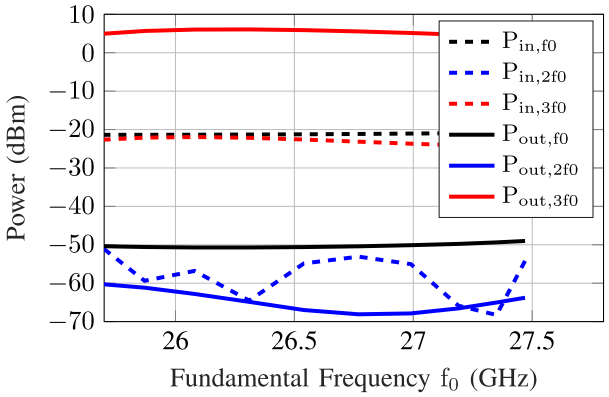

FIGURE 6. Simulated power level of the 1st, 2nd and 3rd harmonic at the input and output of Buf1.

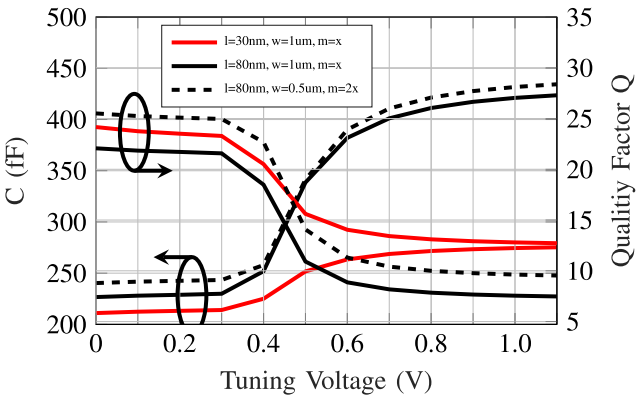

FIGURE 7. Simulated capacitance (C) and quality factor (Q) of a pMOS varactor versus the tuning voltage for different gate finger length (l), gate finger width (w) and multiplication factor (m).

higher oscillation frequency of VCO2, the phase noise is about 3 dB worse for the best phase noise case compared to VCO1.

C. IMPROVEMENT OF THE VARACTOR PERFORMANCE

For the varactor design, the necessary capacitance ratio (C_{max}/C_{min}) of the varactor over the tuning voltage range, required by the wanted frequency tuning range, has to be defined. In general, the C_{max}/C_{min} ratio of the varactor is mainly defined by the varactor process while the absolute capacitance is defined by the total area. Furthermore, it is well known that the quality factor (Q) and the capacitance ratio could be balanced by the varactor finger length with a fixed varactor process. On the one hand, a higher finger length of the varactor results in a higher C_{max}/C_{min} ratio and therefore a lager tuning range. On the other hand a longer finger length increases the series resistance of the varactor, which results in a lower quality factor. One comparison simulation with finger length of 30 nm and 80 nm is performed and shown in Fig. 7. The simulation shows a lowest quality factor of 13 (for 30 nm) and 7 (for 80 nm) at a tuning voltage of 1.1 V, while the capacitance ratio varies from 1.3 (for 30 nm) to 1.8 (for 80 nm).

Another consideration to obtain a higher quality factor is to reduce the width of a single finger,[9] while keeping the total area constant. In Fig. 7 also the capacitance and quality factor for two different finger width is shown without additional routing parasitic. A big quality factor improvement of about 2.5 for shorter finger width is observed ($w = 1\mu m$ and $w = 0.5\mu m$). But this shorter finger width also results in higher parasitic routing capacitance due to more varactor devices in parallel. However the overall performance with this shorter finger width is beneficial for the VCO design. Compared to the varactor in the previous publication [18] the finger width was reduced from 1 μm to 0.5 μm for our final implemented VCO.

Furthermore, the routing of the varactor array due to its big size has also a big impact on the varactor performance, therefore a graphical form of the varactor routing from our previous paper [18] and for the varactor of VCO1 are shown in Figs. 8(a) and 8(b).

It can be clearly seen, that the routing philosophy changed between them. For the routing in Fig. 8(a), the goal was to add as low as possible additional parasitic capacitance by the routing and therefore the connection to all drain and source nodes of the varactor devices was done vertically on the lower metal layers (M2 and M3) and after that, they are connected to the upper side of M7 of the varactor. Then left and right side M7 lines are connected to the symmetry plane (virtual ground) which is used for the VCO tuning port. This routing approach has benefits for a little higher C_{max}/C_{min} ratio and therefore for the tuning range, but the lower metal layers have extremely high series resistance.

Therefore another approach is used for the routing in Fig. 8(b), where the drain and source of the varactor device are now directly connected on top of the device to M7 and then horizontally connected to the other half of the varactor. This reduces the routing resistance dramatically but reduces a bit the tuning range. Since in the used technology the oxide thickness between the upper metal layers (M6, M7 and M8) and the varactor devices is relatively high, the additionally added coupling capacitance is still small enough and has only a little impact on the VCO tuning range. With this improvement and also the varactor width reduction, the worst quality factor at 1.1 V is increased from 4 to 9. It should be mentioned, that the finger width reduction and the enhanced layout routing contribute equally to the improvement of the quality factor in our varactor design.

Finally, that the bulk of the varactor should be connected directly to $V_{t,1}$ or $V_{t,2}$ instead of VDD, to have a clean voltage at the bulk. In this way, there isn't any VCO noise performance degradation due to supply noise or supply spikes, but it reduces the tuning range by about 5%.

[9]With this finger width reduction, the gate resistance is reduced a lot.

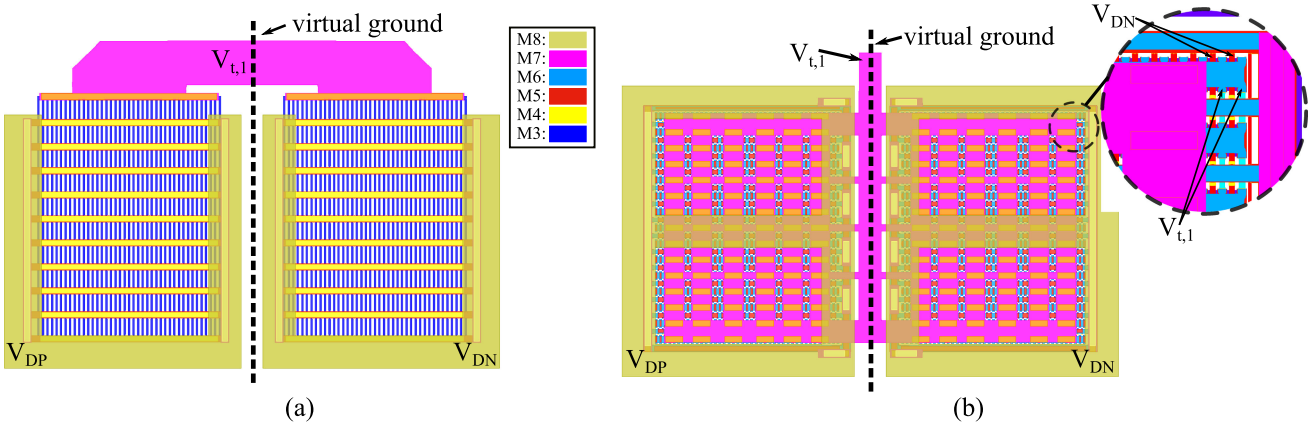

FIGURE 8. A graphical form of the routing in (a) the old varactor from [18]. (b) The new optimized varactor.

D. MINIMIZATION OF PA BLOCK IMPACT ON VCO PHASE NOISE

It is observed in the authors' first transmitter front-end implementation during the measurements, that the VCO phase noise has been dramatically degraded by about 3 dB while enabling the PA circuit.[10] Due to this new observation, an intensive investigation in simulations and experiments has been performed to understand this effect and to solve this issue.

1) SOURCES OF SUPPLY NOISE

In the radar system, several supply noise sources exists. The most obvious one is the supply generation devices (e.g., a power management IC (PMIC)). On the integrated radar chip, more circuit blocks are supplied with a single voltage supply source,[11] therefore all blocks sharing the same power supply domain could also add noise in the supply lines, especially the blocks with a high power consumption like the power amplifier.

In case of the presented transmitter chip, which is wire bonded on a PCB, the supply resistance caused by the bond wires, PCB routing lines, pad resistance and further on-chip routing resistance to the blocks as shown in Fig. 9(a) is called supply resistance R_V. This supply resistances R_V together with the noise originated from the active elements of the PA block could result in a low frequency noise at the internal chip supply line. To illustrate this, the noise on the supply is simulated for the given power amplifier for different supply resistances R_V and with/without current source RC noise filter similar to Fig. 9(b).[12] The result is shown in Fig. 10(a) and the supply noise due to the PA block at the internal chip supply node (VDD_{int}) without RC filtering reaches already $23\,nV/\sqrt{Hz}$ noise at supply line with only an $R_V = 0.1\,\Omega$ at 1 MHz offset frequency, but with enabled biasing filter the supply noise could be reduced to $4\,nV/\sqrt{Hz}$ at same conditions. This simulation results can clearly explain the root cause of the phase noise degradation mentioned at the beginning of this section.

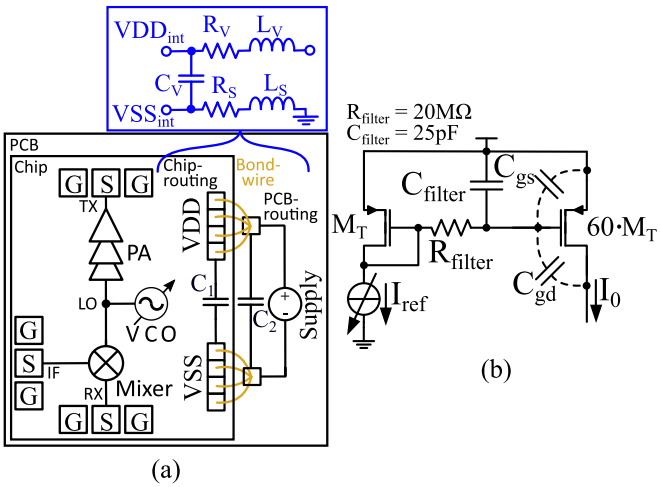

FIGURE 9. (a) Block diagram of the supply connection to a transceiver chip. (b) Schematic of a pMOS current source with RC low pass noise filter.

2) SUPPLY NOISE INFLUENCE ON VCO PERFORMANCE

Designing a VCO with a large continuous tuning range in an advanced CMOS technology will result in a high K_{VCO} (the derivative of the oscillation frequency over the tuning voltage), since the maximum allowed tuning voltage of the varactor is limited. This high K_{VCO} makes the VCO very sensitive to any noise either from the tail current source, the gate biasing circuits or also the supply noise.

In this section the tail current mirror is implemented as the schematic in Fig. 9(b). The noise performance in this current mirror at 1 MHz offset frequency is mainly dominated by the flicker noise of the MOSFET devices. This high noise can be reduced with larger transistor width, but it will result in a large area consumption. Furthermore, in order to save current consumption, large multiplication factors are used inside the

[10]The phase noise measurement of the transmitter was done on-wafer at the 77 GHz TX output.

[11]To reduce product costs and system complexity, it is intended to use as few supply domains as possible, ideally only one.

[12]In the simulation the external supply source noise is assumed to be zero.

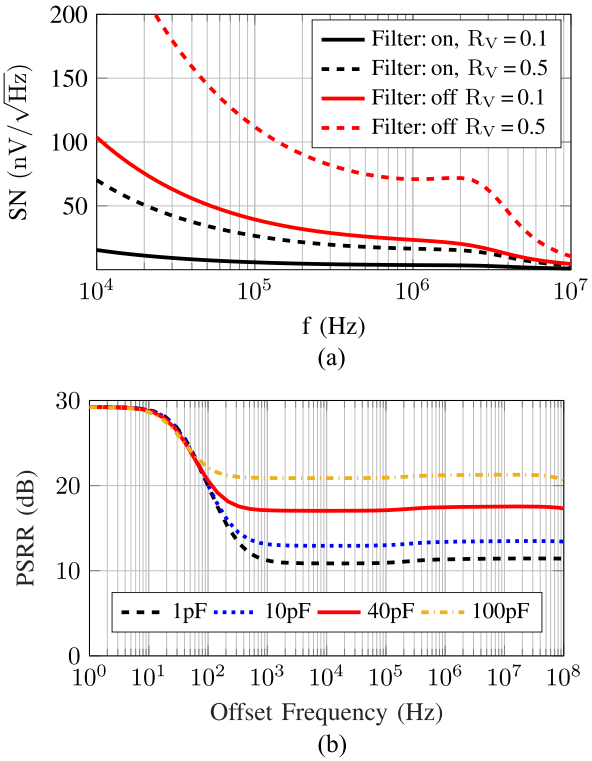

FIGURE 10. (a) Simulated supply noise generated by the PA at the node VDD_{int} in Fig. 9(a) for different values of R_V and with/without RC biasing filter. (b) Simulated PSRR of the current mirror from Fig. 9(b) for different values of C_{filter}.

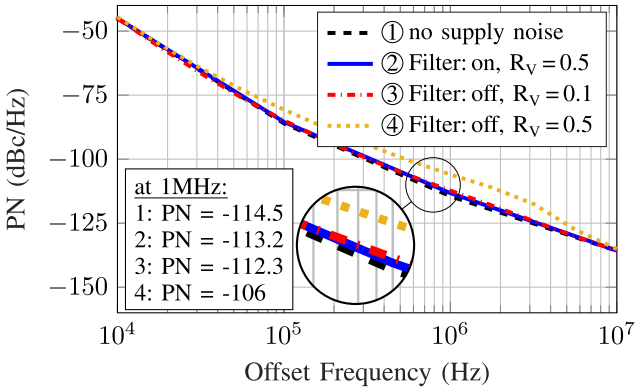

FIGURE 11. Simulated VCO phase noise with the supply noise from Fig. 10(a), generated by the power amplifier.

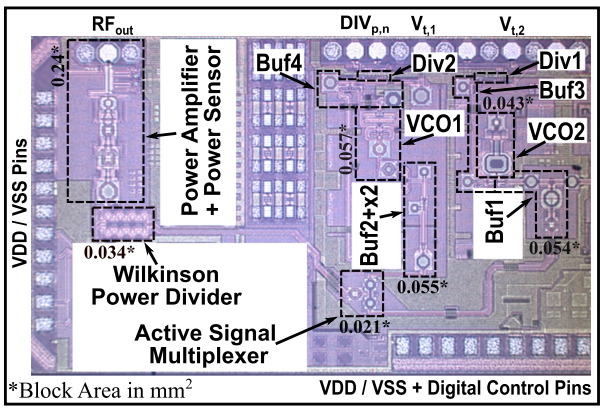

FIGURE 12. Chip-photography of the implemented transmitter.

mirrors to get the high tail currents in the circuits. Therefore, all the noise from the previous mirror stages are multiplied by the scaling factor and it results in a high VCO tail current noise. To overcome this issue, a RC low pass filter consisting of R_{filter} and C_{filter} is realized in the last mirror stage to filter out all the noise from the reference currents. In order to filter the noise efficiently, this filter should feature a cut off frequency as low as possible, e.g., 1 kHz. In order to have an area-efficient filter layout, the preference is to have a resistance of R_{filter} as high as possible to make a small capacitance for a fixed cut off frequency, since a large capacitor consumes much more chip area in comparison to a higher resistance. Furthermore, to avoid any large voltage drop across this high resistance (R_{filter}), thick oxide pMOS devices are used for the last current mirror stage, due to their much lower gate leakage current. However, it requires a higher drain source voltage to ensure a saturated operation of the current mirror.

It should be mentioned that the minimum needed filter capacitance C_{filter} not only determines the corner frequency of the filter, but also has big impacts on the power supply rejection ratio (PSRR). Fig. 10(b) shows the PSRR of the current mirror for different values of C_{filter} and the PSRR performance above the cut off frequency is improved for higher values of C_{filter}. The reason for it is that in case a supply noise is present on chip, then a minimal V_{gs} variation is achieved if C_{filter} is large enough in comparison to C_{gd} of the output transistor $60 \cdot M_T$ and in this way the gate voltage follows the supply changes. Thus, the output current is not changed due to the almost constant V_{gs}.

So for the final transmitter integration, both the VCO and PA are optimized for best PSRR performance. For example the power amplifier and the buffer stages are optimized for low noise which will result in lower supply noise at the supply line. Additionally an on-chip LDO is placed between the external supply and the VCO to further improve the power supply rejection.

To show the phase noise degradation due to the generated supply noise by the PA, a VCO simulation is performed where the supply noise from the PA in Fig. 10(a) is used. The phase noise versus the offset frequency is shown in Fig. 11 and for the highest supply noise the PN at 1 MHz degrades by about 8 dB. For the case mentioned at the beginning of the section, the supply noise in Fig. 10(a) with R_V of 0.5 and enabled RC filter is considered for the VCO phase noise simulation. A PN degradation of 1.3 dB is expected from simulation and the difference to the measured 3 dB degradation is caused by the supply noise from other buffers which are not included in Fig. 10(a).

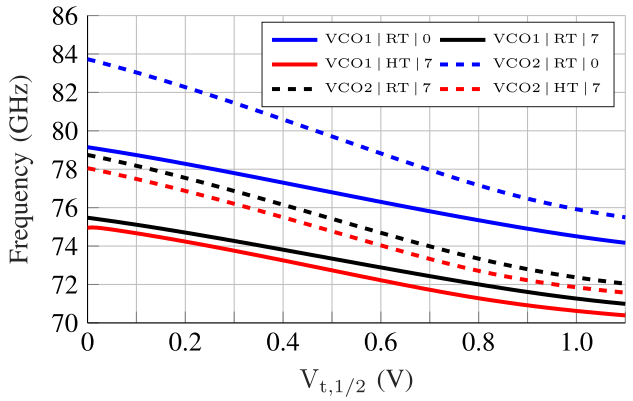

FIGURE 13. Measured frequency at RF_{out} versus the tuning voltage $V_{t,1/2}$ at temperatures of 25°C (RT) and 125°C (HT) and a coarse control setting (CT_{ctrl}) of 0 and 7 for VCO1 and VCO2.

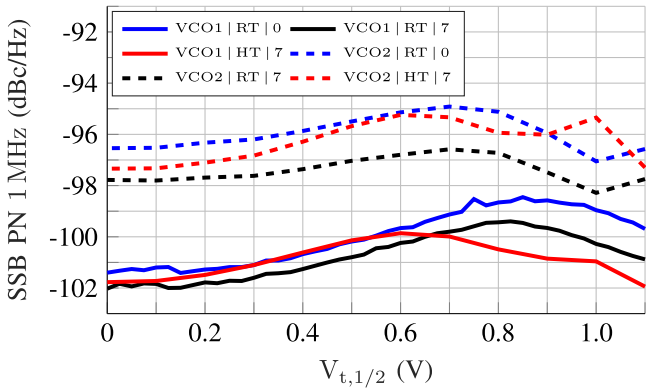

FIGURE 14. Measured phase noise (PN) at 1 MHz offset frequency at RF_{out} versus the tuning voltage $V_{t,1/2}$ at temperatures of 25 °C (RT) and 125 °C (HT) and a coarse control setting (CT_{ctrl}) of 0 and 7 for VCO1 and VCO2.

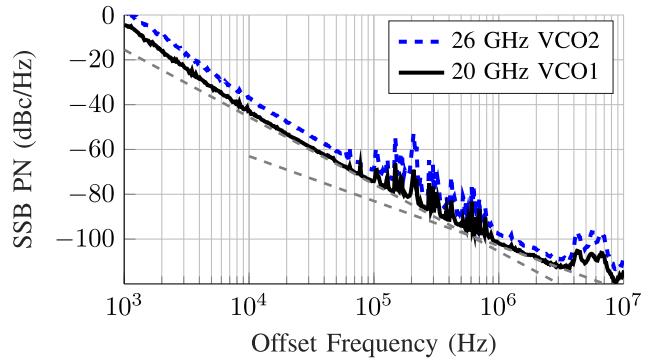

FIGURE 15. Measured phase noise versus offset frequency at $V_{t,1/2} = 0$ and $CT_{ctrl} = 4$ (The spurs between 100 kHz/3 MHz and 1 MHz/10 MHz are caused by the measurement environment).

IV. EXPERIMENTAL RESULTS

A photography of the presented transmitter chip manufactured in a TSMC 28 nm technology is shown in Fig. 12 and the overall shown chips size is $2565\,\mu\text{m} \cdot 1530\,\mu\text{m}$. Since the complete chip is integrated with other building blocks and device test-structures, the presented blocks in this paper are

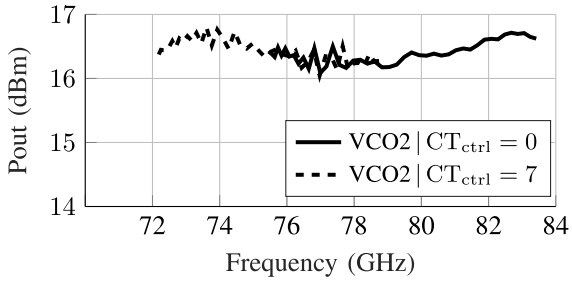

FIGURE 16. Power at the output of the power amplifier (RF_{out}) versus the frequency for VCO2 at a coarse tuning setting (CT_{ctrl}) of 0 and 7.

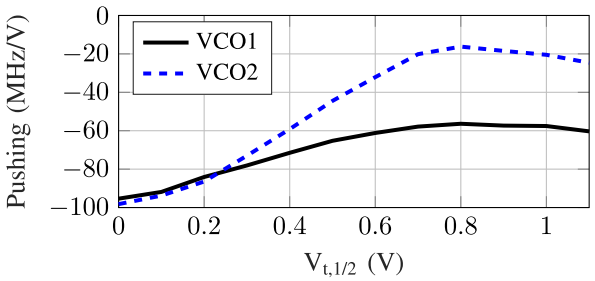

FIGURE 17. Measured VCO pushing at RF_{out} versus the tuning voltage $V_{t,1/2}$ at a temperature of 25 °C and a coarse control setting (CT_{ctrl}) of 4 for VCO1 and VCO2.

marked in Fig. 12 with dashed boxes and the occupied area of the corresponding RF circuits is also shown. The RF core of VCO1 together with Buf2 and the Doubler consumes an area of $0.112\,\text{mm}^2$ whereas the RF core of VCO2 and Buf1 consumes an area of $0.097\,\text{mm}^2$. The Active Multiplexer, the Wilkinson Divider and the Power Amplifier occupies an area of $0.021\,\text{mm}^2$, $0.034\,\text{mm}^2$ and $0.24\,\text{mm}^2$ respectively. The power consumption of the whole transmitter is with 855 mW/857 mW for VCO1/VCO2 from a single 2.1 V power supply and it is almost identical for both VCO chains. The core current consumption for both VCO cores is 50 mA from the same 2.1 V supply, but the voltage remaining for the core transistors is still 0.9 V which ensures the device reliability of the VCO core whereas the remaining 1.2 V are used by the LDO and the current source. The RF core of Buf1 and Buf2 consumes each 150 mW and the RF core of the active signal multiplexer and the power amplifier consumes 40 mW and 460 mW.

The complete TX chip is measured on wafer with DC and E-band probe tips. The VCO characteristic (frequency tuning range and phase noise) are measured with a Keysight E5052b signal source analyzer and the output power is measured with a E-Band power sensor and power meter.

In Fig. 13 the VCO tuning characteristic at the output of the power amplifier (RF_{out}) is shown for VCO1 and VCO2. For VCO1 the frequency can be continuously tuned from 79.15 GHz to 74.17 GHz and 75.47 GHz to 70.99 GHz for a coarse tuning setting of 0 and 7 respectively at a chuck temperature setting of 25 °C. This means an average continuous tuning range of 4.75 GHz and a coarse tuning range of

TABLE 1. Performance Comparison of State-of-the-Art mmWave Frequency Generators

	This Work VCO1		This Work VCO2		DCO [13]	DCO [24]	VCO [25]	HBT VCO [26]
Technology	28 nm CMOS		28 nm CMOS		40 nm CMOS	16 nm FinFET	28 nm CMOS	350 nm BiCMOS
Supply Voltage [V]	2.1	0.9 [a]	2.1	0.9 [a]	0.7	0.85	0.9	3.3
Frequency Range [GHz]	71 – 79.2		72 – 83.7		48 – 62.5	68 – 84	56 – 65	56 – 65
Output Power [dBm]	16.5		16.5		5	5	10	4
Best PN @ 1 MHz [dBc/Hz]	-102		-97.5		-100.1	-97.5	-99.4	-105
Best PN @ 1 MHz norm. to 77 GHz [dBc/Hz]	-101.7		-97.6		-97.5	-97	-96.6	-103.4
VCO Core Power Consumption [mW]	105	45 [a]	105	45 [a]	13.5	10	23	—
FoM [b] @ 1 MHz [dBc/Hz]	-179	-183 [a]	-175	-179 [a]	-184	-185	-181	—
VCO multiplication	x4		x3		x3	x3	x4	x2
Signal Generation	Push-Push + Doubler		Third Harmonic		Third Harmonic	Third Harmonic	Push-Push + Doubler	Push-Push

[a] Effective VCO core voltage without LDO and current source.
[b] $\mathrm{FoM} = \mathrm{PN} - 20 \cdot \log(f_{osc}/f_{offset}) + 10 \cdot \log(P_{DC}/1\ \mathrm{mW})$

3.2 GHz and therefore the total tuning range is 8.2 GHz. At a temperature of 125 °C, the frequency drops on average by 650 MHz compared to the frequency at 25 °C with a small temperature frequency drift of 65 MHz/Kelvin. Thus a continuous tuning range over the temperature between 25 °C and 125 °C of 4 GHz is achieved which is large enough for LRR application.

The continuous tuning range of VCO2 at 25 °C for a coarse tuning setting of 0 and 7 is from 83.73 GHz to 75.50 GHz and 78.74 GHz to 72.04 GHz respectively. A total tuning range of 11.7 GHz is achieved with a fine tuning and coarse tuning range of 7.5 GHz and 4.2 GHz respectively. The frequency drift over temperature is almost the same as that for VCO1.

The phase noise at 1 MHz offset frequency of VCO1 and VCO2 at 77 GHz TX output is shown in Fig. 14. For VCO1 at a temperature of 25 °C the best phase noise of −102 dBc/Hz is achieved at a tuning voltage of 0 V and a coarse tuning setting of 7, and the worst phase noise is −98.5 dBc/Hz at a tuning voltage of 0.9 V and a coarse tuning setting of 0. At 125 °C the phase noise is degraded at 0 V only by 0.2 dB and the worst phase noise is 0.5 dB better compared to that at 25 °C. This is mainly due to an increasing PTAT referenced tail current for higher temperatures and therefore even higher oscillation amplitude in the VCO core. Compared to the previous presented VCO in [18], the worst case phase noise is improved by 1.5 dB due to the improved varactor design shown in Section III-C.

At a temperature of 25 °C the best/worst phase noise of −98.3 dBc/Hz / − 94.9 dBc/Hz for VCO2 is achieved at a tuning voltage of 1 V/0.7 V respectively. In the complete VCO tuning range the phase noise is varying by 3.3 dB at 25 °C. For high temperatures of 125 °C the phase noise is degraded by maximal 1.6 dB. The above achieved VCO tuning range and phase noise is sufficient for the LRR and SRR applications.

The measured phase noise at 1 MHz offset of VCO1 fits very well to the simulated phase noise in Fig. 5, where the deviation for the best phase noise and the worst phase noise condition is less than 0.5 dB. For VCO2 the deviation between the simulated and measured phase noise is also less than 1 dB for the best phase noise condition, whereas in the worst condition the measurement shows a 3 dB higher phase noise. The overall simulated tuning range for VCO1 is about 6.9 GHz which is a bit underestimated, compared to the 8.2 GHz (19% higher) from the measurement. The same behavior is also observed in VCO2 where the overall simulated tuning range of 10.1 GHz is also underestimated in comparison to the measured 11.7 GHz (16% higher).[13]

Furthermore, the SSB phase noise versus the offset frequency is shown in Fig. 15 for both VCOs at $V_{t,1/2} = 0$ and $CT_{ctrl} = 4$. The 1/f noise corner frequency of VCO1 and VCO2 could be extracted from the plots and they are around 600 kHz and 800 kHz, respectively. This shows the effective suppression of the 1/f noise up-conversion [17]. The output power at RF_{out} is shown in Fig. 16 and is in the whole frequency range between 16.25 and 16.75 dBm. Compared to the similar PA design already presented in [16] the output power is around 2.5 dBm less and the reason for that is the integration of the directional coupler and the power sensor at the output, but this could be further improved in a second design iteration.

Finally, Fig. 17 shows the pushing of VCO1 and VCO2 versus the tuning voltage at 25 °C and $CT_{ctrl} = 4$. Over the whole tuning rang an excellent pushing performance better than −100 MHz/V is achieved for both implemented VCOs, which confirms our design considerations in III-A.

[13]The root cause of this discrepancy is mainly due to the used varactor model, which systematically underestimates the capacitance ratio and thus the frequency tuning range. This was confirmed by measurements of varactor test structures, which showed a capacitance ratio is about 15% higher than that of the device model.

Table 1 shows an overview performance comparison of the state of art VCOs in literature with our new implemented VCOs. It can be seen that our TX chip has achieved the highest output power and the lowest VCO phase noise variations over the complete VCO tuning range. The calculated VCO FoM (with the effective VCO core supply voltage) of the implemented VCO1 is among the best VCO performance for the analog voltage controlled oscillators,[14] while the implemented VCO2 shows a 4 dB degradation of the FoM due to a higher oscillation frequency, larger VCO tuning range and larger K_{VCO}. The power consumption of the presented VCOs is relatively high in comparison to other VCOs in Table 1 because the design focus is mainly on the absolute low VCO phase noise. However, this power consumption in the VCO core is only a small percentage of the total power consumption of the complete radar chip. Therefore the radar chip can afford this power consumption in order to achieve the best class VCO performance.

V. CONCLUSION

A new TX architecture with dual VCO cores and a third harmonic signal extraction is presented for automotive applications. In addition, the root causes of the performance deterioration due to the integration of all TX building blocks in one TX chip are analyzed and the solutions to get rid of this degradation are proposed. The achieved VCO frequency tuning range of 11% (VCO1) and 15% (VCO2) of the oscillation frequency as well as a best phase noise of -102 dBc/Hz from VCO1 and -98.3 dBc/Hz from VCO2 at 1 MHz measured at TX output are among the best performance VCOs in publication. A record pushing performance of $< \pm 100$ MHz/V for both VCOs is very beneficial for the system application. The demonstrated transmitter performance including the VCO tuning range, the low phase noise and the high PA output power >16 dBm shows the feasibility of CMOS technology for automotive LRR and SRR applications.

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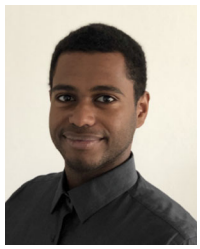

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