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Design of an Absorptive High-Power PIN Diode Switch for an Ultra-Wideband Radar

DEEPAK N. ELLURU (Graduate Student Member, IEEE), ABHISHEK K. AWASTHI (Member, IEEE), S. PRASAD GOGINENI (Life Fellow, IEEE), DREW TAYLOR (Member, IEEE), ALI SHAHABI, ANDREW N. LEMMON (Senior Member, IEEE), CHANGHYUN CHUNG, AND JOOHAN LEE

(Regular Paper)

Department of Electrical and Computer Engineering, Remote Sensing Center, The University of Alabama, Tuscaloosa, AL 35487 USA

CORRESPONDING AUTHOR: Abhishek K. Awasthi (e-mail: abhishek.awasthi.ec@gmail.com).

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ABSTRACT This paper details the development of a low-loss, PIN diode single-pole double-throw (SPDT) absorptive switch for an ultra-wideband radar. The fabricated switch operates with a peak power of 200 watts at a 10% duty cycle. It has an insertion loss of less than 0.8 dB, a return loss greater than 19 dB, and isolates the transmitter and receiver beyond 37 dB over the frequency band (170 MHz-470 MHz) for sensitive radar measurements. An external RF limiter and a low-power CMOS switch at the receiving end are used to reduce video leakage from the PIN diode switch and enhance the isolation up to 80 dB. In addition, a fast-switching MOSFET-based PIN diode driver circuit is designed with a dead-time control circuit to minimize the cross-conduction currents for the PIN diode switch. The rise and fall times for the PIN diode switch are less than 200 ns. The switch-driver includes integrated low-noise power supplies that generate −50 V, 15 V, and 5 V from a common rail 50 V input source.

INDEX TERMS Driver, MOSFET, PIN diodes, radar, SPDT, switch, T/R switch.

I. INTRODUCTION

Polar regions are undergoing rapid changes attributed to rising temperatures, and sea levels have been increasing steadily over the last decade. According to recent studies [1]–[4], these changes are ascribed to significant contributions from the large ice sheets of Greenland and Antarctica. Several surface and airborne measurements have been carried out in Greenland and polar regions to help better understand these changes [5]–[6]. To support these efforts, we are developing an ultra-wideband (UWB) multi-channel high-power VHF radar for airborne measurements of the polar ice [7]. The radar is designed to sound more than 4.5 km thick ice, map internal layers from the surface to the bed, and image the ice-bed interface over a swath of 500-1000 m. The return loss for internal layers close to the bed can be as high as 90 dB, and this requires a radar with a very high sensitivity to map these layers. The radar obtains high sensitivity by employing a large power-aperture product, pulse compression, high pulse repetition frequency (PRF), and coherent processing. Any spurious signals injected by the transmitter into the receiver during the reception period will degrade radar sensitivity. The power amplifiers we used have a large turn-off and turn-on times. We needed a high-power transmit-receive (T/R) switch to protect the receiver during transmission and minimize noise and radio frequency interference (RFI) signals coupled to the antenna and injected into the receiver. We also needed to terminate the high-power amplifiers in a matched load to prevent oscillations and damage. We designed and developed a high-power absorptive T/R switch with high isolation and very low-loss for use with ultra-wideband radars. The switch allowed us to develop a highly sensitive radar to sound and image about 5-km thick ice with fine resolution.

Rodriguez *et al.* [8] demonstrated a PIN diode T/R switch based on a balanced duplexer configuration to achieve high isolation between the transmitter and receiver. However, this switch has high insertion loss and slow switching speed. Also, the switch used a driver designed using bipolar junction transistors with lower negative bias voltage. Johansen [9] designed a PIN diode driver for an MRI application that used a FET operating at a lower negative voltage with additional

current limiting circuitry. A Transmit Array Spatial Encoding (TRASE) [10] application that used short pulses of high-power signal for achieving high-resolution spatial encoding was developed using PIN diodes switching coil circuits. An extensive study on PIN diode driver circuits [11] was also conducted by modifying the driver circuitry to optimize PIN diode switching times using BJTs and biasing them at different conditions. Several other studies have also involved high power switches for radar applications [12]–[14]. Various PIN diode SPDT switch configurations are discussed in [15]–[16].

Most commercial-off-the-shelf (COTS) high-power switches use series and shunt PIN diodes to terminate isolated ports in a very low impedance by forward-biasing the shunt diode in a high impedance by reverse-biasing the series diode. The low impedance termination of the high-power amplifier (PA) may result in failure or oscillations. We developed a high-power absorptive PIN diode switch with a very low insertion loss and high isolation.

This paper discusses the design and analysis of a low-loss, PIN diode absorptive switch with an integrated MOSFET-based driver. The switch design addressed the low impedance termination of shunt diode to prevent the high-power amplifier from being terminated in a low impedance load. The switch transmitting and receiving ports are terminated in a 50-ohm matched load irrespective of the switch state (Transmit to Antenna or Receive to Antenna). The insertion loss of the T/R switch is low (∼0.6 dB) which improves the overall sensitivity of the radar. A new fast PIN diode driver circuitry complementing the SPDT switch is also designed using a push-pull FET configuration with a dead time circuitry for reducing the cross-conduction currents at the input stage and biasing voltage sufficient to handle peak RF power of 200 W. The switch also includes an ultra-low-noise power-supply to reduce any supply-generated RFI that can reduce radar sensitivity. The driver circuit provides fast switching, higher current handling, improved efficiency, and more flexibility to drive multiple PIN diodes simultaneously. The driver can also be modified for higher reverse bias voltages to handle high power. A custom-built low noise −50 V 10-Watt DC-DC power convertor is developed using an isolated flyback topology for sinking PIN diode reverse currents. The SPDT switch designed will be used in UWB VHF radar shown in Fig. 1. The radar is designed to operate from 170 MHz to 470 MHz over a bandwidth of 300 MHz, peak-power handling capacity 200 W per channel, Isolation (I) $>$ 37 dB, Insertion loss (IL) $<$ 1 dB, and fast switching. The high-power PIN diode switch is followed by an off-the-shelf low-power CMOS switch to further enhance isolation between transmitter and receiver by up to 80 dB.

In the next section, we describe the details regarding the development of the PIN diode models and attributes, followed by SPST and SPDT switch designs. The design of the driver is also discussed in detail, followed by tests and measurements. Finally, we conclude by integrating the switch with the radar system for high power and optical delay line tests to validate the switch performance for sensitive radar measurements.

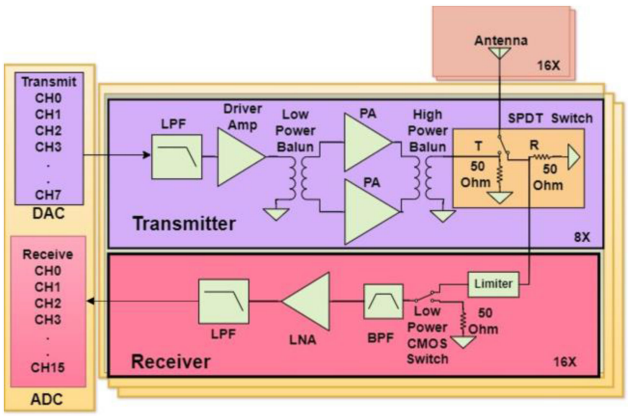


FIGURE 1. Block diagram of VHF radar system incorporating high power SPDT switch.

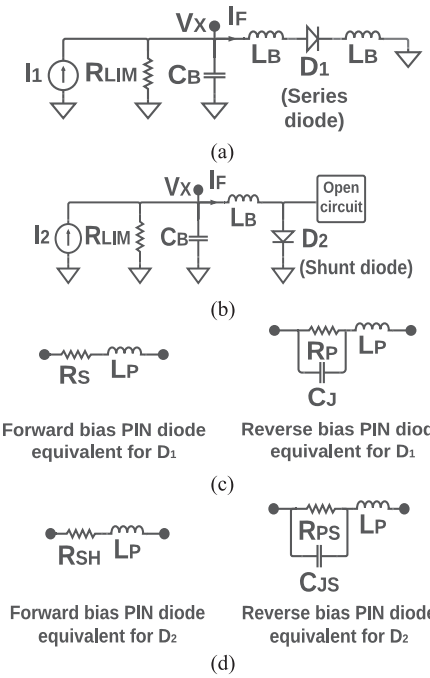


FIGURE 2. (a) Bias network for series diode. (b) Bias network for shunt diode. (c) Equivalent for D_1 in forward and reverse bias. (d) Equivalent circuit for D_2 in Forward and reverse bias.

II. DESIGN ASPECTS OF THE PIN DIODE BIASING CIRCUIT

A MACOM semiconductor MEST2G-150-20-CM26 (series) and MSWSH-100-30 (shunt) silicon PIN diode are used in this design. The diode parameters are extracted from the specification sheet of the manufacturer. Fig. 2(a) and (b) depict the PIN diode bias network models for series and shunt diodes D_1 and D_2. The forward bias and reverse bias equivalent circuits for diodes are represented in Fig. 2(c) and (d). The switching speed (T_{FR}) [17]–[18] of the diode from forward bias (FB) to

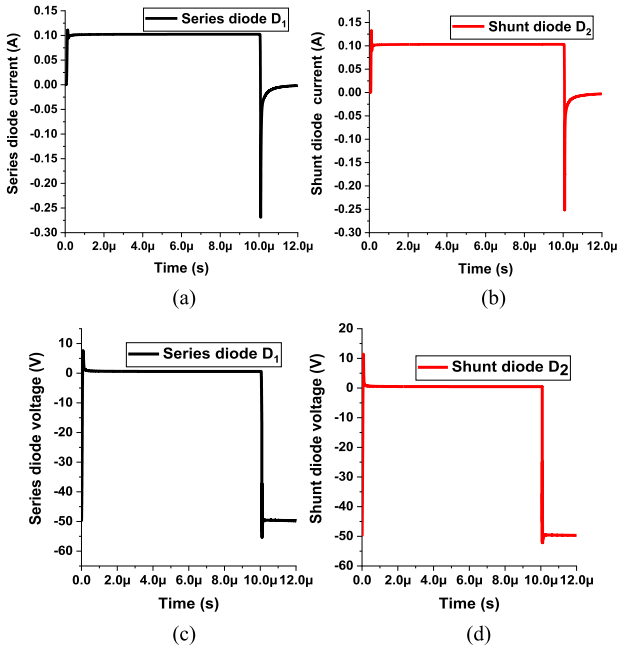


FIGURE 3. Diode simulated responses when $I_F = 100$ mA. (a), (b) Current step response of diodes. (c), (d) Voltage step response for the diodes.

TABLE 1. Calculated T_{FR} for the PIN Diodes

Diode	W (μm)	R_S (100 mA)	calculated τ (μs)	$\frac{I_F}{I_R}$	T_{FR} (ns)
D_1 (Series)	115	0.6	1.130	100/261	359.4
D_2 (Shunt)	80	0.4	820	100/251	274

reverse bias (RB) is given by

$$T_{FR} = \tau \ln\left[1 + \frac{I_F}{I_R}\right]. \tag{1}$$

The diodes are biased with a forward current (I_F) of 100 mA with a low series resistance (R_S). I_F is controlled by using a current limiting resistor (R_{LIM}). It is set to 150 Ω when 15 V is applied at the input of the bias section. A lower I_F reduces T_{FR} but increases R_S and consequently increases the RF power loss ($P_{loss} = 0.5 I_{RF}^2 R_s$). I_{RF} is the peak RF current through the diode. The carrier lifetime (τ) is calculated using the following

$$\tau = \frac{W^2}{(2\mu_T) I_F R_S}. \tag{2}$$

where W is the width of the intrinsic barrier region of the diode and μ_T is the ambipolar mobility.

Caverly SPICE models [19] are used for the diodes D_1 and D_2 and simulated using the Keysight ADS tool. The simulated diode currents and voltages are as shown in Fig. 3(a), (b), and (c), (d). T_{FR} for diodes is calculated using (1) and shown in Table I. D_2 settles faster than D_1 because of the shorter

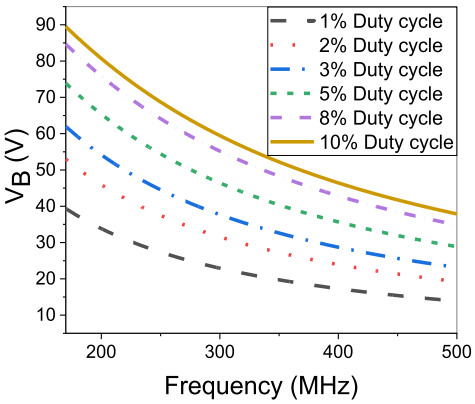


FIGURE 4. Magnitude of the RB voltage (V_B) applied versus frequency at varying δ.

carrier lifetime. The speed of the diode (T_{RF}) from reverse bias (RB) to forward bias (FB) depends upon the PIN diode driver performance, and W. Other critical parameters when operating in RB are the stored charge in junction capacitance and reverse bias resistance of the PIN diode. R_P and R_{PS} are several orders higher in magnitude for equivalent circuits, as shown in Fig. 2(c) and (d). $C_J = 0.19$ pF and $C_{JS} = 0.56$ pF for D_1 and D_2. The parasitic inductance (L_p) is negligible at low frequencies and ignored in simulations over our radar frequency range. Another aspect for proper operation of the PIN diode in high power RF application is the magnitude of the applied reverse bias voltage (V_B) [20]–[21]. V_B depends on the peak RF voltage (V_{RF}), duty cycle (δ), frequency (f), and width of the intrinsic barrier (W) region and is calculated [20] by the following

$$|V_B| = \frac{|V_{RF}|}{\left\{1 + \left[a\left(1 + \sqrt{1 + (b)^2}\right)\right]^2\right\}^{0.5}}. \tag{3}$$

where a and b are diode coefficients.

$$a = \frac{\pi f W^2}{0.95 \mu V_{RF} \sqrt{\delta}},\ b = \frac{0.95 \mathrm{u} V_{RF} \sqrt{\delta}}{W v_{sat}}. \tag{4}$$

The operating condition of the selected diodes is well below the avalanche breakdown (V_{BR}) to avoid punch through. The radar operates at 1% δ (duty cycle) and 1-μs pulse for mapping near-surface ice layers and shallow ice of 1-km depth. It operates with 5% to 10% δ and 5 or 10 μs pulse to map internal ice layers and sound more than 1-km thick ice at a pulse repetition interval (PRI) of 100 μs. The peak RF voltage for 200 W peak power is 141.2 V. The negative bias is critical for the shunt diode (D_2) compared to D_1 because of the smaller intrinsic barrier width. The RB voltage is plotted against frequency at different δ for $V_{RF} = 141.2$ V, as illustrated in Fig. 4. As the frequency increases, the bias voltage reduces. However, with the increase in δ, the bias voltage increases significantly at the lower end of the frequency spectrum. According to (3), the bias voltage is valid for a single tone signal, and at 10%,

V_B is 89.4 V at 170 MHz. In a pulse compression radar, transmit signal frequency varies over time. The transmit signal chirp (170 MHz–470 MHz) is divided into ten equal time frames of 1 μs each for a 10 μs chirp to determine bias voltage requirement. As a consequence, the δ for the corresponding frequencies in each segment is small, and the PIN diode can be operated in a conditionally safe mode at lower frequencies. For example, the first frequency segment, 170-200 MHz, lasts for only 1 μs in the 10 μs duration chirp. With an effective δ of only 0.01, V_B is -40 V. It is unconditionally safe to operate the switch at 53 dBm with a bias voltage -50 V in this frequency segment. Similarly, the second segment, 200 MHz-230 MHz, lasts for another 1 μs, and V_B is -35 V at the start of the frequency segment (200 MHz) and is unconditionally safe to operate the switch at 53 dBm with a bias voltage of -50 V. However, V_B becomes less stringent with the successive progression of the frequency segments. A Tukey window applied to the transmit signal to reduce Fresnel sidelobes causes a further reduction in the required V_B at the lower frequencies. The driver and -50 V supply are designed to handle RF voltages from 150 to 200 W. Determination of current (I_F), switching times, and negative bias voltage (V_B) for low RF distortion is crucial before proceeding to the bias network design, switch design, and the PIN diode driver circuit.

The bias network plays a crucial role in the switching performance and RF-DC isolation between the switch and the driver. Bias network shown in Fig. 2(a), (b) forms a parallel RLC circuit. The time-domain responses of these circuits are analyzed by applying nodal analysis at V_x for diodes D_1 and D_2. Diodes D_1 and D_2 in Fig. 2(a) and, (b) are replaced with the forward bias equivalents shown in Fig. 2(c) and, (d).

A generalized second-order differential equation is obtained after solving for the currents which, is of form

$$I' = \frac{\partial^2 I_F}{\partial t^2} + \left(\frac{R_S}{\alpha L_B} + \frac{1}{R_{LIM}}\right)\frac{\partial I_F}{\partial t} + \frac{\left(\frac{R_S}{R_{LIM}} + 1\right)}{\alpha C_B L_B}. \quad (5)$$

R_S is replaced by R_{SH} for D_2 in equation (5), where I' is

$$I' = \frac{I_i}{\alpha C_B L_B}.$$

Here i = 1, $\alpha = 2$ for D_1; and i = 2, $\alpha = 1$ for D_2 for the bias networks in Fig. 2(a), (b). Initial conditions are applied to determine the natural frequency response of the circuit. L_B is the RF choke for RF-DC isolation, and C_B is the decoupling capacitor. In combination, L_B and C_B form a low pass filter. Here $I_F = 100$ mA when R_{LIM} is set at 150-Ω. $R_S = 0.6$ Ω and $R_{SH} = 0.4$ Ω for the diodes. Under the source free ($I' = 0$) condition, (5) becomes a homogeneous differential equation which is

$$s^2 + sy + z = 0. \quad (6)$$

The constants y and z are

$$y = \left[\frac{R_s}{\alpha L_B} + \frac{1}{R_{LIM} C_B}\right], \; z = \frac{\frac{R_s}{R_{LIM}} + 1}{\alpha C_B L_B}.$$

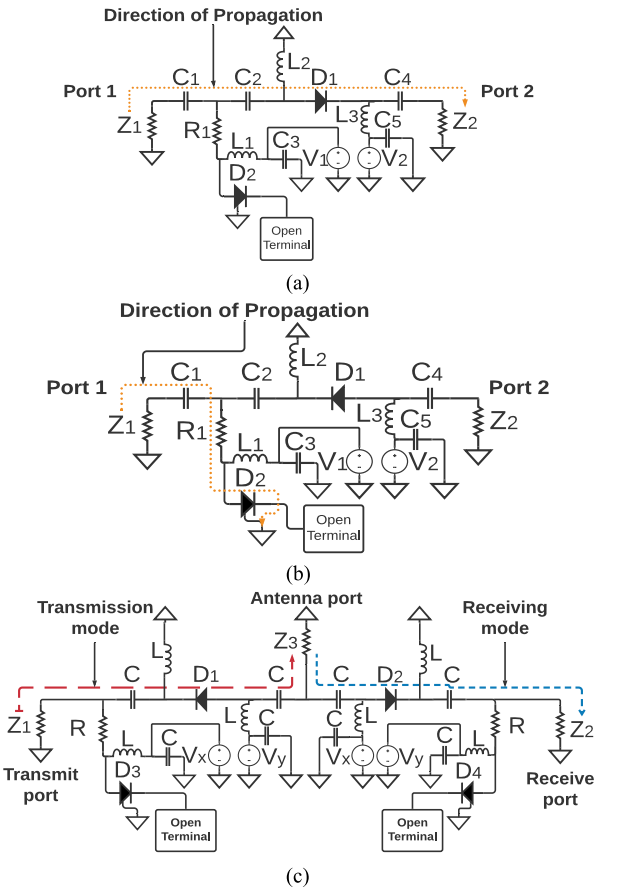


FIGURE 5. Switch configuration. (a) SPST switch in the transmission path. (b) SPST switch when terminated to 50-ohm. (c) SPDT switch implementation.

$$s = \left[\frac{-y \pm \sqrt{k}}{2}\right], \; k = y^2 - 4z. \quad (7)$$

The values of k are chosen carefully to avoid excess overshoot and optimal switching times. When $k > 0$ the circuit is overdamped, when $k < 0$ it is underdamped, and when $k = 0$ the circuit is critically damped. $L_B = 581\ nH$ provides an impedance of 598 Ω to 1.7 kΩ over the frequency band (170–470 MHz) to isolate the driver from the PIN diode switch. C_B is chosen accordingly to achieve closer to the critically damped condition and lower diode current settling times.

III. SWITCH DESIGN

A. SINGLE-POLE SINGLE-THROW (SPST) SWITCH DESIGN

Before realizing an SPDT switch configuration, a single-pole single-throw (SPST) switch shown in Fig. 5(a) and (b) is designed and optimized as a baseline for the absorptive switch mechanism. The RF signal is excited at Port 1 and then observed at Port 2. Appropriate DC blocking capacitors and RF chokes are used to obtain good transfer characteristics. Here, L_1=L_2=L_3=561 nH and C_3=C_5=100 pF form a low-pass filter to eliminate high-frequency signals. The circuit is further

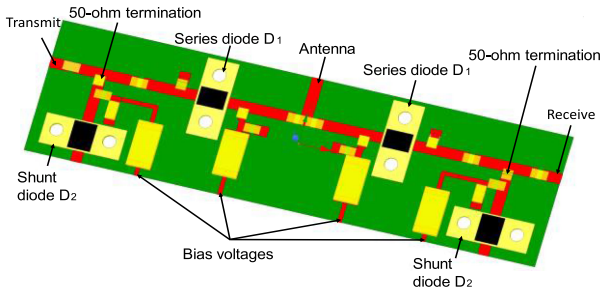
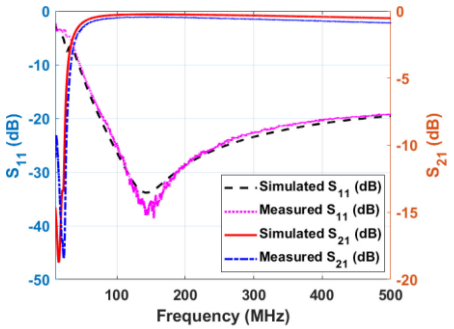


FIGURE 6. 3-D model of the switch.

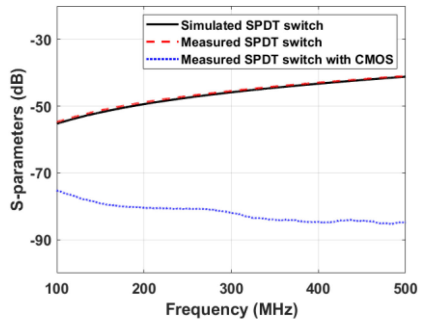
explained using two test cases. Case I: A positive bias is applied at V_2 (15 V) and a negative bias at V_1 (-50 V). This forward-biases the diode D_2, and creates a low-impedance signal path for transmission as illustrated in Fig. 5(a). Case II: A negative bias applied at V_2 (-50 V) with a positive bias at V_1 (15 V). This causes the diode D_2 to be reverse-biased, blocking the RF signal from reaching Port 2. Therefore, a return path is created for the signal which is match-terminated to the ground through the load R_1 as shown in Fig. 5(b).

B. SINGLE-POLE DOUBLE-THROW (SPDT) SWITCH DESIGN

The block diagram of the SPDT switch with the transmitter and the receiver section of the radar system is shown in Fig. 5(c). The bias voltages V_x and V_y are complementary. When V_x is negative, and V_y is positive, the RF signal propagates from the transmit port (T) to the antenna port (A). When V_x is positive and V_y is negative, the back-scattered or reflected signal from a target or the ice surface enters the antenna port and is routed to the receive port (R). The PA output is connected to transmit port, and the receive port is connected to the input of the receiver section. An off-the-shelf limiter is used to minimize the measured video leakage of 3 V_p connected to the receive port of the T/R switch. An external CMOS switch is also used for enhancing the isolation between the transmit port and receiver port of the radar. The COTS CMOS switch is operated to provide high isolation (OFF) during transmission (T-A) and low loss (ON) during the reception (A-R). In transmission mode, the receive port is terminated in a 50 Ω load, reducing spurious signals being coupled into the receiver. The output stage of the PA is terminated in a 50 Ω matched load during receiving mode, and in this period, the PA does not transmit. Any noise or spurious signals from the power amplifier are terminated in a 50 Ω resistor when the PA is not transmitting. The switch is optimized, and co-simulated in Ansys HFSS; and the 3-D model is shown in Fig. 6. The switch is fabricated on an FR4 substrate. The through-hole PIN diodes are mounted on an elevated cavity that also serves as a heat sink. The EM simulated switch results in an Insertion loss (IL) $\leq$ 0.4 dB, a return loss (RL) $\geq$ 19 dB, and the fabricated switch has an IL $\leq$ 0.8, RL $\geq$ 19 dB, and an isolation (I) $\geq$ 37 dB in the frequency band, as shown in Fig. 7(a) and (b).



(a)



(b)

FIGURE 7. (a) Transmission, reflection coefficient simulated versus measured. (b) Isolation comparison of measured versus simulated and with the CMOS switch.

TABLE 2. MOSFET Parameters

MOSFET PARAMETERS		
Parameters	N-channel	P-channel
V_D (max)	100 V	-100 V
I_D (max)	±4.5 A	±4.5 A
V_G (max)	±20 V	±20 V
Q_G	15 nC	26.2 nC
C_{GD}	23 pF	28 pF
C_{GS}	577 pF	1402 pF
C_{DS}	16 pF	13 pF

IV. PIN DIODE DRIVER DESIGN

A. FET MODEL

Careful implementation of the PIN diode driver circuit is critical for enhancing the diode switching performance [22]–[24]. Parasitics of the gate driver, switching type, slew rate, and isolation are considered to maximize the gate driver performance. The FET selected has device parameters described in Table II under optimal conditions.

A low-side driver topology in conjunction with a push-pull FET configuration is implemented. The ON time (t_{on}) of the FET is

$$t_{on} = \frac{C_{eq} V_{gsmax}}{I_g} \tag{8}$$

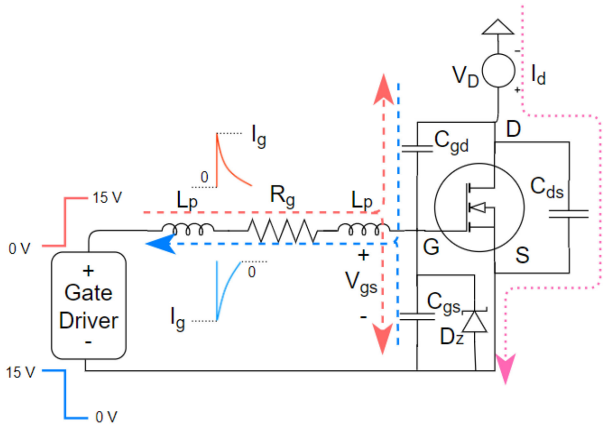


FIGURE 8. Interfacing NMOS with the gate driver.

TABLE 3. PIN Diode Driver State

state	T_{p3}	T_{n3}	PMOS	NMOS	Diode (D_Z)
1	High	High	off	on	Reverse bias
2	High	Low	N/A		
3	Low	High	N/A		
4	Low	Low	on	off	Forward bias

where C_{eq} is

$$C_{eq} = \frac{Q_{tot}}{V_{gsmax}} .$$

C_{eq} is the equivalent charge due to the junction capacitances, and I_g is the gate current generated by the driver supplied to the gate of the FET. The maximum gate to source voltage (V_{gsmax}) is provided by the manufacturer. Charge (Q_{tot}) is proportional to the gate voltage applied. A gate-driver for the FET is shown in Fig. 8. The drain of the NMOS FET is biased at V_D. The driver level shifts the input voltage and toggles the gate from 0 V to 15 V to turn on the FET and then 15 V to 0 V to turn it off. A 15 V Zener diode is placed parallel with V_{gs} to ensure this voltage limitation. An appropriate gate resistor (R_g) is used to reduce the effect of parasitic inductances (L_p) for stable operation and limit I_g. Higher R_g reduces the switching speed and reduces oscillations at the gate of the FET.

B. DRIVER IMPLEMENTATION

The complexity of the driver is reduced by using discrete components, an off the shelf FET gate driver, and a power MOSFET. Several other gate driver topologies [25]–[26] are reported in the literature for power switching applications. However, the simplicity of these designs is also applicable for the PIN diode switching application. The PIN diode driver includes control logic, a dead time circuit, and a push-pull FET configuration. Fig. 9(a) shows the block diagram of different driver stages. The control logic consists of an inverting

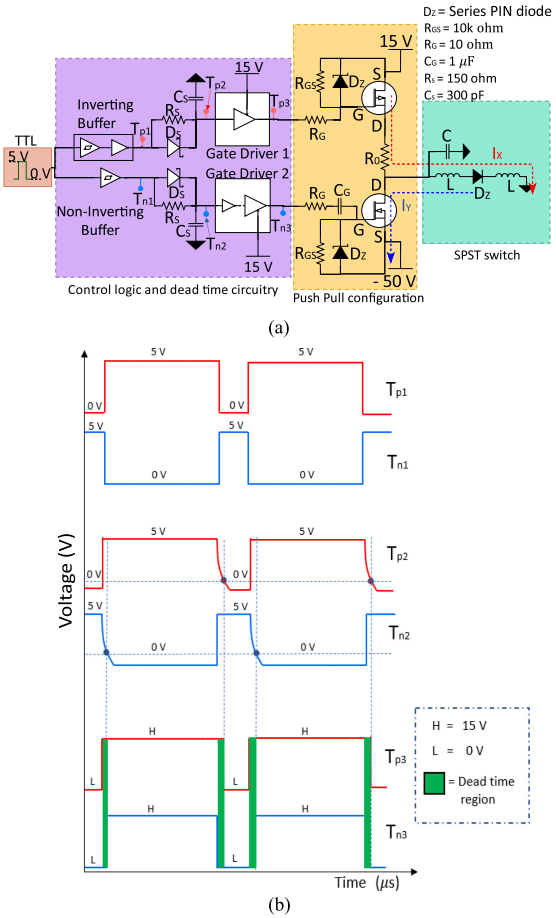


FIGURE 9. (a) PIN diode driver schematic consisting of control logic, dead time circuitry and a low side push pull configuration. (b) Timing waveforms of interfacing the gate driver to the gate of the complementary FETs.

and a non-inverting buffer driven by a transistor-transistor logic (TTL) signal. The radar generates a frequency modulated (FM) linear chirp from 170 MHz to 470 MHz operating at 1% to 10% δ for a fixed period of 100 μs. The TTL logic generated by the digital system is synchronized with the radar waveform. As shown in Fig. 9(b), an inverting and a non-inverting buffer are driven by the TLL logic signal. The output of the buffers are T_{p1} and T_{n1}. The rising edge of T_{p1} and T_{n1} transitions to 5 V as the current flows through a low impedance high-speed Schottky diode (D_s) path. However, the trailing edge discharges through a high impedance resistive path (R_s) and shunt capacitance (C_s), causing the trailing voltage waveform to decay slowly, as shown by T_{p2} and T_{n2} in Fig. 9(b). The roll-off rate at the trailing edge depends on the time constant (C_sR_s). C_s (300 pF) *and* R_s (150-ohm) are selected to get a dead time of 100 ns. With its internal Schmitt trigger logic, the gate driver uses the hysteresis phenomena to set the voltage limit and generates a delay profile at the trailing edge for creating a deadtime region. The non-inverting input gate driver senses T_{p2} trailing edge and sets voltage above 1 V to 15 V (shown by T_{p3}), which is also the maximum supply rail driver voltage. Similarly, the inverting gate driver senses

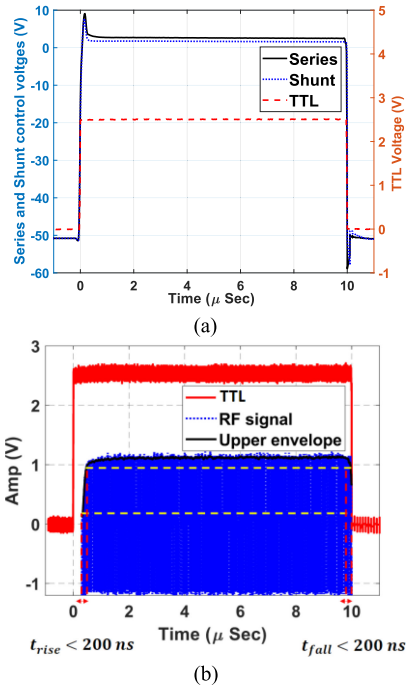


FIGURE 10. **Measurements. (a) Transient switching waveform of the series, shunt PIN diodes. (b) Rise time (t_{rise} < 200 ns) and fall time (t_{fall} < 200 ns).**

the falling edge of T_{n2} and sets voltage greater than 1 V to 15 V, followed by an inversion represented by T_{n3}.

The number of components in the inverting and non-inverting path is kept small to minimize the propagation delay and achieve symmetric dead time zones. The dead time circuitry also generates a propagation delay of 100 ns. A low-side push-pull configuration that consists of complementary FETs is used. The source of the PMOS device is fixed to a 15 V supply rail, and the NMOS source to a −50 V supply rail. The FETs operate in conduction mode when $|V_{gs}|$ is 15 V. The gate of the PMOS is directly coupled to R_g, whereas NMOS is AC coupled (C_g). The coupling capacitance is calculated using

$$C_g = \frac{Q_G}{\Delta V_C} + \frac{15 \times (1-\delta) \times \delta}{\Delta V_C \times R_{GS} \times f} \tag{9}$$

where ΔV_C is the maximum tolerable AC ripple across the capacitor which was assumed to be very small. R_{GS} is set to 10 kΩ and f at 10 kHz. C_g was approximated to 1 μF. The capacitively coupled node varies from −50 V to −35 V periodically and toggles V_{gs} from 0 to 15 V and vice versa.

Table III describes the operation of the driver circuit. Dead-time circuitry avoids cross conduction currents when transitioning from state 1 to state 4 and vice-versa. The green region in Fig. 9(b) shows a dead time of 100 ns. State 4 of the PIN diode is in forward-bias, and the current in the diode is limited by resistance (R_0 = 75 ohm). An SPDT switch requires dual PIN diode drivers with complementary TTL pairs fed at the input. The driver is designed on a four-layer FR4 substrate for noise immunity. The transient switching response of the driver is measured with the SPDT switch as

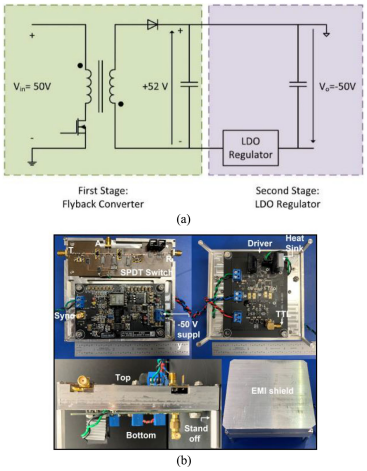


FIGURE 11. **(a) Power convertor supply design. (b) Enclosure for the switch with EMI shielding.**

plotted in Fig. 10(a) for the series and shunt diodes at 100 mA bias currents. On and off time is less than 300 ns including the driver propagation delay which is 150 ns. The measured rise time (t_{rise}) and fall time (t_{fall}) of less than 200 ns is achieved for the PIN diode switch, as shown in Fig. 10(b).

C. POWER SUPPLY AND ENCLOSURE DESIGN

A −50 V DC-DC power supply was developed to support the special requirements of operating the switch. It is designed to provide continuous output power up to 10 W at −50 V from an input dc rail of 24 V to 50 V. The primary goal for this design is to achieve very low output voltage ripple and EMI performance suitable for the radar applications shown in Fig. 11(a). The first stage consists of a flyback DC-DC converter with a switching frequency of 500 kHz. The galvanic isolation provided by this stage reduces any common-mode noise that otherwise would propagate through this power rail into the sensitive radar circuitry.

The second stage consists of a low drop-out (LDO) linear regulator (part number LT3091IFE#PBF) designed to suppress the switching voltage ripple generated by the first stage. As a result, the power supply's output voltage ripple is less than 20 mV at the switching frequency of 500 kHz with an input voltage of 50 V. This design also features a 4-layer PCB stack-up to minimize noise generated by the switching action of the first stage. The layout of the PCB is designed according to best practices for reducing conducted and radiated emissions. First, internal PCB layers are assigned for routing sensitive signals. Second, the high di/dt power loop is routed with wide copper regions and minimal loop area. Third, the void regions on all PCB layers are flooded with ground planes, and these layers are stitched together around the board's periphery to enclose the internal traces in a Faraday cage. This measure significantly reduces the radiated EMI that could otherwise propagate to the nearby radar circuitry. Separate 15V and 5V power rails are also needed to support operation of the switch in this system. A custom two-stage design derives these rails

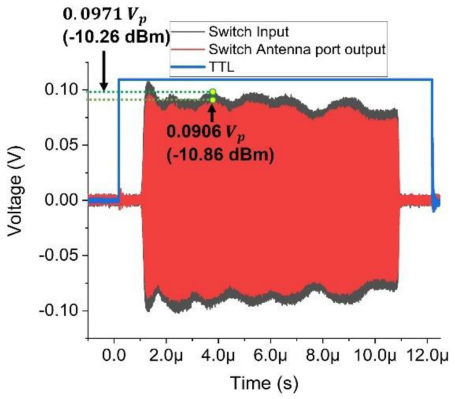
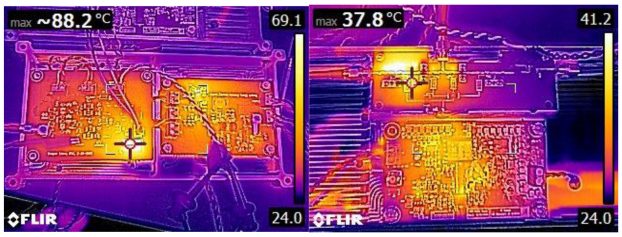


FIGURE 12. High power tests with the SPDT switch module.



(a) (b)

FIGURE 13. Thermals. (a) Driver, 15 V and 5 V power supply. (b) PIN diode switch and −50 V supply module.

from the main DC power bus. The first stage consists of a synchronous buck converter, which is implemented using a monolith controller IC with an integrated switch (part number LT8620). This stage provides an intermediate regulator voltage at 18 V. The second stage consists of a pair of LDO regulators (part number LT3045) which produce the final 5 V and 15 V rails. An enclosure is designed using the Solid works CAD software and milled from a lightweight alloy using the CNC machine, as shown in Fig. 11(b). The dimensions of the box are roughly *12.7 cm* × *12.7 cm* × *5.05 cm.*

V. HIGH POWER TESTS

High power tests are conducted in a controlled lab environment to evaluate the performance of the PIN diode switch. The transmitter port of the SPDT switch is connected to a 200 W (53 dBm) chirped pulse. The receiver port is connected to a 30-dB attenuator terminated in 50 Ohms. The antenna port of the switch is connected to the oscilloscope through a 62-dB attenuator. Fig. 12 shows the measured waveform on the scope when a chirp in black is applied at the transmitter port and measured at the antenna port indicated in red for the SPDT switch. The insertion loss is 0.6 dB which is calculated by considering the difference in power levels from the measurement. Temperature measurements of the PIN diode driver, switch, and power supplies are done to validate its performance at room temperature, as shown in Fig. 13(a) and (b). Since two complementary pairs of PIN diode drivers are used for controlling four PIN diodes in the current SPDT topology, the power dissipation of the complementary FETs in the driver circuitry with the current limiting resistors (R_0) are dependent on the duty cycle (δ). Low cross conduction currents due to the deadtime circuitry and low ON-resistances of the complementary FET ensure low dissipation. The maximum power dissipation for the FET is less than 15 mW at 10% δ. The current limiting resistors dissipate maximum power of 2.7 W at 90% δ during the receive mode (antenna to receiver) and 0.3 W at 10% δ during the transmit mode (transmit to antenna). The overall temperature of the switch module and power supplies stays below 45° C. A few parts, such as the current limiting resistor carrying bias currents, can go more than 50° C and are padded with a heat sink. The temperature measurements indicates that the switch can be operated safely for extended periods.

VI. INTEGRATION OF THE SWITCH WITH THE UWB RADAR

The previous sections discussed standalone SPDT switch design and its performance aspects. A single-channel module of the radar is implemented to verify the UWB chirped-pulse radar's performace with the SPDT switch. The UWB radar consists of 8 identical transmit and receive modules to sound and image about 5-km thick ice. Fig. 14 shows the detailed architecture of the single-channel module of the radar. It consists of a transmitter (52-53 dBm peak transmitting power), an SPDT switch, and a receiver. The switch driver board and custom-built DC power supplies are mounted on the backside of the metal plate. The metallic enclosure separates RF and power supply sections to reduce RFI. Fig. 14 shows the RF section without the enclosure to show various radar parts. Fig. 15 shows the block diagram for evaluating the performance of the integrated module with the T/R switch. We used a 7.5 km optical delay line and attenuators to simulate 3.75 km thick lossy ice. The loop sensitivity of the radar excluding antenna gain for a single channel is defined as

$$S = P_T + G_{PC} + G_{CI} - N \tag{10}$$

where P_T is total transmit power, G_{PC} is pulse compression gain, G_{CI} is coherent integration gain and N is thermal noise power. The system parameters of the radar are given in Table IV. The theoretical loop sensitivity based on the system parameter is 191.37 dB. Fig. 16 shows the single-channel radar measured impulse response. We applied the Tukey window to the transmit signal to reduce Fresnel lobes and a Hanning window to the reference signal used to reduce range sidelobes that result from pulse compression of the received signal [27]–[28]. The measured range resolution is 51.72 cm and matches the ideal response for a radar with 300 MHz bandwidth. The increased range sidelobes on either side of the mainlobe are caused by amplitude ripples of the transmit chirp signal shown in Fig 12. These ripples are caused by power amplifiers and can be eliminated or reduced by pre-distorting the chirp signal. However, we have not pre-distorted the chirp for measurements reported in this paper. Our primary focus is to show that the integrated system with the T/R switch has

FIGURE 14. Single channel module of the UWB Radar.

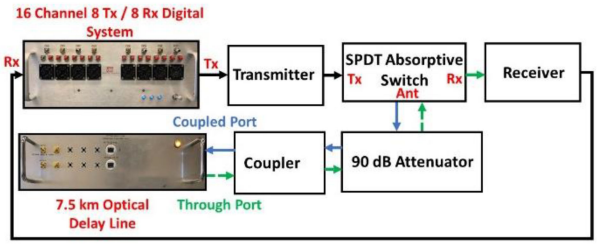


FIGURE 15. Optical delay line loop back test of the UWB Radar.

TABLE 4. Radar System Parameters

Parameter	Value	Unit
P_T, Transmit Power	52	dBm
Bandwidth (BW)	300	MHz
Pulse duration (T)	10	us
G_{PC}, Pulse Compression Gain (k*BW*T)	30.17	dB
G_{CI}, Coherent Integration Gain	24	dB
N noise power (kTB)	-85.2	dBm

k = multiplying factor for hanning window.

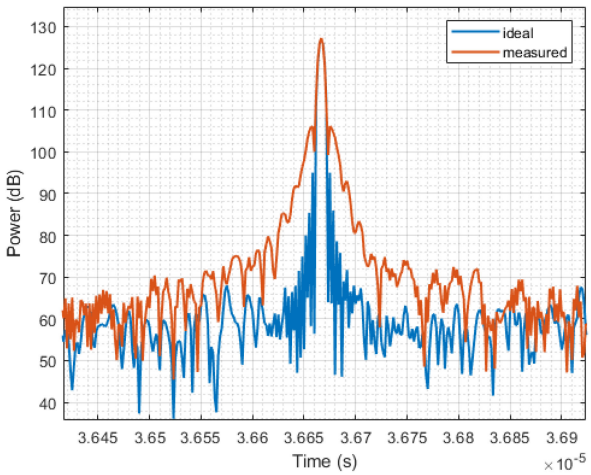


FIGURE 16. Pulse compressed received signal of the loopback test.

adequate sensitivity to sound and image about 5-km thick ice. The measurement is carried out with 122.6 dB attenuation. The signal-to-noise ratio (SNR) observed from the A-scope is 67.6 dB. Loop sensitivity from the measeured data can be obtained as

$$S = SNR + Attunation\ in\ loop$$

Hence, the loop sensitivity obtained from the measured result is 190.2 dB. The results matched with the theoretical value within 1.5 dB. The low insertion loss of the SPDT switch in receiver mode helps keep the receiver's overall noise figure low. High isolation between transmitter and receiver provided by the switch ensures the proper operation of the low power receiver. The performance aspects of the switch and the driver designed in its current form are compared in the literature described in Table V.

VII. CONCLUSION

The development of a high-power PIN diode absorptive switch for UWB radars is presented above. The design is carried out in several stages, from modeling the PIN diode using SPICE models, to optimizing the diode switching performance, to building a circuit supporting the need for high power. The transmit and receive ports are always terminated with 50 Ω impedance to protect the PA output stage and the receiver. The PIN diode driver circuit is built using a low-side push-pull configuration and a built-in dead time circuitry at the input stage to reduce cross conduction currents without compromising the switching performance. The driver is designed to generate a −50 V reverse-bias voltage and a forward-bias current of 100 mA. Custom-built −50 V, 15 V, and 5 V power supplies are also developed to bias the MOSFET supply rails on the PIN diode driver board. Fast PIN diode switching times and high-power tests at 200 W peak power are also verified. The thermal results also validate the performance of the system. The current switch operates with a peak power of 200 W or 20 W average power with a submicrosecond switching speed with the driver. However, to use it at higher power levels, the bias voltages must be increased based on equation 3. The PIN diode selected can withstand a

TABLE 5. Comparision of the Proposed Switch and Driver Design With the Others Availiable in the Literature

COMPARISION OF THE PROPOSED SWITCH AND DRIVER DESIGN WITH THE OTHERS AVAILIABLE IN THE LITERATURE

Ref. No	Operating frequency (MHz)	Insertion loss in transmit (dB)	Insertion loss in receive (dB)	Peak transmit power (kW)	On/off times (ns)	Min-Isolation (dB)	Max-negative bias voltage (V)	Driver technology	Absorptive/ reflective	Driver Complexity
[8]	100 - 350	< 0.9	< 1.3	1	1300/200	> 85	-12	Bipolar junction transistor	Reflective	Low
[9]	-	-	-	-	2000/400	-	-5	FET and BJT	-	High
[10]	8.2			0.3 – 0.9	900/3800		-125	FET	-	High
[12]	53	0.1	0.7	120	High	83	-28	-	-	High
[14]	150 - 600	< 1.5	< 1.5	1	-/2300	> 40	-40	BJT	Reflective	Low
This work	140 - 500	< 0.8	< 0.8	> 0.2	< 350	> 37 With CMOS > 80	-50	FET	Absorptive	Low

continuous power of 150 W and a peak power based on the RF duty cycle. The diode has a maximum biasing limit of 500 V. The switches will be integrated into a multi-channel (8 transmit/receiver, 8 receive only) UWB radar system and deployed to Antarctica to map the deep internal ice layers of the ice sheets during 2022-2023 and following field seasons.

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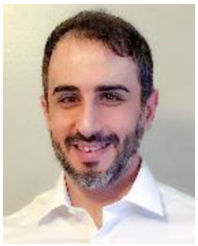
DEEPAK N. ELLURU (Graduate Student Member, IEEE) received the bachelor's degree in electronics and communication engineering from India, and the master's degree in RF and microwave communication from the University of Alabama in Huntsville, Huntsville, AL, USA, in 2018. He is currently working toward the Ph.D. degree in microwave circuits, antenna design, and microwave remote sensing technology.

ABHISHEK K. AWASTHI (Member, IEEE) received the B.Tech. degree in electronics and communication engineering from Ajay Kumar Garg Engineering College Ghaziabad (UPTU Lucknow) Ghaziabad, India, in 2008, the M.Tech. degree in digital communication from the Ambedkar Institute of Technology Delhi (GGSIP University Delhi), New Delhi, India, in 2011, and the Doctoral degree from the Department of Electrical Engineering (RF and Microwave), Indian Institute of Technology Kanpur, Kanpur, India, in 2018. In 2018, he was an Assistant Professor with the Department of Electronics Engineering, Madhav Institute of Technology & Science Gwalior, Gwalior, India. After that, he joined the Electronics and Communication Department, Amity University Jharkhand, Ranchi, India. He is currently an Assistant Research Engineer with the Remote Sensing Center, University of Alabama, Tuscaloosa, AL, USA. His current research interests include the design and analysis of antennas, phased antenna arrays, and ultrawideband radar systems.

S. PRASAD GOGINENI (Life Fellow, IEEE) is currently a Cudworth Professor of engineering with the University of Alabama, Tuscaloosa, AL, USA, and the Director of Remote Sensing Center. From 2005 to 2016, he was the founding Director of the NSF Science and Technology Center for Remote Sensing of Ice Sheets (CReSIS), University of Kansas, Lawrence, KS, USA. From 1997 to 1999, he was the Manager of NASA's Polar Program. He has been involved with radar sounding and imaging of ice sheets for approximately 35 years and contributed to the first successful demonstration of SAR imaging of an ice bed through ice more than 3 km thick. He also led the development of ultrawideband radars for measuring the thickness of snow over sea ice and the mapping of internal layers in polar firm and ice. He and his students developed early versions of radars being flown now as a part of the NASA OIB mission. Dr. Gogineni was the recipient of the Louise Byrd Graduate Educator Award at the University of Kansas and was a Fulbright Senior Scholar at the University of Tasmania in 2002.

DREW TAYLOR (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the University of Alabama, Tuscaloosa, AL, USA, in 2008 and 2011, respectively, and the Ph.D. degree in electrical and computer engineering from Mississippi State University, Mississippi State, MS, USA, in 2018. He is currently an Assistant Professor of electrical and computer engineering with the Remote Sensing Center, University of Alabama. His research interests include digital and embedded systems, radar signal processing, and remote sensing of the earth.



ALI SHAHABI received the Ph.D. degree in electrical engineering from the University of Alabama, Tuscaloosa, AL, USA, in 2020. He is currently holding a postdoc research position with the Electrical and Computer Engineering Department, University of Alabama. His current research interests include the design of power electronics converters, modeling of wide- bandgap power semiconductors and modules, and drive of electric motors.

ANDREW N. LEMMON (Senior Member, IEEE) received the B.S. degree in electrical engineering from Christian Brothers University, Memphis, TN, USA, in 2000, the M.S. degree in electrical and computer engineering from The University of Memphis, Memphis, TN, USA, in 2009, and the Ph.D. degree in electrical engineering from Mississippi State University, Starkville, MS, USA, in 2013. From 2000 to 2010, he was an Embedded Systems Design Engineer with FedEx Corporation, Memphis, TN, USA. From 2010 to 2013, he was a Graduate Research Assistant with the Center for Advanced Vehicular Systems (CAVS), Mississippi State University. He is currently an Associate Professor with the University of Alabama, Tuscaloosa, AL, USA. His research interests include design of power electronics applications for wide band-gap devices, Simulation and modeling of power semiconductor devices and applications, and advanced control strategies for power electronics.

CHANGHYUN CHUNG received the B.S. degree in mechanical engineering from Sungkyunkwan University, Suwon, South Korea, in 2004, the M.S. degree in intelligent robotics from the University of Science and Technology, Daejeon, South Korea, in 2010, and the Ph.D. degree in mechanical and environmental informatics from the Tokyo Institute of Technology, Tokyo, Japan, in 2013. From 2004 to 2008, he was a Senior Research Engineer with Samsung Electronics, Suwon, South Korea. From 2013 to 2017, he was a Principal Research Engineer with Hanwha Techwin, Seongnam, South Korea. He is currently a Senior Research Specialist with the Office of Technology development and Service of Korea Polar Research Institute, Incheon, South Korea.

JOOHAN LEE received the B.S. degree in geology from Kongju National University, Gongju, South Korea, in 1999, and the M.S. degree in geophysics from Seoul National University, Seoul, South Korea, in 2001, and the Ph.D. degree in polar science from the University of Science and Technology, Daejeon, South Korea, in 2008. He is currently the Principal Research Scientist and Director of the Department of Future Technology Convergence, Korea Polar Research Institute, Incheon, South Korea. His research interests include mapping of internal layers and subglacial topography of Antarctic ice sheet using radar and its signal processing.