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Recent Developments in Integrated Interferer-Tolerant Receivers for Reconfigurable Radios

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ABSTRACT Fragmented spectrum allocations at RF and mm-Wave, increased use of carrier aggregation/MIMO and dense spectrum-reuse in wireless links has led to interest in the design of integrated wideband, high-linearity MIMO RX that provide low noise, blocker tolerance and reconfigurability across signal domains. In this paper, receive architectures for wide operating range and blocker tolerance are presented with a focus on recent developments in reconfigurable N-path receivers. Generalized sequence-mixing architectures that support reconfigurable frequency/spatial/code-domain rejection and filtering are described along with directions of research extending operation to wider bandwidths and higher frequencies.

INDEX TERMS N-path filters, reconfigurable receivers, current-mode, passive mixers, sequence mixers, spatio spectral filtering, walsh function sequence based notch filters, blocker tolerant receivers, blocker tolerant MIMO, interference tolerant receivers .

I. INTRODUCTION

Heterogenous networks (Hetnets) that embed small-cells into multi-user(MU) MIMO macrocells (Fig. 1) can achieve order-of-magnitude improvements in overall capacity by increasing spatial frequency-reuse and energy efficiency [1]–[4]. The extensive use of MIMO pico and femtocells is expected to drive capacity gains for wireless networks in the next decade [1], [3], [5]. However, practical deployment constraints and cells that limit access to users lead to increased interference.

Such moves towards extreme densification and increased spectrum reuse are driven by spectrum scarcity. The potential for opportunistic spectrum access in cognitive radios to overcome spectrum scarcity has been recognized for more than two decades [6], [7].

Changing the mindset from conservative license-based policies, designed to protect primary-users from harmful interference, to open, opportunistic spectrum access requires flexible receivers with blocker tolerance. Receiver (RX) sensitivity required to overcome the "SNR Wall" has proven challenging, particular when combined with interferer tolerance [8] required to support spectrum co-existence. Therefore, standards bodies have adopted a more limited, centralized approach through the use of carrier aggregation in cellular [9], channel bonding in IEEE 802.11ac WiFi or geolocation-based databases. However, the rapid increase in global mobile data and internet-of-things applications, when combined with near theoretical spectral efficiency [3], demands further improvements in utilization efficiency.

Interestingly, this concept of under-utilization can be expanded to the *signal electrospace* or transmission hyperspace, including *frequency, time, space and code-domains* [10] (Fig. 2). In such flexible electro-space radios, wide spatio-spectral/code-domain sensing precludes the use of RF filters; however, the absence of front-end filtering makes the RX susceptible to interferers. For example, -100 dBm desired sensitivity with -25 dBm blockers requires at least 75 dB of ADC dynamic range, leading to impractical power consumption for wideband applications. On the other hand, reconfigurable passive frontend filtering to reject interferers results in higher insertion loss, leading to poorer sensitivity.

In the following sections, recent approaches to achieve linear, reconfigurable receivers are summarized. The focus of this paper is restricted primarily to architectures/receivers implemented in silicon technologies, targeting mass consumer

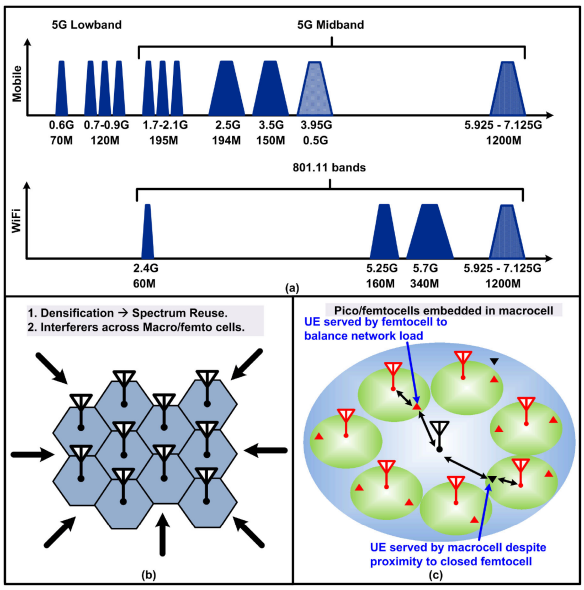

FIGURE 1. **(a) Fragmented 5G spectrum allocations motivate aggressive carrier aggregation to increase data rates. (b) Extremely dense spectrum reuse leads to improved spectrum utilization and network capacity, while (c) increases challenges due to higher number of interfering signals from interfering macro/pico/femto-cells.**

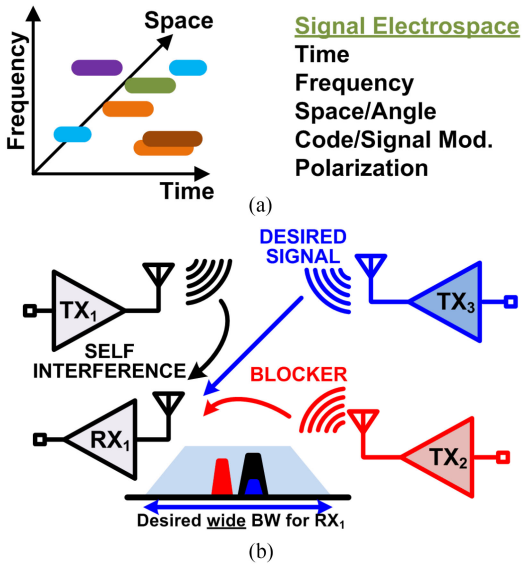

FIGURE 2. **(a) Entire signal *electrospace* can be utilized to improve *full* spectral efficiency. (b) Absence of front-end filtering implies RX must accommodate self-interference as well as blockers from other sources.**

applications such as cellular, WiFi and *Internet-of-Things* (IoT). While techniques discussed have broad applicability, they have been motivated by the desire to leverage the capabilities of scaled integrated CMOS (switches with <200-fs $R_{ON}C_{OFF}$ time constants, incremental near-zero cost of transistors, well-matched capacitors) and mitigate its challenges (poor linearity for large voltage swings, poor 1/f noise, limited high-Q inductors, area limitations that constrain capacitor sizes). This paper also focuses on promising N-path and related mixer-first approaches which provide LO-defined reconfigurable frequency/spatial/code-domain filtering and impedance translation in receivers. Section II describes linear wideband RX implementations using current-mode architectures. Reconfigurable N-path mixer based RX are discussed in Section III. Architecture that extend N-path RX to generalized sequences are summarized in Section IV. Recent efforts to extend reconfigurable filtering to higher frequencies are presented in Section V. Such receivers represent efforts towards achieving the holy-grail of software-defined receivers, with rapid reconfigurability enabling higher spectrum utilization.

II. WIDEBAND INTERFERER-TOLERANT RECEIVERS WITH CURRENT-MODE ARCHITECTURES

Receiver linearity must be sufficient to accommodate intermodulation due to out-of-band interferers. Surface-Acoustic Wave (SAW)-based frontend filtering and duplexers are used to mitigate strong out-of-band interferers as well as TX-RX self-interference in FDD systems as shown in Fig. 3(a). For example, potential self-interference mechanisms in 5G and LTE are reviewed in [11]. Frequency-domain duplexing (FDD) systems require receivers to tolerate a large transmitter (TX) signal leakage through a finite isolation duplexer (Fig. 3(a)). This TX leakage can modulate out-of-band interferers to the band of interest. A scenario for LTE Band 2 as discussed in [12] is shown in Fig. 3(b). The derived IM_3 specification assumes a target OOB-IIP_3 of +5 dBm. As shown in Fig. 3(b), assuming a 50 dB isolation and 2 dB insertion loss in the duplexer, the TX leakage at the input of the RX is -28 dBm. The OOB interferer in this depiction is a continuous-wave (CW) signal at 40 MHz offset with respect to the desired signal frequency (f_{RX}). Notice that the duplexer only provides 4 dB filtering to the CW interferer due to the wideband LTE signal bandwidth [12]. For Band2 the TX signal is at an offset of 80 MHz [12]. The TX leakage, therefore, produces in-band IM_3 products. For the purposes of OOB-IIP_3 calculations, the average TX leakage and CW interferer power over the RX bandwidth is represented using CW tones at 40 and 80 MHz [13]. Achieving 10 dBm blocker 1-dB linearity with >25 dBm IIP_3 in the RX can relax SAW filtering up-front by 20 dB; relaxed filtering specifications and reduced number of SAW filters can also enable tunable passive RF filter deployment in RF frontends.

Supporting 0 dBm input signals (∼316 mV peak signal swing) while providing the low-noise amplification necessary for RX sensitivity is a challenge in scaled CMOS technology with low supply voltages. Over the last decade, current-mode architectures have been extensively used to break the trade-off between low noise amplifier (LNA) gain and linearity [15]–[17] where the RF input signal drives G_M cells that translate the signal to RF currents (Fig. 4(a)). Ensuring low impedance nodes in the RF chain and delaying conversion to voltage domain till the IF enables filtering prior to conversion to voltage and hence improved linearity. The input amplifier in such receiver is a low-noise transconductance amplifier (LNTA) which provides input matching to antenna impedance, R_{ANT} and high output impedance. In the case of

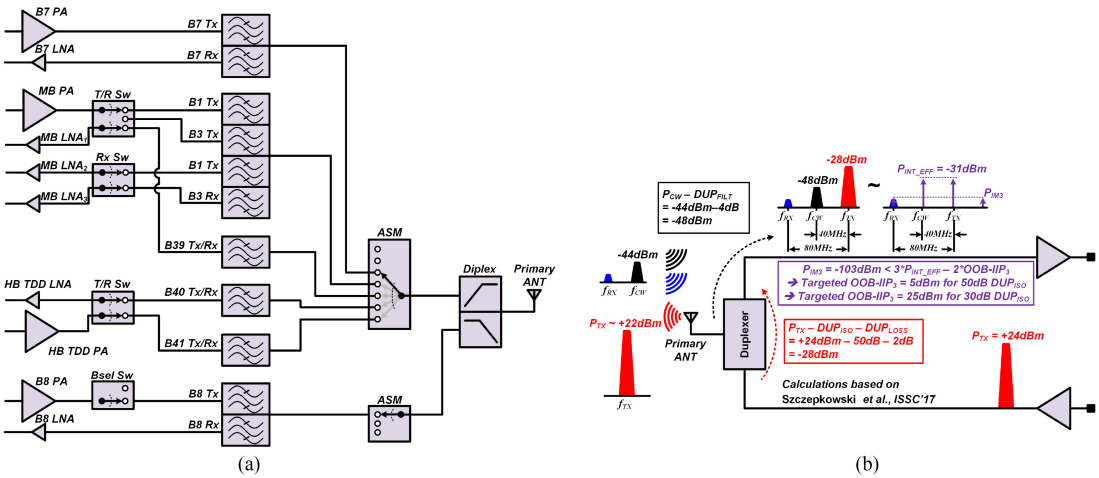

FIGURE 3. (a) An example implementation for LTE RX demonstrates the need for array of filters and duplexers to enable tolerance of TX leakage and strong intererers, while also enabling multi-band operation [14], (b) TX leakage signal results in inter-modulation mechanisms causing receiver desensitization. The annotated numbers are for Band B2 of LTE [12], demonstrating the linearities required for typical LTE operating scenarios.

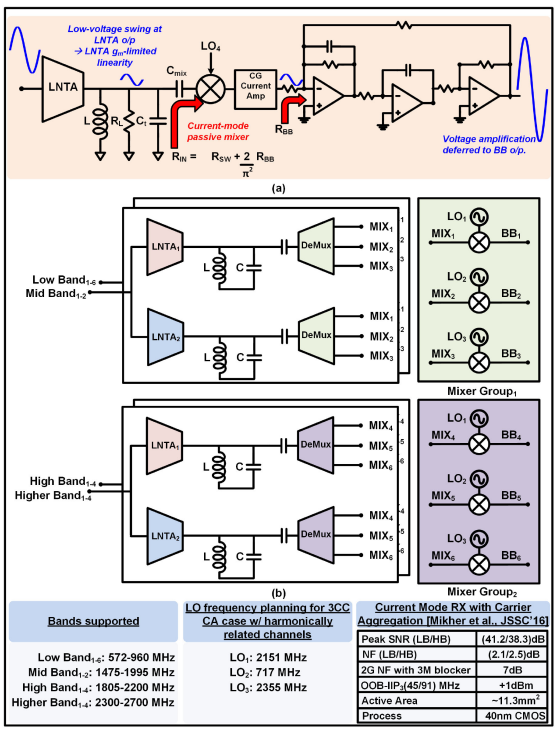

FIGURE 4. (a) Low-noise, wide-band and high-linearity performance is supported with current mode LNA front-end architecture. (b) [24] utilizes multiple current-mode parallel paths to support carrier aggregation.

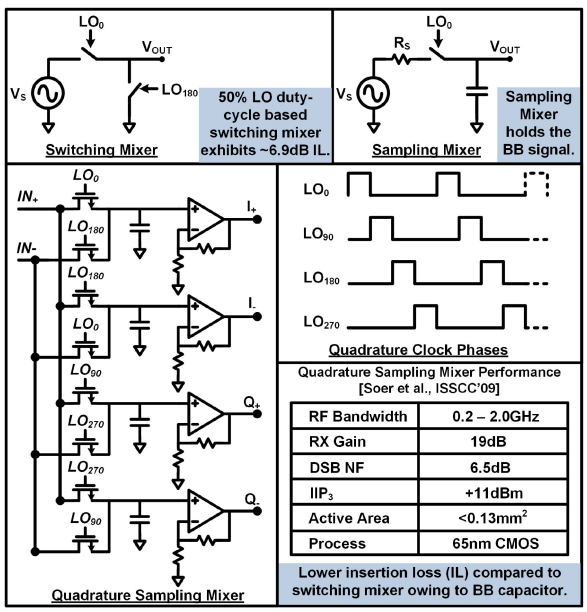

FIGURE 5. Passive mixers driven by non-overlapping clocks (25% duty-cycle in this figure) improve noise, insertion loss and linearity when compared to 50% duty-cycle driven mixers. [26] utilizes a quadrature Sampling Mixer approach to achieve wideband, linear RX with 6.5 dB DSB NF and +11 dBm IIP_3.

RX targeted for wide operating frequency range, wideband matching is achieved using feedback techniques [18] and/or through well-established noise-cancellation techniques building on the initial concept in [19].

The low-noise transconductance amplifier (LNTA) drives multi-phase passive mixers driven by non-overlapping LO pulses. While current-mode passive-mixer design optimization for 50% duty-cycle is detailed in [20], the I and Q mixers are both enabled for a part of the LO cycle. This causes coupling between the I and Q paths, which in turn reads to asymmetric gain around the center frequency and impacts mixer IIP2 and noise figure. I and Q path isolation can be improved by optimizing the coupling capacitor from the LNTA to the mixers [20] or by splitting the LNTA output to two active stages at the cost of RX linearity. On the other hand, the use of non-overlapping LO pulses (Fig. 5) ensures that the I and Q paths are not connected to the LNTA output at the same time, providing isolation between I and Q paths leading to symmetric gain about the center frequency, higher mixer gain (reducing NF impact of subsequent blocks) and improved linearity as detailed in [21].

When coupled with careful frequency planning and separation of RX chain across different bands, the LNTA with passive-mixer architecture has shown to be useful for supporting receivers that operate across a wide frequency-range across all their paths. For example, [22] achieves 4.5 dB NF and 16 dBm out-of-band IIP_3 across 0.4 GHz to 0.9 GHz using such an approach. A lower NF is achieved of 3 dB is achieved in [23] by using the passive-mixer following LNTA to provide high in-band impedance (leading to in-band voltage gain) while providing out-of-band filtering. In a recent implementation [24], the authors present a wideband receiver architecture that supports carrier aggregation (both intra and inter-band) for both 3 G and LTE standards. The architecture uses 16 parallel RF ports driving current mode front-ends with passive mixers, achieving overall +1 dBm (OOB IIP_3) linearity. Fig. 4 shows one such RF path with current-mode LNTA front-end. The passive mixers are driven with LO that is frequency planned to ensure that harmonic reception doesn't impact the receiver sensitivity. Wideband LNTA input matching is achieved through capacitive feedback. Such band-separation approaches to support carrier aggregation and MIMO are also adopted in [25], which features 20 RX paths in 12 nm CMOS, achieves 600M-6 GHz operation and supports 6 inter-band CA. In this case, external LNAs are used to relax NF requirements in integrated RX. In the following, we focus on techniques that aim to simpify multi-band, multi-mode RX design through the use of reconfigurable front-ends, potentially increasing the operating range of each path and thereby reducing the number of required RX paths.

III. RECONFIGURABLE INTERFERER-TOLERANT N-PATH FILTERS AND MIXER-FIRST RECEIVERS

Passive switching-mixers in CMOS driven by rail-to-rail LO can provide higher linearity than LNAs at the input. However, the absence of RF gain leads to poorer RX noise figure. Nevertheless, overall higher dynamic range can be achieved through mixer-first approaches where IIP_3 improvements outweigh NF degradation. While integrated passive mixers can accommodate >0 dBm input, a switching mixer using a 50% duty-cycle LO has been shown to have (Fig. 5) 6.9 dB insertion loss (IL). The impact of LO duty-cycle was investigated in [27] and a quadrature passive-mixing approach with 25% duty-cycle non-overlapping clocks reduced mixer insertion loss to 0.9 dB, leading to overall <6 dB NF at 2.4 GHz with passive LC matching network. The impedance translation property of passive mixers was also observed in [27] where the mixer translates the baseband capacitance impedance to the LO-defined RF frequency, enabling high-Q LO-defined filtering at RF nodes. A mixer-first architecture was subsequently proposed in [26], adopting the quadrature sampling mixer which reduces passive mixer loss as compared to switching mixers (Fig. 5). Wideband 0.2 GHz to 2 GHz operation is achieved using a balanced 180° based input-matching network with ∼6.5 dB NF and IIP_3 of 11 dBm.

Such multi-path architectures where the switches are commuted across filters with time-constants that are much larger than LO period are similar to N-path filters proposed in the 1960s [32]. The potential to realize frequency-translated filters using such approaches that are well-suited to CMOS integration has led to increasing research interest in the last decade.

A mixer-first architecture that leveraged the impedance transparency provided by passive mixers to provide reconfigurable RF input matching and bandpass filtering at RF input was proposed in [28], [33]. In this case, the mixers are driven by non-overlapping clocks (shown in Fig. 6 for $N = 8$ [28]. Each of the N mixer switches are sequentially connected to the RF input, with corresponding capacitors, $C_{L,i}$ storing the average RF when i^{th} switch is enabled (Fig. 6). As derived in [33], the effective RF input impedance can be shown to be,

$$Z_{in} = R_{sw} + \gamma R_B || Z_{sh} \tag{1}$$

$$Z_{sh} = \frac{4\gamma}{1-4\gamma}(R_{sw} + Z_a) \approx 4.3(R_{sw} + Z_a) \tag{2}$$

$$\gamma_{8\,ph} = \frac{2}{\pi^2}(2-\sqrt{2}),\ for\ 8\ phase\ LO \tag{3}$$

where Z_a is the effective antenna impedance and 0.1 GHz–2.4 GHz operating frequency range in 65-nm CMOS with ∼4 dB NF [28].

While RX performance is improved with increase in LO phases, generating non-overlapping pulse (NOP) LO phases becomes challenging at multi-GHz frequencies, limiting RX operating frequency. Overlap between LO phases leads to charge sharing across baseband capacitors since more than one is connected to the RX input at the same time. Notably, finite switch resistance limits out-of-band filtering and the impact of harmonic down-conversion can be significant for low N [28], [34].

Achieving low NF by increasing mixer switch size introduces power and operating frequency trade-offs due to parasitic capacitances. A gain-boosted N-path approach while incorporating reconfigurable N-path filtering is proposed in [29], [35]. As shown in Fig. 7, RF N-path filtering present both at the input and output of the RF G_M-cells provides better out-of-band filtering and supports higher linearity. Gain across the N-path mixer structure is similar to the Miller-effect and enables the use of smaller switches and effectively smaller capacitances for given bandwidth, leading to lower area and power. The current re-use structure in the gain-boosted N-path filter front-end in [36], results in additional (*indirect*) BB amplification that relaxes the BB amplifier noise requirements. Measured over 0.1–1.5 GHz this work achieves an OOB IIP_3 of 13 dBm with NF < 3 dB.

While the mixer first-schemes can provide input-matching and linear operation, higher NF due to the absence of the LNA can be mitigated by using noise cancelling approaches. [30] presents a mixer-first architecture to ensure low noise figure while providing a wideband input match and enhanced linearity. A low noise figure (∼2 dB) is achieved with frequency translated noise cancellation (FTNC) architecture that comprises of a mixer-first front-end providing the input match

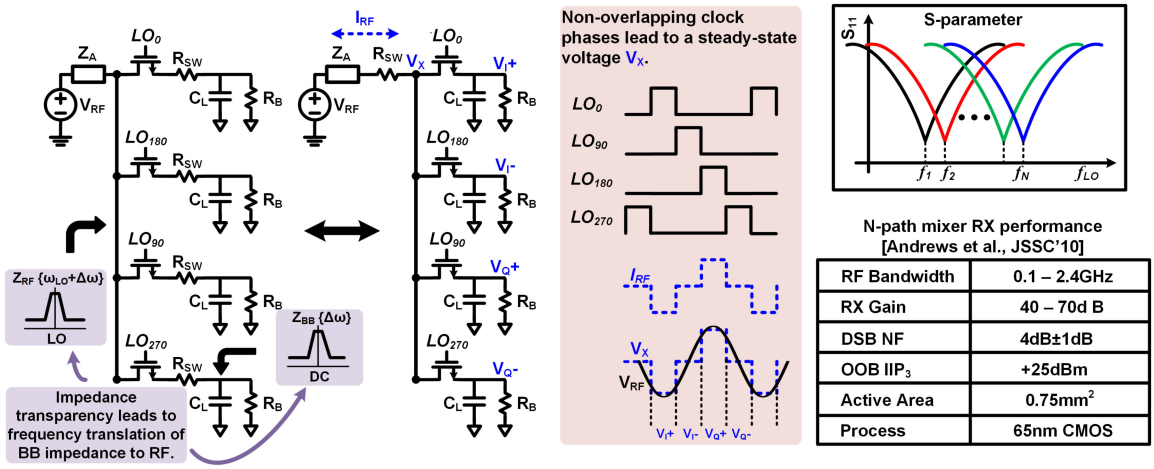

FIGURE 6. N-path mixer-first RX [28] exploits impedance translation from baseband to RF to provide LO-defined filtering and impedance matching, while mixer-first approach leads to 25 dBm IIP_3.

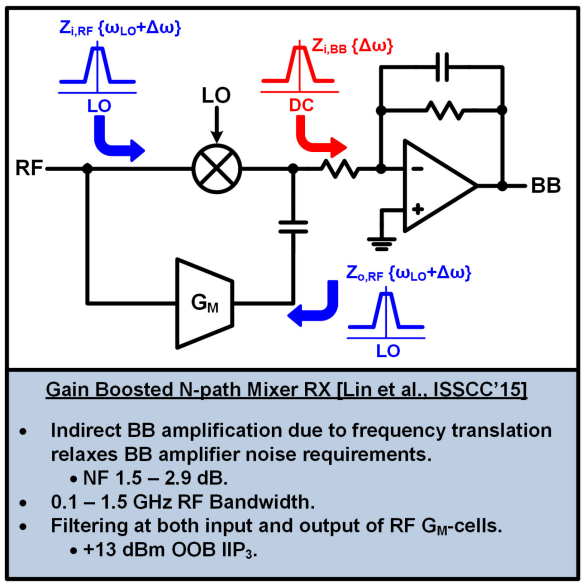

FIGURE 7. Gain-boosted N-path RX architecture enables lower power consumption by enabling smaller switches sizes and lower area by enabling smaller capacitances [29].

through the ON resistance of switches comprising the mixer. Conversion gain of the receiver is 70 dB while measuring +13.5 dBm out-of-band IIP_3. More importantly, the noise canceling architecture with low non-overlapping clock phase noise ensures a nominal degradation of 2.2 dB in NF in the presence of a 0 dBm blocker.

The linearity of such N-path approaches is limited by switch linearity in CMOS technologies. Replacing SAW filters for such receivers require IIP $_3$ of ≈+35 dBm and IIP_2 of ≈+90 dBm. In [31], an N-path bandpass filter is followed by a N-path notch filter using a topology that achieves relatively constant V_{GS} and V_{GD} voltages across the switches while also maintaining a low V_{DS} (Fig. 9). The key challenge in implementing a passive-mixer topology that achieves this is that the switches see IF voltage on its drain/source and RF on the source/drain during mixing operation. In [31], the authors implement N-path bandpass and notch filters by relying on down-conversion through bottom plate capacitors in a differential RF configuration. This allows setting DC voltages on the source and drain nodes of the switches. The differential RF configuration ensures a virtual ground at the drain and source nodes of the shared switch. This arrangement enhances the linearity of the N-path filter switches due to an effect akin to bootstrapping in T/H sampling switches. The implemented architecture reports OOB IIP_3 of about +44 dBm for a blocker at 80 MHz offset from in-band. The reported blocker 1-dB compression at 80 MHz offset OOB blocker is +13 dBm. The RX supports operation from 0.1–2.0 GHz with a noise-figure of 6.3 dBm for operation at LO frequency of 1 GHz. The bottom-plate N-path architecture is further extended in [37] where the bottom plate voltage of the N-path mixer capacitors is connected to NOP-driven switches for readout. A 180°-phase shift in the readout switches leads to a 2x voltage boost equivalent to a passive-voltage boost. The bottom-plate readout scheme in addition to an implementation in 22 nm FDSOI technology and a 2:1 transformer between the mixer and the antenna enables low noise figure with small switch size and consequently low power consumption. The implementation in [37] achieves 5 dB-9 dB NF and 25 dBm OOB IIP_3 from 0.6 GHz to 1.2 GHz operation while consuming only 600 μW power, demonstrating the promise of mixer-first N-path RX for low-power IoT applications.

While this review has focused on the use of N-path approaches in mixer-first receive architectures, the last decade has also seen extensive research in the realization of tunable N-path band-pass and band-stop networks in receive chains for blocker filtering. Excellent reviews of concepts, design challenges and research for wideband RX, N-path filters and mixer-first RX are described in [34], [38]. Interestingly, such networks also display non-reciprocal properties, leading to the demonstration of integrated circulators and isolators that are

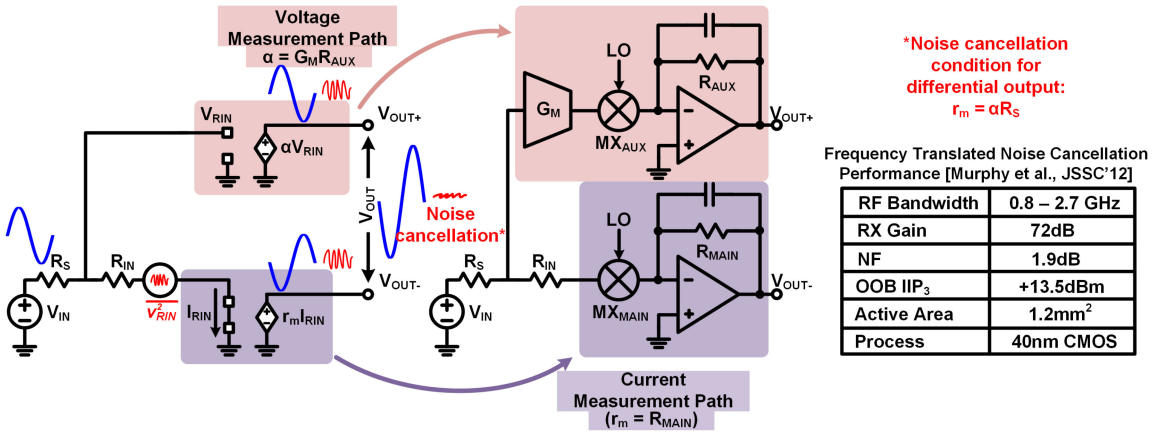

FIGURE 8. Noise canceling architecture in [30] presents an approach to alleviate the challenge of high noise figure associated with mixer-first architectures.

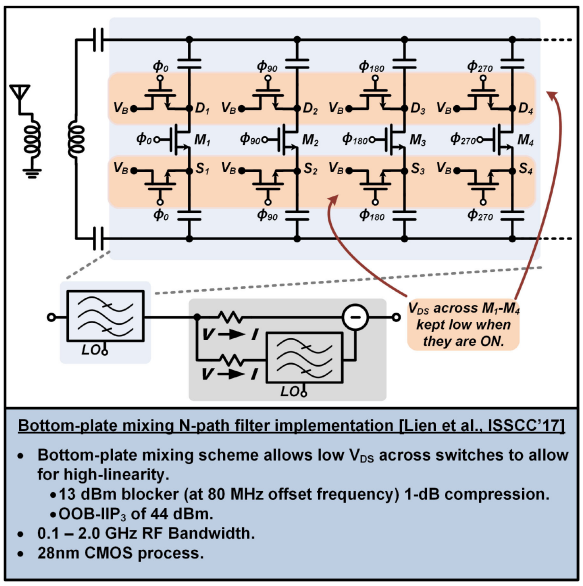

FIGURE 9. Improved linearity in N-path mixer RX through bottom-place N-path techniques is demonstrated in [31]. The approach leads to constant V_{GS} and V_{GD} voltages across the switches while also maintaining a low V_{DS} enabling 44 dBm OOB IIP_3.

tunable with LO frequencies and can be extended to reconfigurable passive networks [39]–[41]. While LO-phase noise is similar to conventional mixers in N-path mixer RX, N-path filters and non-reciprocal circuits must consider reciprocal mixing due to phase noise and it's impact on noise figure. An analysis of phase noise for such architectures is presented in [42]. Additionally, clock path imperfections can lead to noise/signal folding from harmonics and degraded blocker rejection and therefore the clock design must be careful to avoid overlap between LO pulses [43].

Reconfigurable RX have also been demonstrated with passive mixing following by sharp frequency filtering using time-varying components in [44], [45]. The proposed filtering-by-aliasing technique places an integrate-and-dump circuit and a time-varying resistor following the passive mixer to enhance filtering of close-in blockers, demonstrating 17 dBm IIP_3 for blockers at 1.2x BW offset for RF frequencies varied from 0.1 GHz to 1 GHz (assuming variable LO to the passive mixers).

IV. GENERALIZED N-PATH SEQUENCE MIXING

N-path mixer operation in receivers, described in the Section III assume mixers driven by non-overlapping clock pulses as shown in Fig. 6. A mathematical analysis of N-path passive mixers using transient signals is presented in [33] to derive intuitive equivalent LTI networks. A unified analysis of the linear periodically time variant (LPTV) N-path structure in mixing and sampling domains is presented in [46] with a more recent simplified analysis in [47]. The following summarizes a correlator-based analysis described in [48]. This approach presents an intuitive explanation for N-path filter or mixer operation where switches are driven by generalized orthogonal sequences. The mathematical underpinnings of the correlator-based analysis are described in Section IV-A and Walsh-Functions as an orthogonal basis function are summarized in Section IV-B. Receivers that leverage this generalized sequence-driven reconfigurable N-path filters to achieve interferer-filtering in the frequency-domain, spatial-domain and code-domain are described in Section IV-C, Section IV-D and Section IV-E.

A. N-PATH FILTERS AS CORRELATORS

Fig. 10(a,b) presents series and shunt N-path filters respectively, where switches are driven with orthogonal sequences, W_k. Orthogonality across W_k implies,

$$\frac{1}{T_0}\int_0^{T_0} W_i(t)W_j(t)dt = \frac{\delta_{ij}}{N} = \begin{cases} 1/N, & \text{if } i = j \\ 0, & \text{if } i \neq j \end{cases} \quad (4)$$

Assuming $R_A C >> T_0$ (long integration times relative to LO period), the steady-state voltage on the shunt and series capacitors in FIg. 6(a,b) can be shown to be [48], [49],

$$V_{C,j}(t) = \frac{\int_0^t V_{RF}(t)W_j(t)dt}{\int_0^t W_i(t)W_i(t)dt} \quad (5)$$

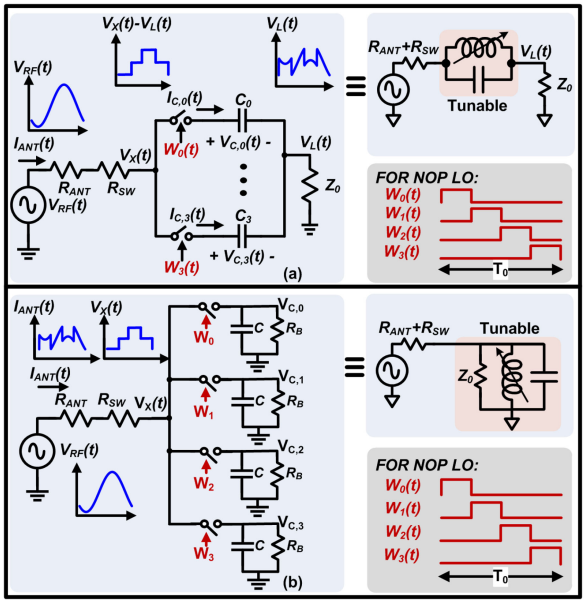

FIGURE 10. Series (Fig 10(a)) and shunt (Fig 10(b)) N-path filter with switches driven by orthogonal sequences; filtering can be generalized from NOP pulses to other orthogonal basis functions in Fig 11.

Therefore, the steady state voltage across the capacitor is a correlation or dot product of the voltages $V_{RF}(t)$ and $W_j(t)dt$. Assuming a single-tone RF input and NOP pulses for W_j, if the RF signal frequency, f_s is not equal to the LO signal or its harmonics, the correlation from (5) is zero. On the other hand, $f_{RF} = mf_{LO}$ leads to a staircase approximation of the input signal. Therefore, at RF frequencies close to the LO, $V_X(t)$ is shown in Fig. 10(a) representing a bandpass response. On the other hand in Fig. 10(b), $V_L(t) = V_X(t) - V_{C,k}(t)$, leading to a bandstop filter. While these results are expected from [33], [46], the correlator-based interpretation suggests that N-path filter operation can be extended to any set of orthogonal sequences, W_k that satisfy (4).

B. ORTHOGONAL BASIS FUNCTIONS:

Orthogonal basis functions that can be used to drive passive mixers are shown in Fig. 11. Non-overlapping pulses, typically used in N-path mixers, represent one such basis function where the lack of overlap between pulses ensuring orthogonality. Walsh functions (WF), similar to Fourier transform, also represent a complete and orthogonal basis set for representing signals [50]. WF, as shown in Fig. 11, are restricted to ± 1, making them compatible with digital implementations. The order of WF-seq can be increased by generating additional sequences with higher number of zero crossings in time period T_0 [50]. Fig. 11 shows a 2^{nd}-order and 3^{rd}-order WF-seq along with 4-phase and 8-phase NOP with same period T_0.

Similar to Fourier series, a periodic signal $x(t)$ can be represented using WF coefficients, c_k, [50] and $WF_k(t)$

$$x(t) = \sum_{k=0}^{\infty} c_k WF_k(t) \tag{6}$$

where $WF_k(t)$ represents k^{th} WF-seq. The WF coefficients are computed by

$$c_k = \int x(t) WF_k(t) dt \tag{7}$$

For the 2^{nd}-order WF, the WF coefficient, c_k, for sinusoidal signal at frequency f_0 and the correlation with the 4-phase NOP is shown in Fig. 11. For a zero-mean sinusoidal signal, correlation with $wal(0)$, $sal(2)$ is zero (Fig. 11 and (7). Therefore, a 2^{nd}-order WF representation of the input sinusoidal signal requires computation of two coefficients. Similarly, a 3^{rd}-order WF representation requires computation of four coefficients related to $sal(1)$, $cal(2)$, $sal(3)$ and $cal(3)$ (Fig. 11). As discussed in [48], the sinusoidal signal representation accuracy increases with increasing order for both NOP (translating to narrower pulses) and Walsh Functions.

C. RECONFIGURABLE SHUNT NOTCH FILTERS FOR INTERFERER-REJECTION

Low-noise blocker filtering at receiver front-end is a critical requirement in FDD communication. For example, LTE standards mandate more than 40 dB rejection of TX leakage to prevent desensitization in diversity receivers with 27 dBm TX output power [52]. This stringent requirement is typically met with SAW filters which provide high-Q band-specific filtering. In a multi-band use case, multiple SAW filters are required with each SAW filter preceded by a single-pole multi-throw switch to cater to multi-band use case [24]. This succession of switches and filters leads to ~3 dB insertion loss up the receiver chain [14]. Hence, for LTE diversity receiver use case, any SAW-less scheme would require roughly 40 dB TX leakage filtering with $\lesssim$ 3 dB noise degradation of the diversity receiver. Recent works on reconfigurable shunt (N-path or otherwise) notch-filters have demonstrated promise of SAW-less operation for such applications [52].

A shunt notch-filter is shown in Fig. 12(a) that provides a shunt low impedance at the LO-defined center frequency while presenting a high impedance at all other frequencies. Such notch/bandstop filters approach enables rejection of specific interferers while enabling reception over a wide frequency range, which is of interest in CA scenarios where desired frequencies may be widely separated. Unlike the bandstop filter in Fig. 10(b) which presents a high impedance at bandstop frequency, the shunt notch filter ensures low signal swing for given interferer power. Inductor-based notch-filter topologies with NOP LO and WF sequences are shown in Fig. 12(a,b). The inductor high-pass response is frequency-translated about the LO frequency, f_0, creating a notch at f_0. Notably, shunt switches are needed to maintain inductor current when N-path switches to RF_{IN} are disabled. Applying WF-seq instead of NOP to the N-path filter in the configuration leads to the same response. Importantly, since either WF_i or $\overline{WF}_i$ is enabled, shunt switches across the inductor are no longer necessary in Fig. 12(c).

The capacitive parasitics associated with an inductor make it challenging to implement the notch filter with a physical

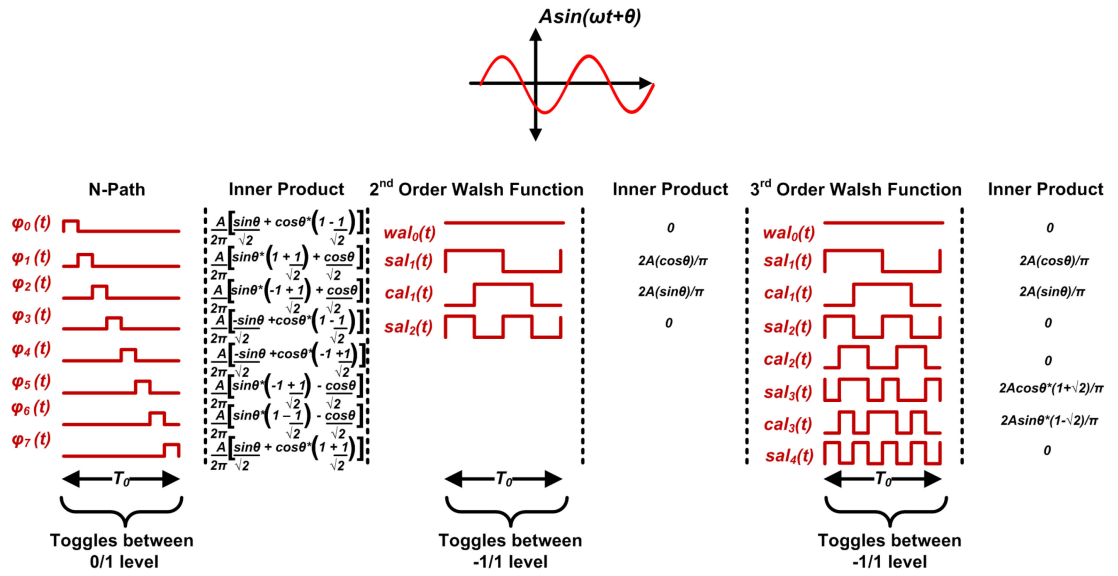

FIGURE 11. Orthogonal basis functions: Non-overlapping LO pulses, 2^{nd}-order Walsh-Functions, 3^{rd}-order Walsh-Functions.

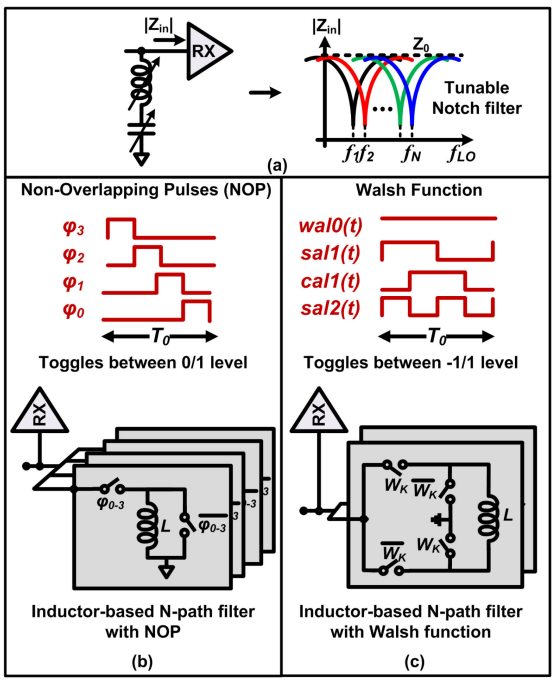

FIGURE 12. (a) Shunt notch filtering is of interest for wideband receivers where specific interferers must be rejected, (b) Notch filter design with non-overlapping LO pulse based N-path filter, (c) Walsh function sequence based N-path filter [48].

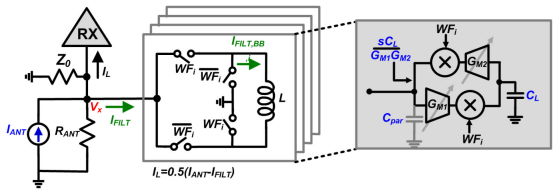

FIGURE 13. Four-correlator bandstop filter where the inductor is implemented using a frequency-translated gyrator. The correlators are driven WF-sequences and can be reconfigured by changing WF-seq from the 3^{rd}-order WF-seq at one frequency to two 2^{nd}-order WF-seq at two frequencies to create a dual-frequency notch filter [48].

inductor. A four-correlator bandstop filter is shown in Fig. 13 where the inductor is emulated with a gyrator [48]. An RF G_M-cell is used in the gyrator to reduce noise/parasitics at RF input. The four-correlator implementation in 65-nm CMOS is shown in Fig. 14. A reconfigurable approach can be adopted where the correlators are driven by an 3^{rd}-order Walsh-Function or two 2^{nd}-order Walsh-Functions. Measured performance is shown in Fig. 14 two independently tunable frequency notches (correlators driven by 2^{nd}-order WF) demonstrating the ability to reject multiple interferers using such N-path structures.The notch filter implementation in 65 nm CMOS achieves 20 dB rejection at one frequency and 14 dB concurrent rejection at two frequencies (limited by number of correlators) and operates across 0.3 GHz to 1.4 GHz with 2.5 dB–3.5 dB NF.

D. RECONFIGURABLE WALSH-FUNCTION BASED SPATIO-SPECTRAL FILTERING FOR INTERFERER-REJECTION IN MIMO ARRAYS

Arrays of N-path mixers sharing baseband capacitors can provide spatio-spectral selectivity where frequency of reception is determined by the LO frequency while angle-of-incidence (AoI) received is determined by relative phase-shifts between NOP driving the N-path mixer elements [53]. Such an approach achieves phased-array operation which is equivalent to a multiple-input single-output system, where only information from specific AoI is preserved. Such an approach cannot support subsequent multi-beamforming. Fig. 15 shows a multiple-input multiple-out (MIMO) receiver, representative of systems operating in emerging 4 G/5G and WiFi links. Similar to the arguments in Section IV-C, it is preferable to

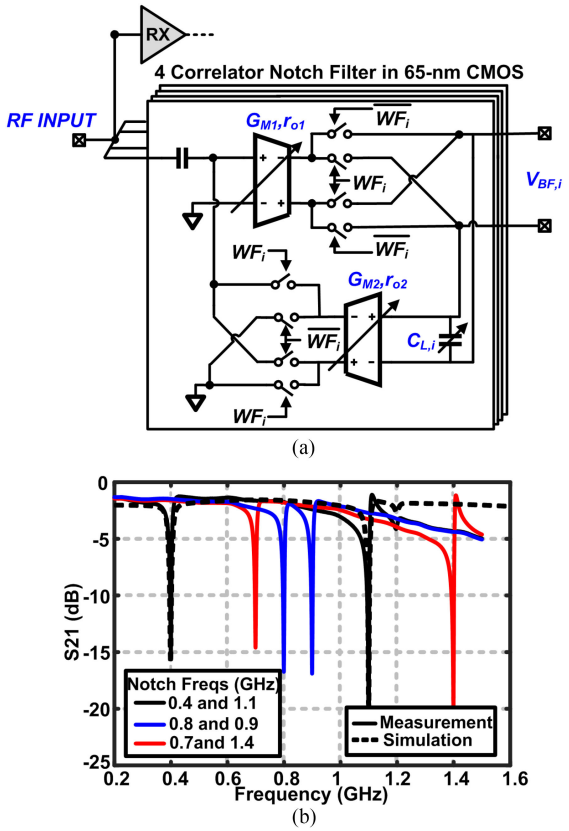

FIGURE 14. (a) Schematic of the four-correlator reconfigurable bandstop filter in [49]. (b) Measured S21 when two 2^{nd}-order WF-seq are applied to the filter leading to stopband at two independent frequencies [49].

have a wide field-of-view as well as wide frequency range with spatio-spectral notch filtering for rejecting specific interferers. Such an approach preserves a wide field-of-view for all elements while rejecting interferers determined by their angle-of-incidence and frequency [54]–[56] and support subsequent multi-beamforming in the digital domain (Fig. 15).

The reconfigurable WF-based shunt frequency filtering in Section IV-C can be extended to arrays by combining the baseband capacitances in the correlators across multiple elements (Fig. 16). Notably, the shunt spatio-spectral notch filters appear in parallel to the input and present a low effective impedance at the antenna for frequencies and AoI defined by the period of the WF-sequences and relative phase between the WF-sequences that are applied. The four correlators in each elements can be driven by 4 3^{rd}-order WF-seq of period T_0. The four correlators can also be configured as two pairs each driven by a 2^{nd}-order sequence with period T_1 and T_2. This enables spatio-spectral notching at each element input at two independent frequencies and AoI as shown in Fig. 16 where notch frequency and AoI are moved to two different combinations [51]. This receive array supports subsequent MIMO beamforming enabling flexible operation from 0.3 GHz to 1.4 GHz (limited by LO generation in 65-nm CMOS) and provides up to 20 dB rejection at two independent AoI/frequencies, while degrading NF by ∼3.2 dB.

The use of N-path RX for MIMO is also demonstrated in [57] to accomplish mutual impedance tuning in a mixer-first MIMO RX. Variable impedance networks are introduced the couple the baseband of different elements in the MIMO RX together and the N-path RX translates the coupling to RF input. The N-path RX network is hence able to compensate for antenna coupling in the MIMO RX, resulted in improved SNR. The implementation in 45 nm RFSOI operates from 0.1 GHz–3 GHz with 3–6 dB NF and is able to demonstrate a 5–7 dB SNR improvement in different MIMO antenna scenarios.

E. RECONFIGURABLE CODE-DOMAIN RECEIVERS USING WF-SEQ MIXING

Sequence-mixing N-path filters can also be used to implement code-domain receivers with code-stop and code-pass properties at RF input. Such an RX was first proposed in [49] with principle of operation summarized in Fig. 17. The desired input is assumed to be RF signal at f_0 modulated with a pseudo-random code, PN_{R1}. Leveraging the analysis in (5), the sequence, W_k applied to the k^{th} mixer in the N-path RX in Fig 17 is,

$$W_k = \varphi_k \cdot PN_{R1} \tag{8}$$

Extending the correlation properties of N-path mixers, the voltages on the capacitors are the despread downconverted desired signal. On the other hand, narrowband interferers are spread due to the code-modulated LO and can be filtered out at baseband. The code-pass RX requires the code in the RX to be synchronized with the RF input signal which can be accomplished using traditional pilot tone based synchronization in code-domain receivers.

A gain-boosted 0.3–1.4 GHz N-path RX implementation in 65-nm CMOS is shown in Fig. 18 that combines code-domain sequence-mixing with the gain-boosted N-path architecture described in Section III. In addition, concurrent reception of two signals is enabled by placing two N-path correlators (labeled Channel 1 and Channel 2) in series in the feedback path. Since the correlators are in series, the same RF current, I_{FB}, flows through both correlators. Capacitor voltages in each channel are the correlation of the RF signal with sequences applied to each channel enabling concurrent reception of two code-modulated signal modulated with separate codes(Fig. 18).

Such code-domain filtering can also be used to achieve self-interference cancellation by exploiting orthogonality between codes used to spread TX signal and RX signals in simultaneous transmit and receive transceivers [49], [58], [59]. Code-stop and Code-pass filters can be combined to enhance TX-RX isolation in the code-domain [58]. Code-domain RX with >50 dB TX SI rejection have been demonstrated in 45RF-SOI with TX code-notch and RX code-pass filters operating at the same LO-defined frequency. The SOI implementation supports switch stacking to support linear operation in the TX modulator. In this case, the voltage swing is divided across

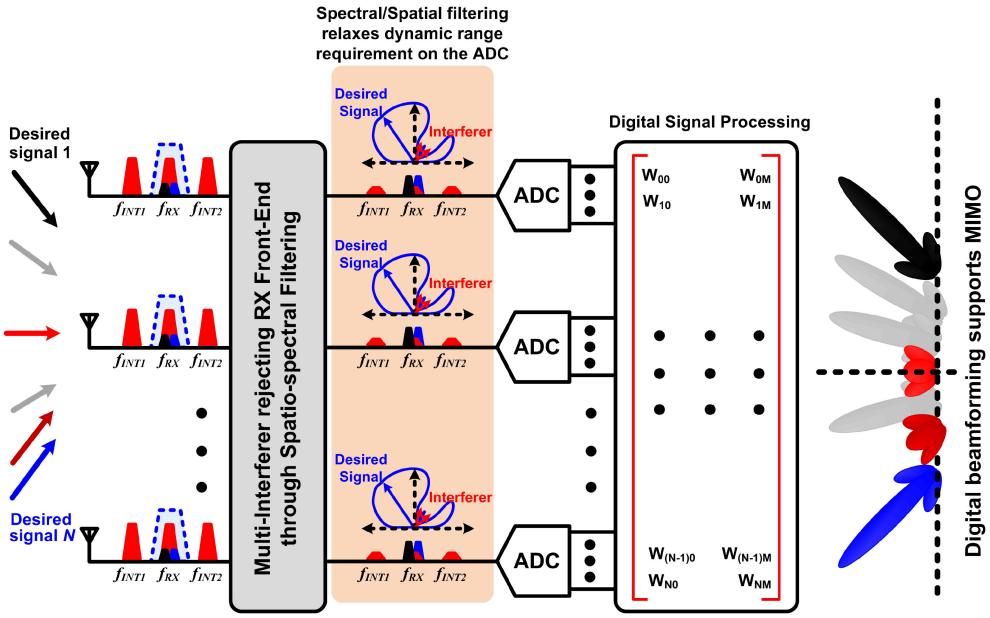

FIGURE 15. Spatio-spectral filtering in MIMO RX front-end leads to rejection of specific interferers while preserving a wide field-of-view (FoV) in each element. Subsequent digital beamforming/MIMO signal processing can lead to multibeam/MIMO operation across entire FoV.

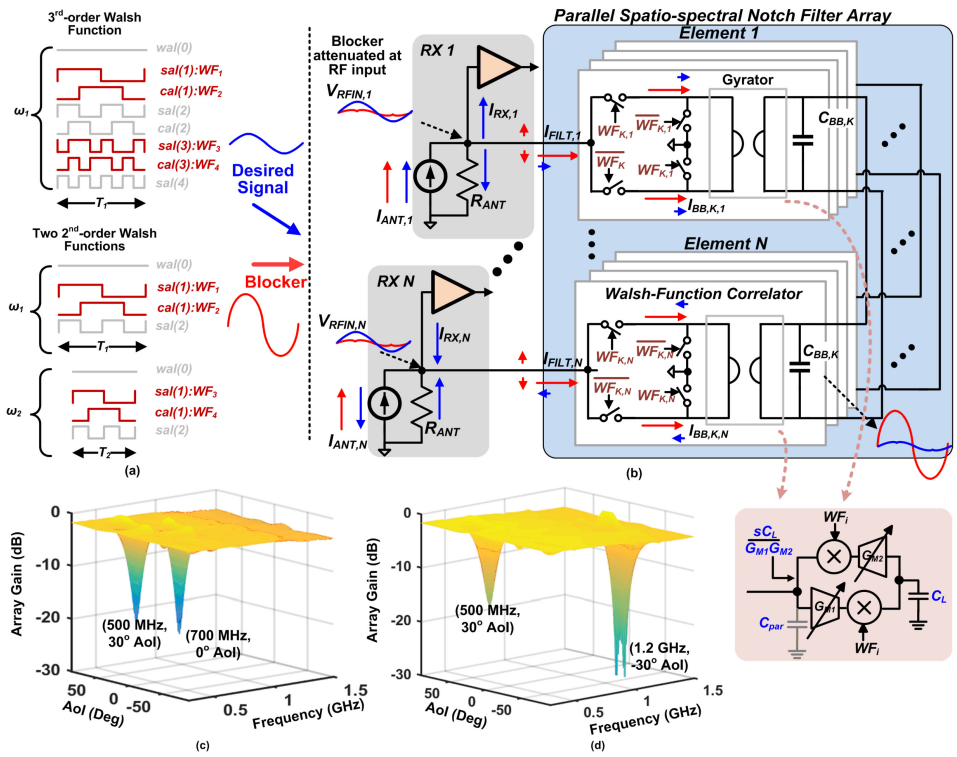

FIGURE 16. Reconfigurable spatio-spectral notch filtering using WF-seq based N-path filters where the baseband capacitors of notch-filters in different elements are tied together [51]. AoI and frequency of spatio-spectral notches are controlled by WF-seq frequency and relative phase. Measured performance showing two notches whose AoI/frequency can be independently controlled.

the transistors in the stack, thereby supporting larger overall signal swing while limiting the individual gate-drain and gate-source swings below breakdown. The RX operation from 0.25 GHz to 1.25 GHz with filter NF of ∼5 dB is supported in [59]. The linearity in RF NMOS switches is limited by the switch being enabled in the off-state for part of the RF cycle, in the case of high input swing. Given typical threshold voltages of $V_{TH} = 0.3\,V$, typical N-path switches support 0 dBm P1dB (∼0.3 V signal swing on 50 Ω.) Higher signal swing can be supported by using complementary PMOS and NMOS transistors. A chopper-based approach and transmission-gate switches improve RX P1dB to ∼10 dBm [59]. These

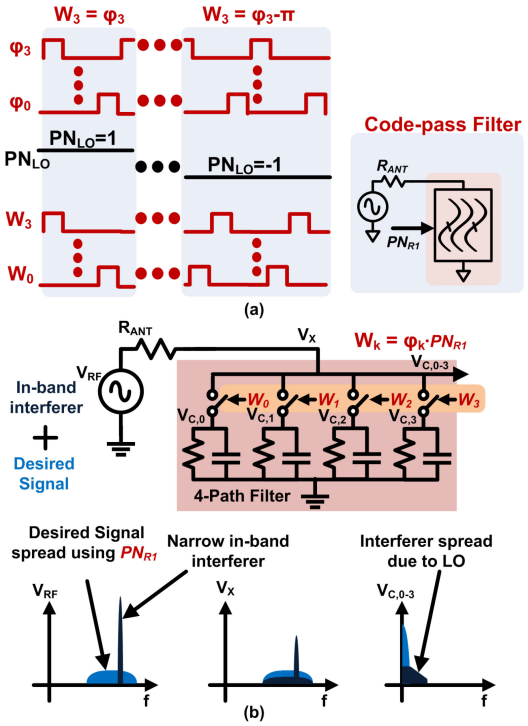

FIGURE 17. (a) LO generation by modulating NOP LO pulses with PN codes [48]. (b) Code-domain RX using N-path mixers with code-modulated LO.

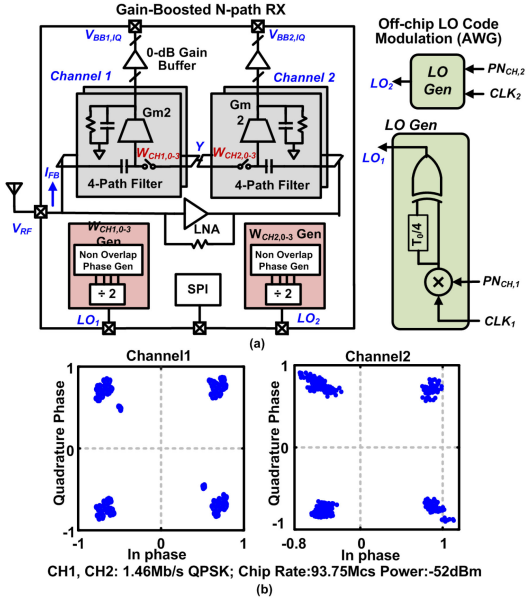

FIGURE 18. (a) Gain-boosted N-path RX with two series N-path correlators in feedback path for concurrent reception of two signals. (b) Concurrent reception of two code-modulated signals using separate codes on the two RX channels at 750 MHz [48].

techniques are also extended to non-contiguous carrier aggregation in [60]. Similarly, techniques described in prior sections in the frequency, spatial and code-domain can be combined to provide enhanced signal selection/rejection based on spectral, spatial and code-domain diversity.

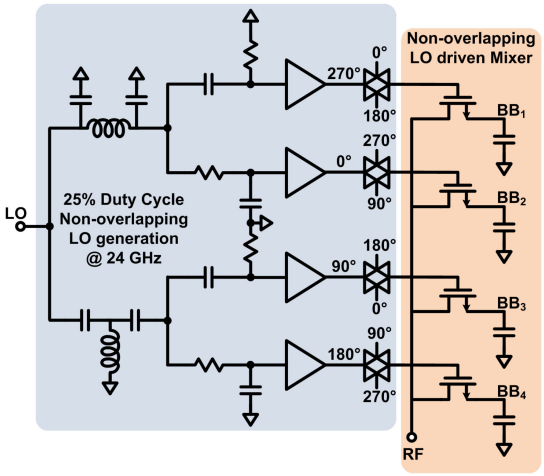

FIGURE 19. 20 GHz mixer-first architecture in [61] extends N-path operation to mm-wave in 45 nm CMOS RFSOI by using small mixer switch sizes and LO generation using tranmission gates and 50%-duty cycle quadrature LO.

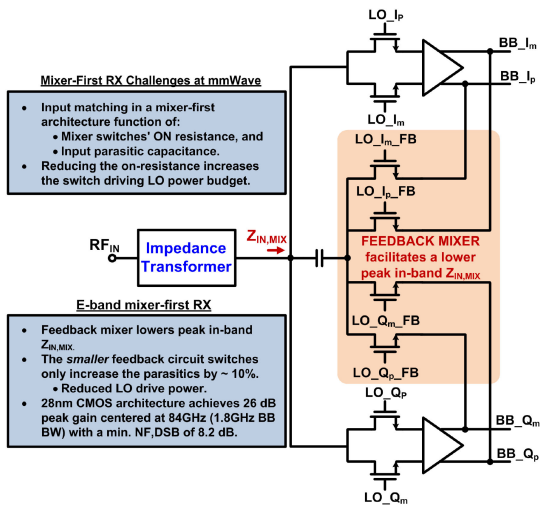

FIGURE 20. mm-wave mixer-first architecture with frequency-translational feedback reduces lower power consumption by reducing mixer switch sizes [62].

V. RECONFIGURABLE RECEIVERS AT RF AND MM-WAVE

Extending the frequency tunability of N-path receivers to higher RF and mm-wave frequencies is challenging due the input parasitic capacitance at the N-path mixer switches and power efficient non-overlapping multiphase LO generation. While $R_{SW}C_{SW}$ time constants scale with technology, even a 200 fs switch time constant, implies capacitance of 40 fF for $R_{SW} = 5\Omega$, which present a parasitic impedance of $-j200/\text{N}\ \Omega$ at 20 GHz in an N-path RX. Additionally, M-phase non-overlapping clocks at f_{LO} are typically generated from frequency-dividers operating from a $2^{M/2-1}f_{LO}$ input clock frequencies. Generating NOP for beyond 10 GHz operation would require frequency dividers operating >20 GHz, leading to increased power for LO generation. Technology scaling to 45 nm RFSOI, series inductor to resonate input capacitance, use of small mixer switch sizes, and a LO scheme relying on passive quadrature generation followed by

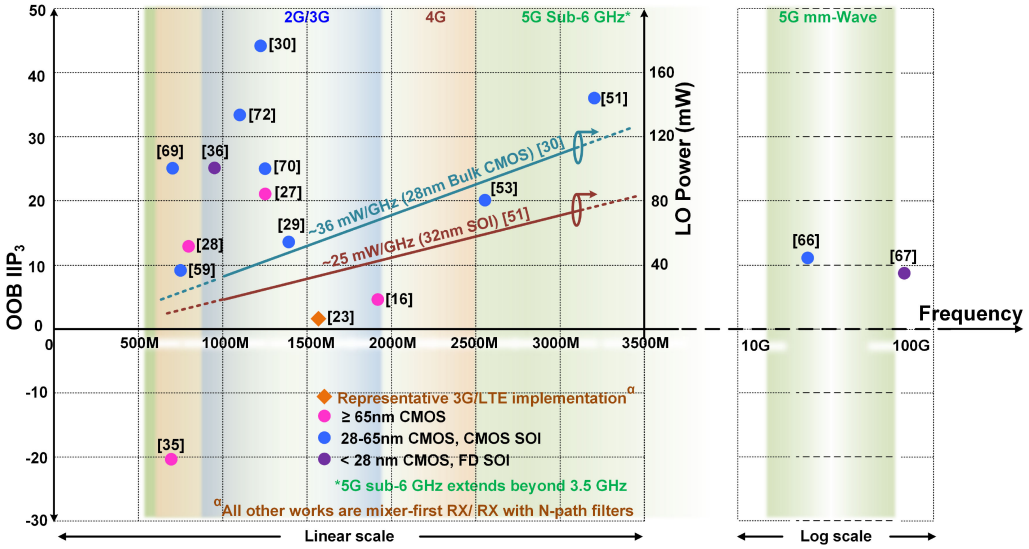

FIGURE 21. **Linearity of mixer-first and N-path RX wideband reconfigurable receivers' (shown through OOB IIP_3) across frequency. Representative 3 G/LTE focused implementation is shown in [24], with N-path mixer-first RX demonstrating substantially higher linearity, promising a path towards linear reconfigurable RX. The plot also shows LO power trends (mW/GHz) based on recent works, demonstrating the challenges of high-frequency N-path RX.**

transmission gates to generate ∼25 % duty-cycle waveforms are used in [61] to demonstrate a 4-phase mixer-first RX operating from 20 GHz to 30 GHz with 8 dB NF and 41 mW power consumption(Fig. 19).

N-path mixer-first receivers with impedance translation are implemented using bipolar transistors in [63] in order to take advantage of high-frequency performance of HBTs in SiGe and III-V technology. Impedance translation is achieved in an HBT by feedback of the baseband signal to the base of the mixer transistor along with the LO. Emitter-coupled logic based LO generation enables 4-phase NOP at 12 GHz. Wideband operation from 300 M to 12 GHz is achieved with 14 dB NF at 4 GHz RF with ∼1250 mW power consumption in a 0.13 μm SiGe BiCMOS. in [64], I-path and Q-path mixers are placed in series, which allows use of 50 % duty-cycle I and Q clocks to relax LO generation requirements. However, shunt parasitic capacitances to ground can increases mixer losses losses since they must be charged and discharged every RF cycle [48], [64], [65]. Mixer-first approaches extended to mm-wave frequencies is also an active area of research for wideband operation with low single-element power in arrays [62], [66]–[68]. Ultra-wideband mixer-first front-end based receiver for mm-wave communications bands (43–97 GHz) with a 1 GHz instantaneous bandwidth is presented in [67]. A mixer-first RX with a passive LC filter load is used in to support the wide signal bandwidths required at mm-wave with high-order out-of-band filtering [68]. Furthermore, [62] presents a mixer-first architecture with low LO driver power while ensuring wideband input match and reconfigurability at E-band. The RX makes use of a frequency-translational feedback through an auxiliary set of mixer switches around the signal path mixer switches to achieve a lower input impedance at the RX input (Fig. 20).

A scatter plot of recently published wideband receiver architectures (supporting varying degrees of reconfigurability) is shown in Fig. 21. OOB IIP_3 linearity across frequency of operation is shown in Fig. 21 for RF and mm-Wave receivers. The operational frequency ranges of standards from 2G-5G have also been highlighted, pointing to interesting trends in state-of-the-art, particularly in the densely allocated spectrum <6 GHz. Firstly, the majority of mixer-first and N-path filter-based receivers have been implemented at lower RF frequencies. While the implementations haven't focused on specific standards, the OOB IIP_3 is typically a key focus in these works. While there are several outstanding challenges that remain to be addressed, comparing the OOB-IIP_3 numbers of the N-path/mixer-first implementations with a representative reference ([24]) shows that most of these works exhibit OOB-IIP_3 >20 dBm with even higher linearity using bottom-plate switching techniques. Mixer-first mm-Wave reconfigurable receivers are still a nascent area of research and linearities are not as high as RF implementations (Fig. 21), however interferers are not as high at these frequencies. Challenges associated with parasitics coupled with LO *distribution* power at higher frequencies are currently a key bottle-neck in the higher mm-Wave frequency region. Lastly, the reported multiphase generation/distribution power numbers from some of these references demonstrate the challenges in designing N-path filter/multi-phase passive mixer-first receivers. While mm-wave receivers inherently suffer from large LO distribution power numbers, increasing the number of clock phases is a big hurdle that N-path receivers in general face at higher frequencies. Fig. 21 also shows the LO power consumption for generating four LO phases as a function of frequency, demonstrating the challenge of of extending such receivers to the higher bands in 5G.

VI. CONCLUSION

The increasing complexity of spectrum allocations and the desire for opportunistic spectrum use through carrier aggregation is motivating development of wideband reconfigurable radios. The last decade has seen extensive research on achieving receivers with wide operating range up to 6 GHz, low noise and high blocker tolerance. While current-mode and passive-mixer techniques are well-established, N-path mixer-based reconfigurable RX have emerged as a promising candidate for realizing receivers that can select/reject signals based on their properties in the frequency/spatial/code domains. Based on demonstrations over the last decade, current and future areas of research interest include (i) further reduction in power consumption of <6 GHz N-path receivers through use of passive gain and noise cancellation techniques, (ii) design of linear wideband transimpedance amplifiers since improved mixer-linearity and >200 MHz signal bandwidths result in TIA performance limiting RX power, noise and linearity [69], [70], (iii) TIA topologies with increased close-in filtering/higher-roll off to enhance out-of-band linearity [71]–[73], (iv) low-power LO generation for multi-phase RX since that remains the most significant driver of power consumption, and (v) extending wideband reconfigurable RX architectures to the spatial-domain in MIMO RX, given the widespread use of MIMO in recent and emerging sub-6 GHz wireless links [74], [75].

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