IEEE Journal of Microwaves

Received 16 September 2020; revised 24 October 2020 and 27 October 2020; accepted 28 October 2020.
Date of current version 7 January 2021.

Digital Object Identifier 10.1109/JMW.2020.3035897

Millimeter-Wave Power Amplifier Integrated Circuits for High Dynamic Range Signals

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(Invited Paper)

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This work was supported in part by the U.S. Defense Advanced Research Projects Agency (DARPA), Army Research Lab (ARL), and Army Research Office (ARO), and Air Force Research Lab (AFRL) as well as industry sponsors including Qualcomm, Intel, Qorvo, Renesas Electronics, and Analog Devices; and in part by a joint project carried out in the GigaHertz Center (Göteborg/Sweden) and financed by the Swedish Government Agency for Innovation Systems (Vinnova), Chalmers University of Technology, Ericsson, Gotmic, Infineon Technologies Austria, National Instruments, Qamcom, RISE, and Saab.

ABSTRACT The next-generation 5G and beyond-5G wireless systems have stimulated a substantial growth in research, development, and deployment of mm-Wave electronic systems and antenna arrays at various scales. It is also envisioned that large dynamic range modulation signals with high spectral efficiency will be ubiquitously employed in future communication and sensing systems. As the interface between the antennas and transceiver electronics, power amplifiers (PAs) typically govern the output power, energy efficiency, and reliability of the entire wireless systems. However, the wide use of high dynamic range signals at mm-Wave carrier frequencies substantially complicates the design of PAs and demands an ultimate balance of energy efficiency and linearity as well as other PA performances. In this review paper, we will first introduce the system-level requirements and design challenges on mm-Waves PAs due to high dynamic range signals. We will review advanced active load modulation architectures for mm-Wave PAs and power devices. We will then introduce recent advances in mm-Wave PA technologies and innovations with several design examples. Special design considerations on mm-Wave PAs for phased array MIMOs and high mm-Wave frequencies will be outlined. We will also share our vision on future technology trends and innovation opportunities.

INDEX TERMS 5G, 6G, dynamic range, energy efficiency, integrated circuits, millimeter-wave, mobile communication, OFDM, peak to average power ratio (PAPR), power amplifier, quadrature amplitude modulation (QAM).

I. INTRODUCTION

With the rapid increase of worldwide mobile data traffic, the mm-Wave spectrum (30 GHz–300 GHz) with its ample unlicensed bandwidth is believed to be the key enabler for the next wireless revolution [1]–[3]. It is envisioned that many of these mm-Wave systems will employ large-scaled arrays that are judiciously designed to boost the link performance and compensate for the path loss, channel nonidealities, and limited performance of mm-Wave electronics.

At the physical layer, power amplifiers (PAs) serve as a critical building block that governs many performance aspects of the wireless link. Reciprocally, changes at the system level due to new communication standards and applications often result in profound impacts on the PA designs. While RF PAs at GHz frequencies have experienced several generations of remarkable design evolutions, the next-generation wireless links for communication and sensing, i.e., 5G and beyond-5G, require mm-Wave PAs with radical innovations in their designs and architectures to deliver nearly "perfect" performance. Fig. 1 shows the "design hexagon" of mm-Wave PAs that highlight the desired PA performance vectors and their tradeoffs.

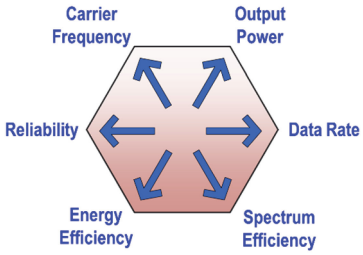

FIGURE 1. Mm-Wave PA design hexagon on performance vectors and tradeoffs.

For example, these mm-Wave PAs should deliver large output power (P_{out}) with sufficient power density to ensure the link budget and compact area compatible with the tight $\lambda/2$ array element lattice. Large P_{out} further allows array aperture reuse for concurrent multi-beam/-stream MIMOs. Covering a wide carrier bandwidth or several non-contiguous bands is critical for multi-standard or frequency-agile communication. PA reliability is also essential for robustness in large arrays.

To maximize channel throughput, mm-Wave wireless links will extensively employ complex modulation schemes, such as high-order QAMs, OFDM, and carrier aggregations; these modulation signals often exhibit large dynamic ranges that can be characterized by their Peak-to-Average-Power-Ratio (PAPR). For example, a single carrier 64 QAM signal typically has a PAPR of around 7.1 dB. Further, the 3GPP 5G NR FR2 400 MHz 2-CC (total 800 MHz) 64 QAM signal has its PAPR of 11.78 dB at a 0.01% CCDF (complementary cumulative distribution function). Therefore, PAs will routinely amplify signals whose averaged P_{out} is approximately 6–12 dB lower than the PA's peak P_{out}. In addition, although many existing radar systems use constant envelope signals, future mm-Wave radar/sensing systems are expected to support complex radar signals and concurrent multi-beams for fast frame/refreshing rates or hyperspectral sensing, which also demands PAs to support high dynamic range signals in such applications.

The extensive use of these high-PAPR signals has a profound impact on how future mm-Wave PAs should be architectured and designed. First, both high peak power added efficiency (PAE) and power-back-off (PBO) efficiency are mandatory to achieve a high average energy efficiency (PAE_{ave}) when amplifying high-PAPR signals, which directly determines the system thermal handling requirements as well as battery life or operation time for mobile devices. Secondly, these high-PAPR signals often exhibit complex constellations that require high PA linearity to preserve the signal fidelity and the subsequent link quality-of-service (QoS). Thirdly, to deliver the promised high throughput, future mm-Wave systems require Gbit/s modulation speeds, and consequently PAs need to handle these wideband dynamic signals. Therefore, in order to support the high-PAPR modulations, the next-generation mm-Wave PAs require an ultimate combination and balance of efficiency, linearity, and modulation rate, as well as the output power, carrier bandwidth, and reliability (Fig. 1).

TABLE 1 PA Power Requirements for Different Antenna Array Sizes†

N array elements	16	32	64	128	256
P_{avg} per PA (dBm)	24	18	12	6	0
P1dB per PA (dBm)	33	27	21	15	9
P_{RF} total (W)	3.9	2.0	1.0	0.5	0.25

†Computed for EIRP = 50 dBm, PAPR = 9 dB, individual antenna gain = 2 dB, and loss 1 dB per antenna connection.

The purpose of this paper is to outline the design challenges on mm-Waves PAs due to the high dynamic range signals and then review recent advances in mm-Wave PA technologies and innovations that aim at addressing these challenges. In addition, this review paper seeks to emphasize the fundamental design concepts and theories, instead of specific designs or performance. Due to the limited scope, this paper will mainly focus on mm-Wave silicon PAs, while compound semiconductor devices, their properties, and some example III-V PAs will be discussed more briefly.

This paper is organized as follows. Section II will summarize the system requirements and their implications on next-generation mm-Wave PA designs for high dynamic range signals. Our discussions will be mainly in the context of mm-Wave 5G standards and array applications. Section III will cover the mm-Wave PA architectures, fundamentals of active load modulation operations/networks, and discussions on device technologies. Section IV will showcase example PA circuits that amplify high dynamic range signals with high efficiency and linearity. Since most mm-Wave systems will rely on phased arrays or MIMOs, special considerations on mm-Wave PAs in these arrays will be discussed in Section V. Finally, we will share our views on future technology trend and research opportunities in Section VI.

II. SYSTEM REQUIREMENTS

Emerging communication systems employ array antennas to produce beams oriented towards specific receivers, and the received signal power is determined by the Effective Isotropically Radiated Power (EIRP) of the transmit array in the user's direction [4]. For ideal beam alignment, the EIRP increases as N^2, where N is the number of antennas (and the corresponding number of PAs), both because the power of the N different amplifiers is combined, and because the angular width of the beam decreases with N. To achieve an adequate link gain budget, EIRP values of the order of 40–60 dBm are typically required [5]. Table 1 below shows the corresponding power output required for array sizes of 16, 64 and 256 elements for a notional 5G small cell base station/ access point link with 50 dBm transmitter EIRP. The table indicates both the average power (P_{ave}), and the peak power required of the PA, based on the signal PAPR employed. Lower EIRP is needed for handset arrays, and higher EIRP for representative backhaul links. The table illustrates that for large N the required power per antenna falls comfortably into the realm of silicon PA technologies. This paper focuses on the designs and tradeoffs of

TABLE 2 PAPR for Various Modulations (Filter Roll-Off Factor = 0.25)

QPSK SC	16QAM SC	64QAM SC	QPSK OFDM	16QAM OFDM	64QAM OFDM
5 dB	6.9 dB	7.1 dB	9.7 dB	10.4 dB	11 dB

3GPP EVM Requirements [6]

BPSK	QPSK	16QAM	64QAM	256QAM
30%	17.5%	12.5%	8.0%	3.5%

mm-Wave PAs operating at these medium/high power levels, e.g., OP1 dB $\geq$15 dBm.

The PAPR requirement emerges from the desire to make efficient use of the available spectrum. It is commonplace for present terrestrial communication systems to use high order QAM, thus increasing the number of bits transmitted per Hz of spectrum by a factor of 2 to 6 (QPSK to 64 QAM). To counter time delay spread and multipath-induced inter-symbol interference, OFDM waveforms are also widely used, in which a number of subcarriers are independently modulated using a QAM approach. The OFDM signals have higher PAPR than the corresponding single carrier (SC) waveforms. Table 2 lists the peak-to-average power requirements for representative modulation standards (which in detail depend on spectral filtering).

The modulation techniques and their associated high PAPR requirements pose a major challenge for reaching high average amplifier efficiency PAE_{ave}. In addition, they place strong constraints on the amplifier linearity. In order to distinguish the transmitted bits within the received constellations, the overall errors created by the link must be kept within bounds. Table 2 lists the allowable EVM (normalized to the rms signal amplitude) for the various modulation schemes [6]. Within the link, it is typical to allocate a prominent part of the error budget to the PA, but there are other blocks that must also be accommodated (particularly related to phase noise of the frequency synthesizers). At GHz RF frequencies (e.g., cellular band), correction of amplifier nonlinearity error resulting from nonlinearity (AM-AM distortion, AM-PM distortion, and memory effects) is frequently accomplished by digital predistortion (DPD) techniques as a standard practice. DPD is used in most base stations and some handsets. It is currently regarded as unrealistic from power, cost and complexity perspectives to have adaptive digital corrections for each PAs in the array, however, let alone running DPD at GHz modulation rates for mm-Wave PAs. An important goal of PA research is, therefore, to maintain sufficient linearity to achieve EVM goals without DPD. An added complication is related to the fact that the load impedance provided to the PA is not necessarily a constant 50Ω. For handsets, it can be dramatically affected by reflections from nearby objects. While classical base stations are typically immune from this, future base stations and access points may encounter sporadic random reflections. In Section IV, we will discuss that, more fundamentally, as the beam is steered in an array, the phasing of outputs between neighboring antennas and PAs changes. The interaction between them through antenna mutual coupling leads to a time-varying change in the load impedance experienced by each PA that can be of order 2:1 VSWR or larger in arrays with wide-scanning angles.

While meeting all the aforementioned requirements, an important PA design objective is to improve power efficiency, both to alleviate heatsinking problems in the arrays, and to minimize prime power requirements (particularly for battery-operated systems). Target PA average efficiencies PAE_{ave} on modulation signals are in the range of 10–30%. Although some recently reported PA designs start to achieve such PAE_{ave} values, it is still very challenging in general to reach the required range of PAE_{ave} for the large dynamic range signals employed in 4G and 5G, also considering the GHz modulation rate and linearity requirements. It must be noted that for communication systems where the cost of spectrum is not extremely high (such as very small cells or space systems) or radar/sensing systems, other modulation formats can be used with lower dynamic range and linearity requirements, that will contribute to higher power and PAE.

III. MM-WAVE PA ARCHITECTURES AND TECHNOLOGIES FOR HIGH DYNAMIC RANGE SIGNALS

In this section, we will outline the specific design challenges of high-efficiency and high-linearity mm-Wave PAs for high dynamic range signals. Our discussion will cover the PA architectures, active load modulation operations/networks, and device technologies. Many of these challenges and considerations for mm-Wave PAs are evidently distinct from those of the low-GHz RF PA designs.

A. ARCHITECTURES

The research on enhancing the PA linearity and PBO efficiency has a long history. Essentially, the related architectures can be divided into: active load modulation, direct load modulation, or supply/polar modulation. The active load modulation architectures typically employ two (or more) PAs that operate at the same carrier frequency and interact with each other through a load modulation network to enhance the over PA back-off efficiency. In 1935, H. Chireix proposed the Outphasing architecture that used two nonlinear outphased amplifiers with constant envelopes [7] (Fig. 2(a)). One year after, in 1936, W. Doherty described the Doherty architecture that used two or more linear PAs to actively load-modulate each other and enhance the whole PA back-off efficiency [8] (Fig. 2(b)). In contrast, the direct load modulation or supply/polar architectures typically have one PA path amplify the carrier frequency signal, while the other path controls the supply amplitude or load impedance based on the real-time envelope. An envelope elimination and restoration (EER) technique was first introduced in 1952 by L. Kahn [9], and it was later evolved to the envelope tracking (ET) technique that was described by A. Saleh and D. Cox in 1983 [10] and B.D. Geller, F.T. Assal, R. K. Gupta, and P. K. Cline in 1989 [11] (Fig. 2(c)). In addition, in recent years, RF power DACs were introduced [13]–[15] (Fig. 2(d)). With their versatile

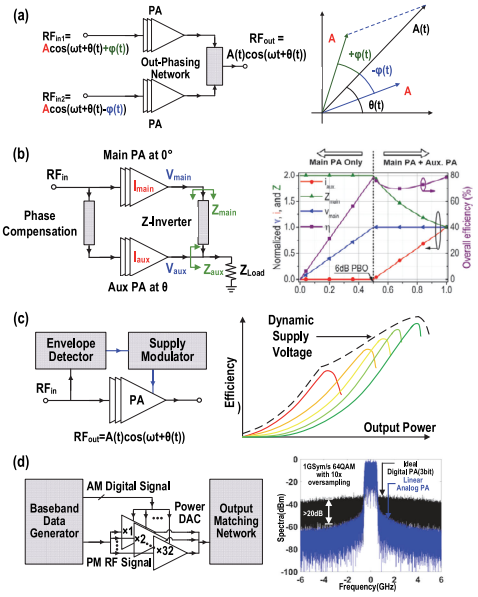

FIGURE 2. PA architectures for back-off efficiency enhancement: (a) Outphasing, (b) Doherty, (c) Supply/polar modulation, (d) RF power DAC.

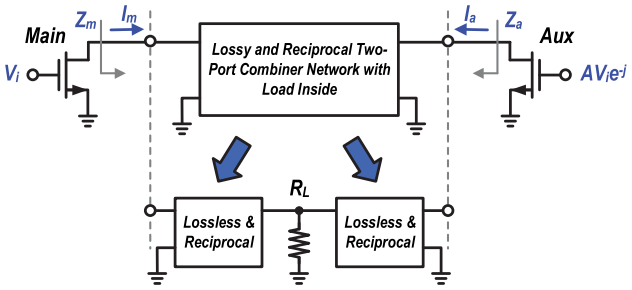

FIGURE 3. Illustration of the black-box design technique in [21], [22], where the Main- and Peaking-/Aux- combiner networks are synthesized to present the optimum peak/back-off load impedances to the transistors.

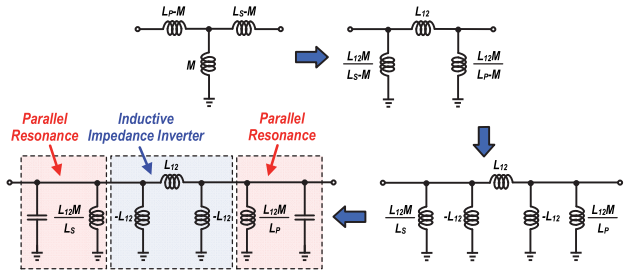

FIGURE 4. The passive network transformation that converts a physical transformer to an inductive impedance inverter. Note that the two extra parallel inductors are resonated out by loading capacitors [103].

digital controls, RF power DACs can be employed as the basic elemental PAs to construct active load modulation PAs, such as Outphasing [16], [17], and Doherty topologies [18], [19].

B. ACTIVE LOAD MODULATION NETWORKS

Among the aforementioned PA architectures, active load modulation networks are considered as a particularly promising solution for 5G/6G applications due to their potential capability of supporting GHz modulation bandwidth. On the other hand, although envelope tracking (ET) PAs and traditional power DACs do not preclude their implementations at mm-Wave, it is challenging for them to support GHz modulation rate while keeping high efficiency and linearity. Therefore, in this paper, we mainly focus on the two active load modulation PA architectures, Doherty and Outphasing PAs, as well as their variants.

A key component in active load modulation PAs is the passive load modulation networks. These passive networks govern how different PA paths should interact with each other as well as the resulting modes of PA operation, efficacy of the back-off efficiency enhancement and the back-off depth, overall PA efficiency, and PA carrier and modulation bandwidths. Although the classic Doherty or Outphasing PA load modulation networks often use $\lambda/4$ transmission lines (T-lines) as impedance inverters, lumped-element approximates instead of $\lambda/4$ T-line are often used in practical integrated RF/mm-Wave PAs due to their compact sizes.

However, approximating classic $\lambda/4$-T-line based load modulation networks inevitably restricts the design space. An alternative powerful approach is to analytically synthesize the Doherty (as well as Outphasing) combiner networks, as proposed in [20]. As illustrated in Fig. 3, this so-called *black-box* combiner synthesis approach begins by specifying the desired output load impedance from large-signal load pull simulations or experiments, for full power and at power back-off, together with the peaking (auxiliary) amplifier output impedance when it is off. An analytical approach is then used to determine an ideal lossy 2×2 impedance matrix with the load embedded, which can satisfy these requirements simultaneously. Conditions, including the peaking (auxiliary) amplifier branch phase shift, are then determined, which allows the impedance matrix to be represented as a combination of two lossless networks together with an external resistor, e.g., a 50Ω load, which aggregates all the losses [21], [22]. As illustrated by circuit examples in the following section, when implemented with practical components this "ideal" combiner, in many cases, has much lower insertion loss than other designs as it integrates matching, load-modulation and impedance transformation functionality all together in its synthesis.

Many mm-Wave PAs, especially in silicon technologies, often adopt the differential configuration to allow capacitive neutralization for gain and stability enhancement, easy biasing/supply feeding, and extra power combining. This stimulates transformer-based Doherty/Outphasing load modulation networks to use transformer's inherent differential to single-ended conversion and avoid additional balun/loss [23], [24], [73], [102], [103]. It is shown that a physical non-ideal transformer can serve as an equivalent inductive impedance inverter with positive/negative inductor-based π-network, while a positive/negative capacitor-based π-network can serve as a

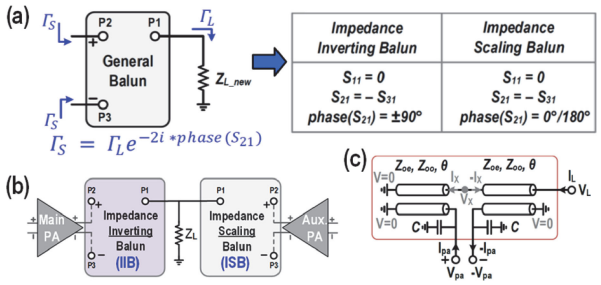

FIGURE 5. (a) Illustration of the general 3-port balun modeling and its impedance inverting/scaling behavior determined by the balun transmission coefficient S_{21} phase. (b) Using impedance inverting balun (IIB) and impedance scaling balun (ISB) as a Doherty active load modulation network. (c) Implementing IIB and ISB using couplers [25].

capacitive impedance inverter [103], see Fig. 4. After absorbing the negative elements, such impedance inverters can be used to construct Doherty/Outphasing load modulation networks with built-in balun functionalities [103].

It should also be mentioned that recent research has been exploring new networks for broadband (over-an-octave) active load modulation operations (Section IV. F). Examples include the 90° coupler used in the Load Modulation Balanced Amplifier (LMBA) [104] and the 180° coupler balun used in a broadband Doherty PA [112].

Moving to high mm-Wave frequencies (W-band and above), transformers often experience insufficient self-resonant frequency (SRF) without becoming exceedingly small and limiting the magnetic coupling, while lumped/distributed networks require multiple passive components as well as area overhead and loss. In contrast, couplers and coupled T-lines are believed to offer very promising solutions at high mm-Wave frequencies that can achieve all the desired Doherty/Outphasing PA output network functionalities, including load modulation, impedance transformation, power combining, and balun conversion, all within a compact area. A recent design in [25] shows that a coupler balun can be designed to function as an impedance inversion balun (IIB) or an impedance scaling balun (ISB), if the transmission coefficient phase from the balanced ports to the unbalanced port is set as 90°/270° or 0°/180°, respectively. Thus, Doherty active load modulation network can be realized by joining the IIB and ISB in a parallel configuration Fig. 5. A 60 GHz coupler-based Doherty PA is demonstrated with a best reported PBO efficiency enhancement (×1.4 over class-B PA at 6 dB PBO) and the best reported PAE_{ave} of SC 64 QAM signals. Moreover, triaxial baluns based on coupled transmission lines have been used in classic broadband push-pull PAs [26]. Recent designs show that a triaxial balun can be judiciously designed to realize Outphasing [82] and Doherty-Outphasing continuum [92] operations at mm-Wave frequencies. Chip demonstrations have shown outstanding back-off efficiency performance at the 28 GHz range and outstanding modulation efficiency with OFDM signals, which can be potentially extended to high mm-Wave frequencies.

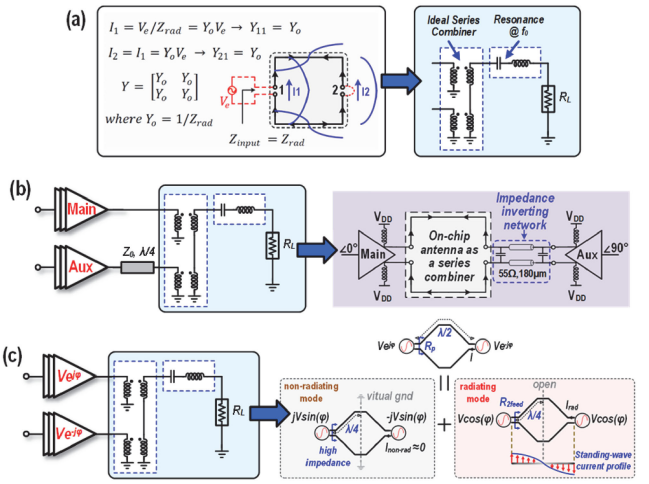

FIGURE 6. (a) A two feed-loop antenna behaves as an ideal series power combiner. The series power combiner can be used in (b) a series Doherty PA architecture [36] or (c) a classic Outphasing architecture [35].

Further, high mm-Wave systems necessitate close integration of antennas and electronics, which interestingly creates a new frontend design paradigm with holistic antenna-electronics co-designs. Multi-feed/multi-port antennas and their interfacing with frontend electronics have attracted an increasing interest in the community [27]–[45]. The unique design freedom and flexibility of multi-feed/multi-port antennas can be exploited to achieve new active load modulation architectures. For example, it is shown that a dual-feed square loop antenna is identical to an ideal series combiner in terms of its driving impedance. This property can be leveraged to achieve on-antenna two-way Doherty or Outphasing PAs/transmitters, where the major active load modulation networks are realized at the antenna level, saving on-chip passives and reducing losses [35], [36] (see Fig. 6). Moreover, it is shown that innovations on multi-feed patch-like antennas can achieve Doherty-like behaviors as well [40]. Further, near-field antenna-antenna coupling can be exploited for high-order Doherty active load modulation for on-antenna deep PBO efficiency enhancement up-to 9 dB [42]. Other antenna-electronics co-designs have realized PAs/transmitters with on-antenna power combining [31]–[34] and Doherty-like modulation by near-field antenna-antenna couplings [27], [28].

C. DEVICE TECHNOLOGIES

Mm-Wave PAs have been enabled by rapid advances in high frequency capabilities of transistors stemming from dimensional scaling both in Si and III-V materials. The device f_t is closely related to transit time of electrons through critical device regions (channel or base), although modified by parasitic capacitances. For MOSFETs, for example, f_t is approximately given by

$$f_t = \frac{g_m}{2\pi\left(C_{ox} + C_{para}\right)} = \frac{1}{2\pi}\frac{v}{L}\frac{1}{\left(1 + C_{para}/C_{ox}\right)} \quad (1)$$

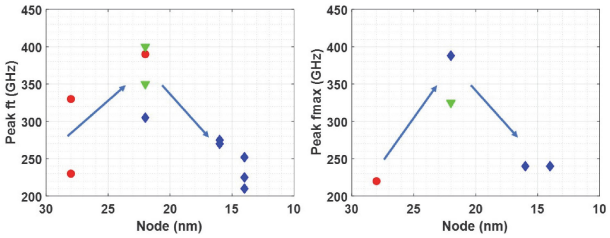

FIGURE 7. Intrinsic f_t and f_{max} values for Si MOSFET IC technologies as dimensions have been scaled (circles: bulk CMOS; triangles: FD-SOI; diamonds: FinFET) [47].

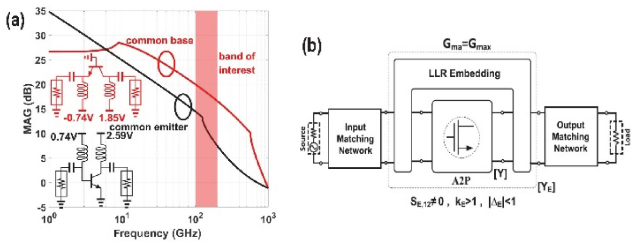

FIGURE 9. (a) A common-base PA using intrinsic InP device behaviors [50]. (b) A common-source amplifiers with embedding for device gain boosting [51].

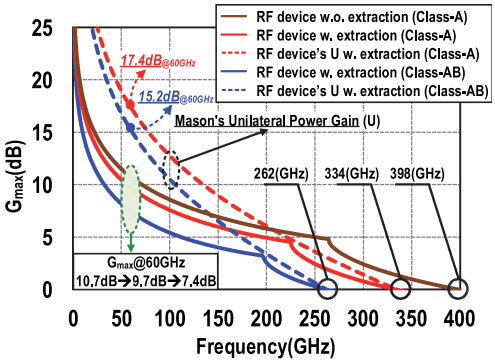

FIGURE 8. Simulated device power gain of a 45 nm CMOS SOI device.

where v is an effective electron velocity (intermediate between saturation and ballistic velocity [46]), L is channel length, C_{ox} and C_{para} correspond to device intrinsic and parasitic capacitances. As dimensions (particularly L) have shrunk, driven primarily by digital circuit requirements, f_t has increased to the 300–400 GHz range for Si MOSFETs.

Dimensional scaling below about 22 nm has not provided further increases in f_t, however, because of the dominance of parasitic capacitances in devices designed for digital circuits [47], see Fig. 7. Device f_{max} has also increased, although not as emphatically in Si MOSFETs (up to 350–400 GHz) because of the reduced relevance of f_{max} to digital circuit performance; by contrast in SiGe HBTs f_{max} has reached 700 GHz [48], and InGaAs pHEMTs f_{max} has reached 1.5THz [49]. It is desirable to have f_t and f_{max} values more than 3× of the carrier frequency in order to attain sufficient device power gain and high power efficiency.

Indeed, one of the fundamental challenges of designing high-frequency PAs of active load modulation architectures is the lack of device power gain at mm-Wave or sub-THz frequencies. Fig. 8 shows the simulated power gain of a 45nm CMOS device. At 60 GHz the device G_{max} drops from 10.7 dB (class-A biasing without layout parasitics) to only 7.4 dB (class-AB biasing with layout parasitics). Note that the G_{max} is the best achievable small signal power gain. In practical PA designs, large-signal operation and load-line matching will further degrade the actual device power gain. While device unilaterization can provide device power gain to Mason's Unilateral Power Gain U, it requires broadband capacitive neutralizations with differential PA operation in practice.

It is also interesting to note that selected circuit designs and topologies actually can allow amplifiers to operate close to the f_{max} of the technologies. Examples include common-base PAs using InP devices leveraging the intrinsic InP device behaviors [50] or common-source amplifiers with narrow-band embedding feedback for device gain boosting up-to *4U,* where U is the device Mason's Unilateral Power Gain [51] (Fig. 8).

On the other hand, for PAs, performance of output power P_{out} and efficiency PAE are influenced by factors that go well beyond gain. The maximum voltage that can be handled is a critical issue, which in turn is related to the breakdown electric field of the material and the distance over which the electric field appears. The channel length scaling of Silicon devices has thus come hand-in-hand with reduced voltage handling. GaAs and InP technologies enjoy a ×1.5-×2 advantage over Silicon in breakdown electric field, and GaN enjoys a ×15 advantage relative to Silicon, so that these technologies are preferred for high output powers. At modest output power levels, Silicon devices are often used in series "stacked" configuration, allowing voltage sharing among multiple transistors to effectively boost their total breakdown voltages [52], [53].

To attain high efficiency, it is important to have a low V_{min} (the lowest V_{ds} or V_{ce} at the maximum output current), so that high carrier mobility is also required. A factor $(V_{max}-V_{min})/(V_{max}+V_{min})$ enters into the efficiency calculation for most PAs [5]. At maximum power, this factor can be 0.9 or above for GaN or GaAs, 0.8 and above for SiGe, and drops generally to 0.6–0.7 for Silicon MOSFETs, although the factor can be increased if devices are operated well below their rated current and power. A dual-drive PA topology is proposed to alleviate the effect of V_{ds} and improve PA efficiency even with limited supply voltages [54].

Linearity issues are potentially more important for mm-Wave PAs than for lower frequency circuits, because of the difficulty of using external predistortion. A variety of architectural issues influence linearity in high power devices. Among them, the variation of output capacitance with output voltage which appears when the device uses a large spacing between gate and drain, or equivalently between base and sub-collector. Device linearity can sometimes be assured with

simple tradeoffs with gain and bandwidth: adding external parasitic resistances and capacitances which typically are voltage independent can mask intrinsic nonlinear device conductances and capacitances.

Beyond strictly peak performance, technology choices for PAs in mm-Wave arrays are influenced by cost, reliability and integration capability. In representative systems, the IC that connects to the antenna must incorporate PAs, switch (for time-division duplex systems), low-noise amplifiers (LNAs), and preferably phase shifters and variable gain amplifiers (VGAs) to shape the signal (or potentially in the future, DACs and ADCs). Silicon CMOS and BiCMOS processes enjoy a considerable advantage in this regard. It is noteworthy that Silicon IC processes have expanded to allow for thick (2–4 μm) copper and aluminum layers to reduce resistances, and thick (10–15 μm) dielectric layer to allow implementations of T-lines with relatively low loss on the top surfaces of ICs, rather than follow the traditional III-V microstrip approach with ground on the backside of the substrate.

IV. CIRCUIT DEMONSTRATIONS

This section provides illustrative mm-Wave circuit demonstrations related to the power amplifier architectures that are reviewed above. It should be mentioned that recent research has shown that many active load modulation PAs are capable of achieving excellent linearity and supporting high data-rate complex modulations without the overhead of digital predistortion or major additional power backoff [76], [92], [103].

A. CLASS AB-BIASED PAS

To evaluate advanced amplifier architecture performance, it is useful to compare it to results obtained for more conventional Class AB bias arrangements and simpler architectures [54]–[70], [96].

In mm-wave applications, considerable work has been reported using differential amplifier configurations together with neutralization capacitors to counter the effects of transistor feedback capacitance [71]. Transformer baluns and combiners are frequently used at input and output as well as the inter-stage matching networks. Different methods for built-in AM-AM/AM-PM linearization have been proposed and demonstrated [62]–[66]. Various harmonic termination schemes have been reported to further improve the PA efficiency [67]–[70]. For 5G 28 GHz applications, output power can reach 19 dBm and 44% PAE, while 6 dB backoff PAE can reach above 20%. Fig. 10 illustrates results in 28nm CMOS incorporating 2nd harmonic shorts to enhance linearity [56].

B. DOHERTY PAS

At present the major technology workhorse for high back-off efficiency is the Doherty PAs. This design is used for virtually all base stations for 3G and 4G, generally in conjunction with DPD linearization. In the mm-Wave regime, however, as noted above the basic Doherty PA architecture is more difficult to implement efficiently, since the increased loss of the λ/4-line

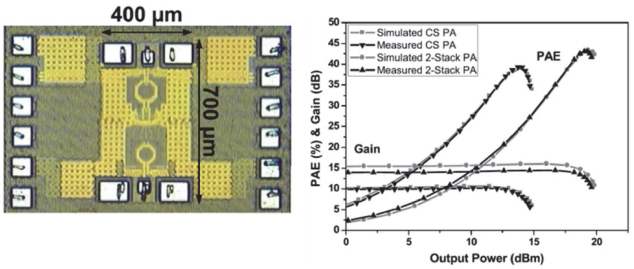

FIGURE 10. Chip photograph and performance of a 28 GHz differential Class AB power amplifiers with linearity enhancement [56]. Results are shown for common-source unit amplifiers and for combinations of two stacked FETs.

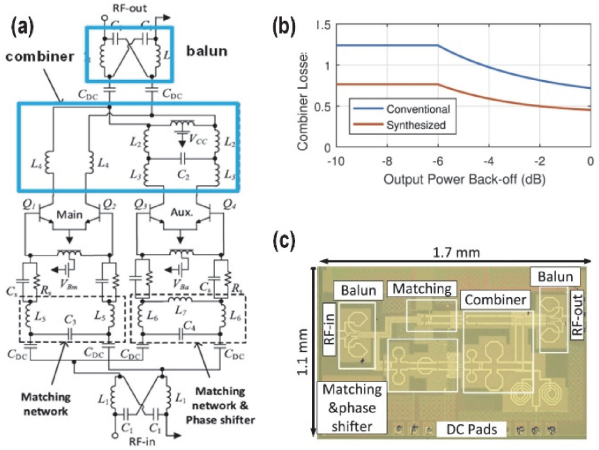

FIGURE 11. A 30 GHz Differential Doherty PA with low loss synthesized output combiner implemented in a SiGe HBT process [75]. (a) The PA circuit schematic. (b) Simulated passive efficiency of the low-loss synthesized output combiner vs. output power PBO levels. (c) Chip microphotograph.

impedance inverter reduces the output power and efficiency as well as the resulting active load modulation.

Initial demonstrations of Doherty PAs in the mm-Wave regime are accomplished in CMOS, CMOS-SOI and GaAs technologies [72]–[74] at 42 and 82 GHz, using classical Doherty combiners or transformer-based designs. Efficiencies at 6 dB back-off for 42 GHz reached 17% (CMOS-SOI) and 23% (GaAs HEMT).

For the mm-Wave Doherty PA designs, output combiner approaches with lower loss are worthwhile. mm-Wave design based on the black-box combiner synthesis technique described in Section III.B is implemented as a differential Doherty PA using SiGe HBTs [75], as pictured in Fig. 11. In operation at 30 GHz, the amplifier exhibits a 6 dB PBO PAE of 24%, with a saturated P_{out} of 21 dBm.

Another application of this synthesis technique, shown in Fig. 12, uses CMOS-SOI unit amplifiers, in a single-ended Doherty configuration.

A symmetric Doherty amplifier is designed using a pair of the 2-stack PAs [76]. The designed combiner (and the output impedance matching network) had insertion loss of

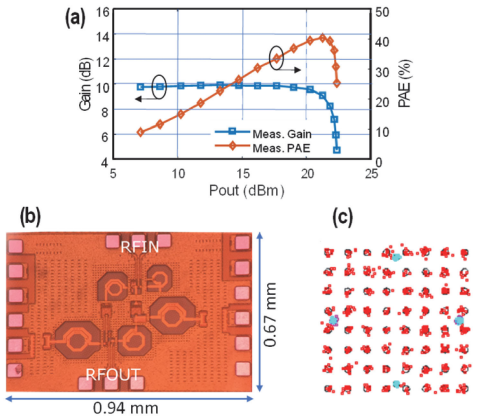

FIGURE 12. A 28 GHz Doherty PA implemented in CMOS-SOI: (a) measured gain and PAE vs P_{out}; (b) chip photograph; (c) measured output constellation for 800 MHz 64 QAM OFDM signal without DPD [76].

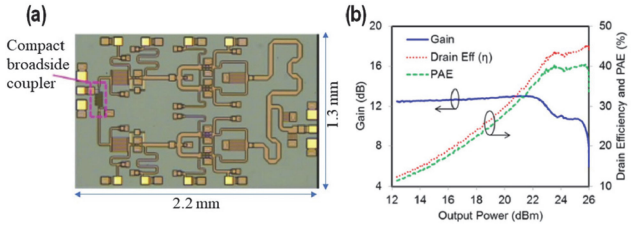

FIGURE 13. A Ka band Doherty implemented in 150nm GaAs pHEMT technology: (a) chip photograph; (b) measured gain and PAE vs output power [77].

only 0.5 dB (compared with more than 1 dB for a more conventional Doherty combiner design), allowing a peak PAE of 40% and P_{sat} of 22 dBm, with a back-off PAE of 28%. With appropriate biasing, the gain curve versus P_{out} does not show significant variations at the onset of peaking/auxiliary amplifier turn-on. As a result, without DPD it is possible to obtain a good constellation with 800 MHz 64 QAM OFDM signals, with average P_{out} of 13 dBm and PAE of 17.4%.

The Doherty architecture has also been explored in III-V PAs for mm-Wave 5G applications. A 28 GHz PA implemented in 150 nm GaAs pHEMT technology is illustrated in Fig. 13, [77]. The circuit uses low loss microstrip lines (with ground on substrate backside) in a classical Doherty design, and achieves peak PAE of 40% and 6 dB back-off PAE of 29% with a P_{sat} of 26 dBm.

The scaling of GaN devices to shorter gate lengths has also enabled high frequency Doherty PAs to be realized in this technology. Initial demonstrations are made at 20 GHz for satellite systems using 100nm gate lengths and peak output power of 35 dBm [78]. There is at present significant interest in the development of GaN Doherty PAs at 28 GHz and above to reach higher power levels needed for some 5G applications. Using 150nm GaN, MMICs are demonstrated in [79] covering 27–40 GHz, reaching 35.6 dBm P_{sat}, and 23% PAE at 6 dB backoff (Fig. 14). Operation with 64 QAM 100 MHz signals is successfully demonstrated without DPD.

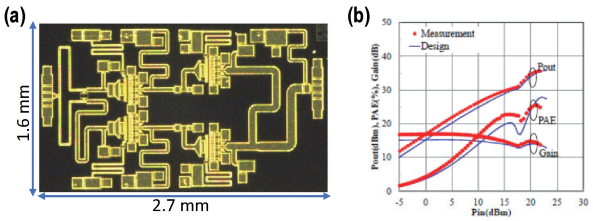

FIGURE 14. A Ka band 3.6 W 2-stage Doherty PA implemented in 150nm GaN technology: (a) chip photograph; (b) measured and simulated gain, output power and PAE vs input power [79].

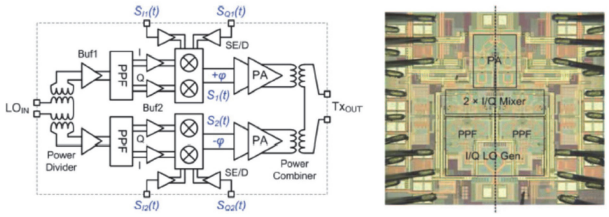

FIGURE 15. Architecture and chip photograph of Outphasing transmitter [80].

As frequencies increase beyond initial mm-Wave bands at 20–40 GHz, the lack of gain is a severe challenge as described above. For the Doherty or Doherty-like PA architectures, which most rely on sequential turning-on of multiple PA paths depending on the input, the auxiliary PA paths are often biased in class-C mode and kept off at low signal levels which means that 50% of the input power is consumed while generating no outputs. As a result, the gain of Doherty PAs is often lower than their class-AB counterparts by at least 3 dB, making their implementations challenging at higher mm-Wave/sub-THz bands. In addition, class-C mode PAs often result in lower output power and soft turning-on characteristics, necessitating asymmetric Doherty topologies with more design complexity. Power-dependent adaptive bias networks are being introduced to address this problem.

C. OUTPHASING PAS

As described in Section III, in an ideal Outphasing PA the linearity dependence on the amplifier sub-blocks is eliminated because the signals they produce have constant voltage amplitude as the load impedance seen by the amplifier's changes. In an initial mm-Wave demonstration, an Outphasing PA is used to provide linearity dramatically improved over a similar amplifier using a cartesian I/Q architecture [80]. At 60 GHz, power amplifier efficiency reached 25% in 40nm CMOS. The corresponding Outphasing combiner is implemented using series-combined transformers and is incorporated along with signal generation circuits in an overall transmitter chip (Fig. 15), although it does not make use of the Chireix compensation strategy for back-off efficiency enhancement.

Mm-Wave PAs are in fact much closer to current sources than voltage sources. Although some Outphasing PA designs claim current-mode operations, they still need voltage source

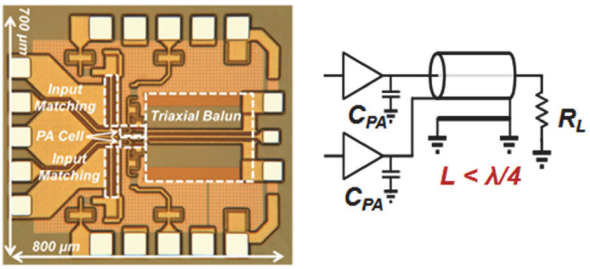

FIGURE 16. A SiGe 28 GHz Outphasing PA microphotograph and simplifier circuit schematic with a triaxial Chiriex combiner [82].

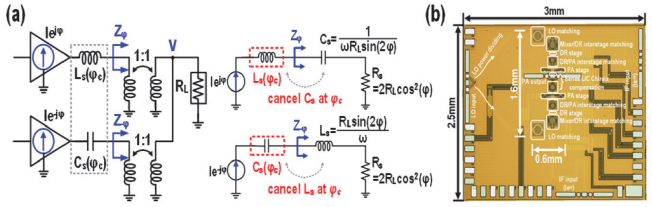

FIGURE 17. (a) Inverse Outphasing architecture using two current-mode mm-Wave PAs, one parallel power combiner, and a series Chireix compensation network. (b) The microphotograph of a 28 GHz inverse Outphasing PA in 45nm CMOS SOI process [122].

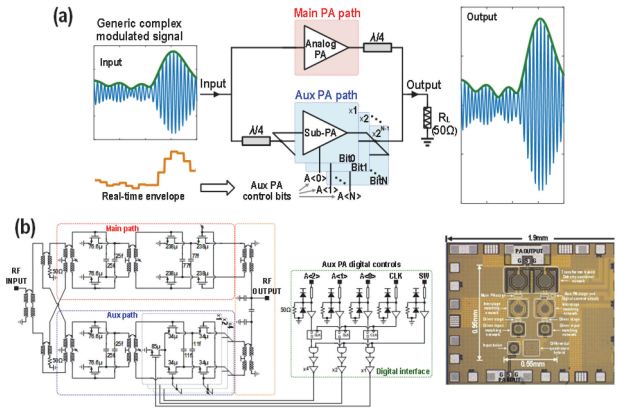

FIGURE 18. (a) Mixed-signal Doherty PA operation principle. (b) Circuit schematic and microphotograph for a 28 GHz implementation in Globalfoundries 45nm CMOS SOI process [85].

approximations in their designs and operations [83], [118]–[121]. In recent embodiments, the signals provided to the transistor amplifiers are generated as nonlinear functions of the input signals, taking into account the device nonlinear transconductance and the specific load impedance to provide the desired constant output voltage [81]–[83]. Additionally, at low P_{out} levels, it is more efficient to change from the Outphasing operation to the more conventional class B operation to improve the PA efficiency, in which both branch amplifiers operate with in-phase combining and signal-dependent output amplitude levels [84]. These approaches are used in a recently reported 28 GHz SiGe HBT based amplifier shown in Fig. 16, [82].

Building block amplifiers are cascode combinations, allowing 23 dBm P_{sat} to be obtained. A Chireix-style output combiner is implemented by using a triaxial T-line combiner approach, in which the line length is adjusted to provide the needed shunt (Chireix) reactance as well as match the transistor output capacitance. The PAE at 6 dB back-off reaches 34.5%, among the highest reported values for 5G mm-Wave PAs. In this reported amplifier, two inputs are required in order to produce accurately linear outputs. The difficulty of generating the two input signals to supply to the two branch amplifiers is an additional challenge associated with the Outphasing PAs. To attain a low EVM, high bandwidth digital modulators and upconverter chains are typically required. In [80] an on-chip signal generator or modulator is implemented and used to provide 16 QAM outputs.

On the other hand, an inverse Outphasing PA proposed recently is demonstrated based on a true current source driving condition as the circuit duality of the classic Outphasing PAs with a voltage course driving condition. Correspondingly, the inverse Outphasing PA employs a simple parallel current power combiner and a series Chiriex compensation network. Its inherent current source driving condition makes the inverse Outphasing more conducive for high mm-Wave applications [122], see Fig. 17.

D. MIXED-SIGNAL DOHERTY PA

Due to the sequential amplification nature of a Doherty PA, a major challenge in its mm-Wave design is to control and ensure the optimum cooperation of the Main and Aux PAs. In other words, the Aux PA should be turned on at the right power level to avoid Main PA gain compression and nonlinear distortions (turning-on too late) or PBO efficiency degradation (turning-on too early). Moreover, the Aux PA should also follow a desired gain relationship with the Main PA to optimize the overall AM-AM/AM-PM of the Doherty PA.

Traditionally, this Main/Aux PA cooperation is achieved by biasing the Aux PA in the class-C region with adaptive biasing circuits, often requiring trial-and-error design practices. While voltage-/current-mode RF DACs can be used to address this issue at low-GHz, it is yet not suitable for mm-Wave PAs (Section III.A) due to the limitation on practical ENOBs and AM/AM or AM/PM synchronization for GHz modulations.

To address this challenge, a mixed-signal Doherty power amplifier (MSDPA) architecture is proposed for simultaneous linearity and efficiency enhancement at mm-Wave, Fig. 18, [85]. The MSDPA comprises one analog power amplifier (PA) as the main PA and one binary-weighted digital PA as the auxiliary PA, while its input is a generic complex envelope-varying modulated signal. Based on the real-time amplitude-modulated (AM) envelope, the auxiliary digital PA weightings are dynamically turned on to perform optimum Doherty load modulation for optimized linearity and back-off efficiency. Moreover, quantization noise is largely suppressed by the mixed-signal Doherty operation and nonuniform quantization (NUQ), while spectral images are substantially reduced by

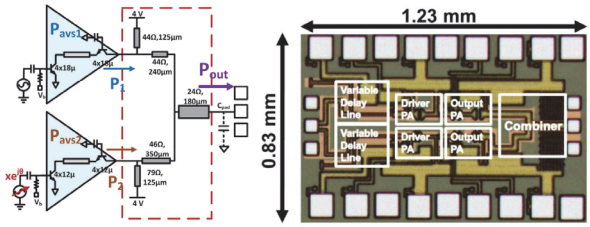

FIGURE 19. **Frequency reconfigurable dual-input mm-Wave power amplifier with active impedance synthesis [90], [91].**

the quasi first-order hold (FOH) operation, which together achieve super-resolution over conventional digital PAs. This makes MSDPA particularly conducive to mm-Wave or compound PA designs by obviating the need for large ENOBs on AM digital controls while still achieving a high linearity. A 3-bit MSDPA is implemented at 28 GHz in a 45nm SOI CMOS process. The prototype PA achieves 40% peak PAE for 23.3 dBm P_{SAT} and 39.4% PAE for 22.4 dBm $P_{1\,dB}$ at 27 GHz in its CW performance. The 6 dB PBO PAE is 33.1% with a 1.68× improvement over a normalized Class-B PA. With only 3 control bits, the MSDPA PA supports a 12Gb/s 64-QAM signal at −24.5 dB rms EVM and average P_{out}/PAE of +15.6 dBm/27.8% without DPD.

Further, it is also shown that with the 3-bit Aux PA, the MSDPA can be reconfigured to optimize its linearity and back-off efficiency under up-to 3:1 antenna load variations (VSRW). This element-level linearization and efficiency enhancement is particularly useful for large array operations in additional to array-level DPDs [123] (Section V).

E. DOHERTY-OUTPHASING CONTINUUM PA

The possibility to independently control the inputs of dual-branch PAs, like the MSDPA above, opens for new design paradigms beyond the Doherty architecture. One of the most interesting applications is proposed in [86], where a continuum between Doherty and Outphasing operating modes is identified.

The continuum operating mode is explored to maintain high efficiency beyond an octave bandwidth in a discrete GaN implementation [87]–[89]. The principle is later generalized and expanded in an integrated 40–65 GHz mm-Wave CMOS reconfigurable PA with asymmetric power combiner and active impedance synthesis [90], [91] (Fig. 19).

Both architectures above require the drive profiles to be reconfigured for each carrier frequency, e.g., changing from a typical Doherty drive profile at one end of the band to a mixed-mode Outphasing drive profile at the other end. An inherent drawback is, therefore, that they are unable to support concurrent transmission of signals across the full bandwidth. Significant requirements are also put on the nonlinear digital signal processing required to accurately generate the desired dual-input waveforms in real-time for a linear output.

An alternative to the digitally driven architectures is to explore analog techniques for generation of the dual inputs. A single-input linear-Chireix (SILC) PA is proposed in [92]. The SILC PA employs a combination of a Doherty and Chireix Outphasing PA for simultaneous back-off efficiency enhancement and linearization. A 28 GHz SiGe HBT implementation demonstrates >20% efficiency and a raw linearity of <5% EVM for a 100 MHz OFDM signal without any DPD.

F. WIDEBAND ACTIVE LOAD MODULATION PA

To maximize the channel capacity, throughput, and frequency diversity, mm-Wave wireless standards often mandate channels with GHz bandwidth over multiple non-contiguous bands. On the other hand, there is a perennial quest for wideband PA technologies with simultaneously high efficiency (at both peak and PBO) and high linearity. Most existing wideband PAs require high-order reactive matching or distributed/balanced architectures that do not support active load modulation or PBO PAE enhancement [64], [93]–[96], necessitating new PA topologies for wideband active load modulation.

For wideband PAs, the asymmetric non-isolating power combiner topology, shown in Fig. 19, is demonstrated with reconfigurable PAs as mm-Wave power DACs [90], [91]. The combiner design seeks to realize complex conjugate matching of the two paths at the parallel combining joint for bandwidth extension. It can also achieve active load modulation for wideband PBO efficiency enhancement by reconfiguring the turning-on points and relative power gain of the PA paths based on the frequency. It can be further extended to a high-order self-similar asymmetric non-isolating power combiner structure for bandwidth and PBO efficiency enhancement.

In parallel, there have been continuous efforts to expand the bandwidth of Doherty/Doherty-like PAs and their variants. It is reported that additional output matching T-lines allows optimum reduction of the combiner impedance transformation ratio (ITR) versus PBO that achieves both bandwidth extension and passive efficiency improvement over PBO [97]–[101]. It is further shown that such multi-line Doherty network can be synthesized using two on-chip physical transformers by modeling them as synthetic T-lines or lumped impedance inverters [102], [103], see Fig. 20. An implementation in 130nm SiGe HBT shows coverage of 28, 37, and 39 GHz 5G mm-Wave bands by reconfiguring the two PA paths [102], while a recent design in 45nm CMOS SOI shows P_{sat}/OP1 dB of 28.3 dBm/26.8 dBm at 28 GHz with 18.7 dBm P_{ave} for 5G NR FR2 800 MHz 2-CC modulations [103].

Recently, a Load Modulated Balanced Amplifier (LMBA) architecture is proposed to achieve broadband active load modulation by leveraging all the four ports of a quadrature coupler [104] (Fig. 21). In the original LMBA configuration, one drives the Isolation port of the coupler by a Control PA, while keeping the Through and Couple ports driven by a pair of quadrature amplifiers, namely the Carrier PAs. It can be shown that the Control PA current will directly modulate the Carrier PA loads (Fig. 21). The LMBA can be viewed as an example of the 4-port network extension of the classic three-port Doherty architecture. Upon the invention of LMBA, there

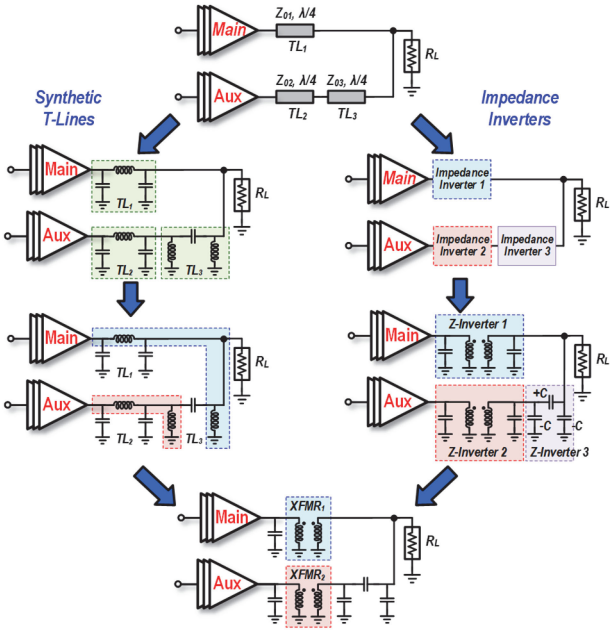

FIGURE 20. A three-line Doherty network can be synthesized using two on-chip physical transformers (XFMRs) as synthetic T-lines or lumped impedance inverters [102], [103].

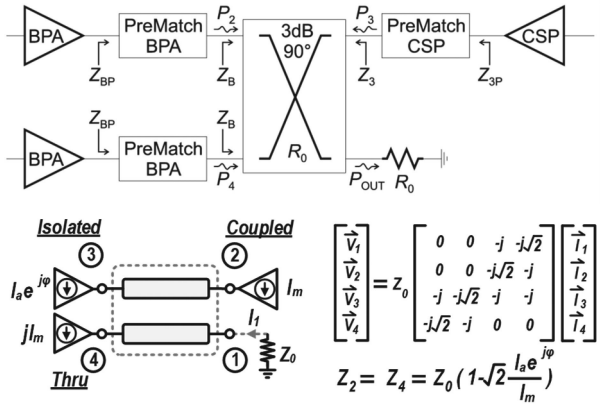

FIGURE 21. Load Modulated Balanced Amplifier (LMBA) for wideband active load modulation operation [104].

has been much follow-up research work on this topology and its derivatives. LMBA has been widely implemented in GaN technologies as hybrid modules or MMICs at RF frequencies [105]–[108] and in silicon for mm-Wave applications [109]. Additional LMBA variants include swapping Carrier and Control PAs for asymmetric Doherty-like PAs with linearity and deep PBO enhancement [110], [111].

It should also be mentioned that a new wideband active load modulation PA topology based on broadband coupler baluns is proposed in [112], as an alternative to LMBA. This PA topology inherently supports differential operation and is potentially more conducive to high mm-Wave wideband operations.

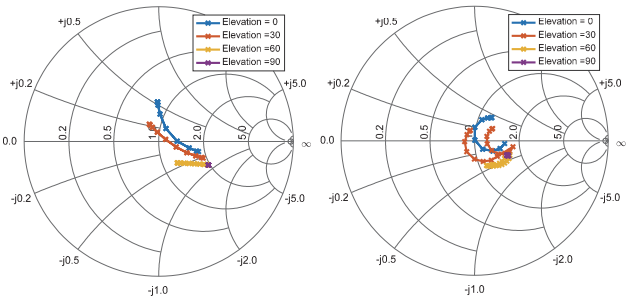

FIGURE 22. Impedance presented to a central (left) and edge (right) placed PA during scanning in a 28 GHz phased array example [124].

In addition, it is commonly believed that distributed PAs cannot provide optimum load over large bandwidth and typically suffer from low efficiency. This conventional notion however can be overcome by combining design techniques, such as nonuniform scaling, supply scaling, and extended resonances, with distributed PAs for high efficiency and wide bandwidth [113]–[116]. Further, recent work has showed that the distributed architecture can be combined with a continuum between sequential PA and Doherty PA operation to achieve wideband PBO efficiency enhancement with an arbitrary degree of load modulation [117].

V. CONSIDERATIONS IN LARGE-ARRAY APPLICATIONS

As mentioned above, mm-Wave PAs are typically utilized in phased array or hybrid beamforming systems. This allows power and signals from multiple low-power transmitters to be combined and concentrated in the direction of the users. The operation of PAs in an array environment brings new challenges that become pronounced at mm-Waves. In this section, we review fundamental efficiency and linearity considerations that PA designers have to be aware of in active antenna array applications but also some promising research directions on how these challenges can be addressed.

A. MISMATCH AND ANTENNA MUTUAL COUPLING EFFECTS

The mutual coupling between elements in an antenna array cause interaction between PAs at their outputs and introduces deviations in the load impedance present to the PA. In phased arrays, it is well known that this *active impedance* depends on scan direction, but similar effects also occur in hybrid and fully digital arrays [123]. The amount of deviation from the nominal 50Ω impedance depends on the coupling coefficients (S-parameters), the location of the element, the size of the array, and the steer direction, see Fig. 22. While isolators placed between the PA and antenna can eliminate these effects at low frequencies, cost, performance and integration requirements prevent this solution in commercial mm-Wave applications. Fig. 23 compares the inherent mismatch sensitivity of four common PA architectures in terms of linearity and average efficiency [127]. While the balanced PA, as expected, is most tolerant to mismatch it has low efficiency for modulated

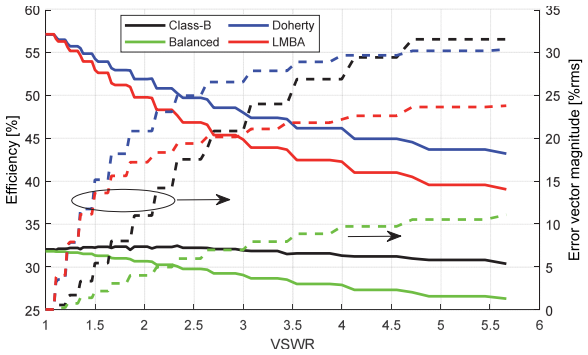

FIGURE 23. Comparison of the load mismatch sensitivity of common PA architectures in terms of average efficiency (—) and linearity (-) [127].

signals. The Doherty and load-modulated balanced amplifier (LMBA) offer improved efficiency, but both present similar mismatch vulnerability.

Understanding how these mismatch and mutual coupling effects deteriorate performance of PAs in active antenna applications is therefore of fundamental importance. A method to predict active array performance from PA model or mm-Wave loadpull data and antenna simulations is presented in [123], [124], [126]. In particular, the analysis accurately predicts the direction dependent EVM observed in phased arrays. Such nonlinear effects are relatively slow varying and may be compensated using efficient beam-oriented DPD techniques [128]. However, the complexity of DPD linearization increases significantly in the general hybrid- and multi-beam MIMO transmitter cases. This highlights the importance of mismatch resilience as an important design parameter for mm-Wave PAs.

Different PA design techniques have been proposed to alleviate the impact of load mismatch. One approach is to utilize PAs with multiple inputs, where the signals to each input are carefully designed to achieve joint back-off efficiency enhancement, mismatch compensation and frequency reconfiguration [128], [129]. Recently, a mismatch tolerant Doherty PA is constructed by alternating between series- and parallel configurations. A 39 GHz CMOS SOI prototype with 10% average efficiency at VSWR = 3:1 is reported in [130]. While these solutions assume prior knowledge about the load impedance, other works have incorporated the load sensing functionality [131], [132] in their design at RF frequencies, which can be potentially extended to mm-Wave frequencies. This results in relatively complex solutions, although a fully integrated self-adaptive CMOS solutions could be foreseen (see Section VI). Alternative solutions that combine inherent mismatch tolerance (e.g., balanced PA) and PBO efficiency enhancement is an interesting area of future research [133].

B. THERMAL CONSIDERATIONS

While the mismatch tolerance discussed above is important for linearity in active antenna arrays, typically the heat concentration due to PA inefficiency is an even greater limitation particularly in large and dense arrays. While efficiency enhancement at the PA level is of prime importance for minimizing excessive heat generation, the operation inside a dense array causes thermal effects that cannot be predicted at individual circuit level. Techniques for joint analysis and understanding of thermal-, electrical- and EM effects in active antenna array applications have been proposed in [134], [135]. With increased level of integration, and hence an expected further increase in power density, it is envisioned that such thermal effects will be of increased importance and co-design between PAs, packages and antenna array will be required. An initial step in this direction is reported in [136], where the antenna array layout is optimized by joint consideration of thermal and antenna EM characteristics, however, with assumption of idealistic PA/transmitter hardware. Bringing realistic mm-Wave PA characteristics and linearity into this analysis is expected to open for interesting directions for future PA research in terms of linearity-efficiency (power dissipation) trade-offs.

VI. FUTURE OPPORTUNITIES

The recent research and developments have substantially furthered our understandings on mm-Wave PA designs, and consequently we have witnessed a myriad of innovations at the device-, circuit topology-, and system architecture levels that have radically advanced the mm-Wave PA performance particularly with high dynamic range signals. However, there are still many unsolved challenges and multiple uncharted areas. In this section, we will give a brief summary on these topics, share our visions on research opportunities, and hopefully motivate the community to continue its explorations on mm-Wave PA designs in the future.

A. POWER, EFFICIENCY, AND BANDWIDTH LIMITING FACTORS FOR HIGH MM-WAVE FREQUENCY PAS

As operating frequencies increase towards sub-THz regimes, the goals of attaining high power and efficiency become more challenging. The limits on gain due to finite f_t and f_{max} in most cases will dictate operation in Class A and not allow sufficient harmonic content for efficiency improvement. With only small gain per stage, a useful amplifier will require many stages (more than 5 stages are common in amplifiers above 200 GHz), which will considerably degrade PAE, particularly since interstage matchings are often quite lossy. Voltage handling in high frequency transistors is limited as well, as noted above, by constraints such as Johnson Figure-of-Merit [144]. Current can be increased with increasing transistor size, but dephasing effects limit dimensions (such as gate finger width in FETs). Transistor size increases also incur impedance matching complications from reduced impedance levels, which often also limits the bandwidth and degrades the efficiency. The device capacitances also grow, and at high frequency the associated load reactance drops rapidly, making matching networks lossy and narrowband. Losses of passive components increase as a result of shrinking skin depth in the metallization (although transmission line losses actually

decrease on a per- wavelength unit basis). The use of microstrip transmission lines with substrate backside ground is increasingly limited by via inductance, and transmission lines implemented in topside metals will become more widely practiced, in III-V processes as well as silicon. To avoid losses from excitation of substrate modes, aggressive thinning of the substrate to below 50μm is necessary, requiring delicate handling and packaging. An additional yet very significant problem is the coupling of signals at amplifier inputs and outputs. Direct coupling of ICs to waveguides has been used for the highest frequencies [145]. This wide range of challenges provides ample room for future design and technology innovations.

As frequency increases, the advantages in voltage-handling and gain from III-V technologies make them increasingly valuable compared to silicon counterparts for PAs. The goal of combining these advantages with the high integration levels and rich selection of digital and analog circuits provided by Silicon has motivated many efforts to provide co-integration of multiple technologies, either in advanced packaging approaches [146] or on a single substrate. Growth of GaN on Silicon substrates is now widely practiced. Recent work has shown that CMOS-like processing can be done with GaN-on-Si to produce nitride-based ICs, followed by wafer bonding to CMOS ICs [147]. It can be anticipated that if sufficient market demand develops, heterogenous integration will become cost-effective such that PA designers can explore benefits of both CMOS and III-V technologies in their solutions.

B. LATENCY/RESPONSE-TIME AND IN-SITU SIGNAL PROCESSING AND COMPUTATION FOR MM-WAVE PAS

Future wireless links promise extremely low latency, i.e., 1ms for 5G massive machine type communication (MTC) and 1μs for 6G networks [137]–[139]. Although the majority of the latency budget is reserved for the upper software layer stacks, if the wireless links operate in highly dynamic, rapidly changing, and often unknown environments, such as drone-based communications/sensing, mm-Wave frontends at the physical layer will require constant adjustments and adaptations, including beamforming/tracking and equalizations, which will cause long latency/response-time in practice. For large-scaled arrays, the system complexity and numerous tunability render conventional LUT calibration and DPD algorithms intractable and ineffective. Therefore, element-level adaptation has become essential to address the challenges in latency/response-time and complexity. This is particularly true to mm-Wave active load modulation PAs in large arrays that, despite their load sensitivity, need to cope with significant antenna load variations (VSWR) due to antenna element couplings and beam steering [4], [124]–[126]. Note that the antenna VSWR variations depend on the location of the element, the size of the array, and the beamforming configurations including array tapering (Fig. 22), which again necessitates element-level adaptive linearization. It has been demonstrated that *in-situ* computations with AI algorithms, such as multi-armed bandit (MAB), continuum-armed bandit (CAB), contextual-bandit (CB), and actor-critic with experience replay (AC) can be utilized to rapidly compute the PA settings to achieve optimum PA linearity and peak/PBO efficiency in a real-time online fashion. An example of an AI assisted mm-wave PA Doherty is illustrated in Fig. 24, [140], [141]. AI-driven optimization on GaN Doherty PA has also been reported by Mitsubishi in [142], showing its efficacy and fast convergence.

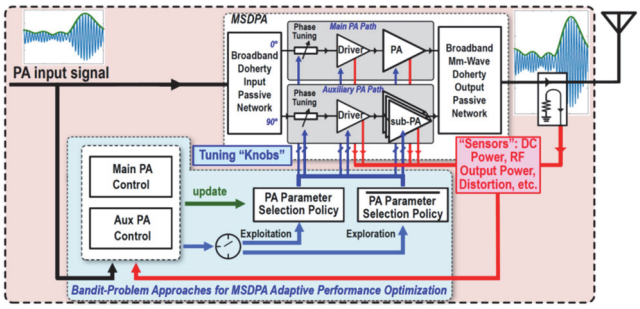

FIGURE 24. AI-assisted mm-Wave mixed-signal Doherty PA. Both inputs and the sensed outputs are sent to the control unit which runs bandit/RL-based algorithms to achieve extended linearity with high PA efficiency [141].

In the future, it is envisioned that there will an increasing level of *in-situ* computation fusion with RF/mm-Wave frontend electronics to enable rapid-response and intelligent systems for next-generation communication and sensing.

C. MM-WAVE/SUB-THZ PAS IN BEYOND-5G/6G SYSTEMS

With 5G already in the commercial deployment, there is an increasing interest in exploring beyond-5G and 6G wireless communication and sensing platforms. It is envisioned that upper mm-Wave and sub-THz frequencies (100 GHz to 240 GHz) will be the major spectrum of interest due to their abundant bandwidth and the potential to achieve the "holy grail" of 1Tb/s wireless network throughput [137]–[139]. It is also expected that very-large-scale arrays will be ubiquitously employed in these beyond-5G/6G systems. Assuming the array element size is proportional to the wavelength, a massive number of elements can be realized within a given array panel size to provide huge array gains and compensate for the high-frequency path loss [137]–[139].

However, a major challenge at the physical layer for beyond-5G and 6G networks is the lack of energy-efficient, wideband, and ultra-compact PAs in low-cost silicon technologies at high mm-Wave/sub-THz. This is even more problematic for large-scale dense arrays, where thermal management is a severe issue. Fig. 25 shows a summary of published 100–190 GHz PAs in silicon and compound processes based on the Georgia Tech PA survey [143]. Although some SiGe and GaN PAs can generate >20 dBm P_{out}, the peak PAE is generally low <14%, let alone the average PAE when amplifying high dynamic range signals. InP PAs offer remarkable energy efficiency at this frequency range. Moreover, there is little study on extending the active load modulation architectures to W-band or D-band PAs, primarily due to the lack of device power gain.

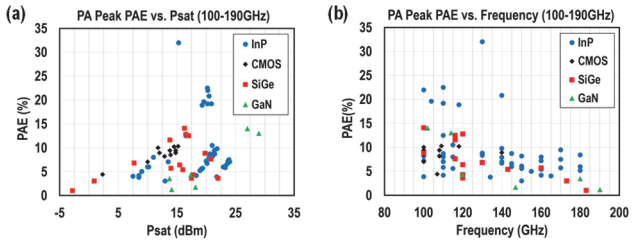

FIGURE 25. **Georgia Tech PA survey on silicon and III-V PAs at 100–190 GHz [143]. (a) PAE vs. P_{sat}. (b) PAE vs. frequency.**

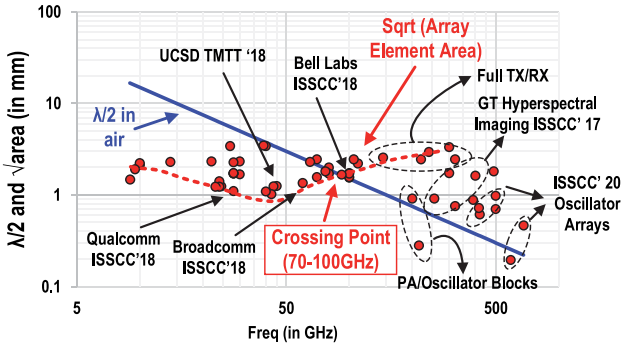

FIGURE 26. **Array element sizes vs. carrier frequencies for recently reported RF/mm-Wave phased arrays.**

Further, next-generation radar and imaging systems require a large instantaneous bandwidth (e.g., >30% at 140 GHz), while wireless links demand ultra-wideband modulations (>100Gbit/s) and high efficiency. However, most reported silicon PAs at 100 GHz and above frequencies present limited bandwidth and low efficiency [143], which deserve considerable research explorations.

In addition, to fit within the λ/2 (in the air) element lattice of a 2D array, the frontend electronics should be sized proportionally to the wavelength, which becomes increasingly challenging at high mm-Wave and sub-THz frequencies. Fig. 26 summarizes the transceiver element size of recently published arrays versus the carrier frequency. It is clear that beyond 70–100 GHz, the reported array element sizes are larger than the corresponding λ/2 element lattice, preventing their use in scalable 2D arrays. Therefore, realizing ultra-compact electronics, including the PAs, that scale with the λ/2 element lattice has now become a high research priority to enable beyond-5G/6G systems with 2D very-large-scale arrays.

VII. CONCLUSION

The rapid growing need for mm-Wave wireless links and the wide use of high dynamic range signals have created many technical challenges and innovation opportunities for next-generation mm-Wave PAs. In this review paper, we have summarized the system requirements on mm-Wave PAs that can handle large PAPR GHz modulation signals. We have reviewed various mm-Wave load modulation PA architectures and device technologies. A wide variety of example mm-Wave PAs are presented to showcase their architecture/circuit innovations and the state-of-the-art performance. We have also envisioned several future research opportunities of mm-Wave PA designs for high mm-Wave beyond-5G/6G systems and intelligent mm-Wave PAs with *in-situ* computations for rapid-response self-adaptive operations. Despite numerous technology advances, the nonstop evolution of mm-Wave wireless systems has resulted in a perpetual pursue of "perfect" PAs and continuously furthered the performance envelope of both Silicon and III-V mm-Wave PAs.

ACKNOWLEDGMENT

The authors would like to thank the students and colleagues in academia, industry, and government for their numerous insightful discussions. They would like to specifically thank Georgia-Tech Electronics and Micro-System (GEMS) lab, UCSD's Center for Wireless Communications, and GigaHertz Centre collaborators both at Chalmers University of Technology and industry. The authors would also like to thank Globalfoundries for providing fabrication support.

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