IEEE Journal of Microwaves

Received 3 November 2023; revised 21 January 2024; accepted 23 January 2024. Date of publication 12 February 2024; date of current version 9 April 2024.

Digital Object Identifier 10.1109/JMW.2024.3358627

A 28GHz, Switched-Cascode, Class E Amplifier in 22nm CMOS FDSOI Technology

NOURHAN ELSAYED [1] (Member, IEEE), SAEEDEH MAKHSUCI [2] (Member, IEEE), AND MIHAI SANDULEANU [3,4] (Senior Member, IEEE)

(Regular Paper)

[1]Global Foundries, Durham, NC 27713 USA
[2]Wayne University, Detroit, MI 48202 USA
[3]Department of Electrical Engineering, Khalifa University of Science and Technology, Abu Dhabi 127788, UAE
[4]Systems on Chip Center, Khalifa University of Science and Technology, Abu Dhabi 127788, UAE

CORRESPONDING AUTHOR: Mihai Sanduleanu (e-mail: mihai.sanduleanu@ku.ac.ae).

This work was supported by Global Foundries, USA.

ABSTRACT Using the stacking technique in CMOS technology for Power Amplifiers (PAs), allows the use of a higher supply voltage. This facilitates achieving a higher voltage swing, and delivering more output power while maintaining a high efficiency. This work presents an improved 2-stacked cascode class-E PA at 28 GHz. Unlike existing topologies, a switching input signal is not only applied at the input transistor, but also at the cascode transistor with an added delay. The design was fabricated in 22 nm FDSOI CMOS technology by GlobalFoundries that offers high performance especially at mm-wave frequencies. Measurement results of the cascode Class-E Power Amplifier achieves a peak PAE of 28%, and 41% DE. The switched-cascode topology showed an improved peak PAE of 35% and DE of 45%. Measured power gain was 8.5 dB with saturated output power (P_{sat}) of 13 dBm. This work reports the best Drain Efficiency (DE) and FoM for a fully integrated PA at 28 GHz in 22 nm FDSOI.

INDEX TERMS Class-E, FDSOI CMOS, high efficiency, power added efficiency (PAE), power amplifier (PA), millimeter-wave, stacking.

I. INTRODUCTION

The large unused available bandwidth in the mm-Waves and sub mm-Waves bands (24–100 GHz) has driven a higher demand for high data rate, high efficiency, and high integration transceiver systems that are able to deliver high output power. Intrinsically, Power Amplifiers (PAs) consume the most power in a transmitter system; their performance and design is instrumental to the overall performance and reliability of the system [1]. The challenge with designing PAs is maintaining high efficiency while delivering high output power [2]. This usually results in a design trade-off between the two. As more wideband commercial wireless communications (such as 5G and 6G), at mm-Wave frequencies, utilize Orthogonal Frequency Division Multiplexing (OFDM) to provide a more spectral efficient digital modulation. Hence the efficiency/output power capabilities trade-off becomes more critical [3]. Traditionally, III-V technologies have been the preferred choice for high power applications involving PAs [4], owing to their high-power capabilities. However, with an increased demand for higher integration, advancement in scaled CMOS technologies has allowed the advent of transistors with higher $f_T > 300$ GHz and $f_{max} > 400$ GHz. But, these technologies still suffer from a limited breakdown voltage which limits the output swing, and low gain devices which limits the Power Added Efficiency (PAE) of the PA. Moreover, the poor quality factor of the on-chip passives [5], [6], contributes further to lowering the PAE. Typically, traditional linear PAs (such as class AB), operate in the back-off region from the maximum output power [7] for being able to accommodate large Peak Average Power Ratio (PAPR) QAM/OFDM modulated signals. In back-off, the efficiency dramatically drops. Multiple techniques were used in literature to increase the output power of linear PAs. Combining multiple PA's introduces the problem of low efficiency associated with on-chip combining techniques. One of the most interesting efficiency enhancement techniques is the stacking technique. Stacking

multiple devices gives the freedom of increasing the supply voltage resulting in a larger output swing. Stacking in SOI, and FDSOI technologies has been studied extensively in [4], [5], and [8], [9], [10] as they're more power efficient. Aside from the stacking technique, there has been a growing interest towards non-linear switched mode CMOS PAs for mm-Wave applications. These PAs are usually more efficient that the linear counterparts due to their theoretically lossless operation [11]. The class-E PA has been of particular interest due to its simpler output matching network. However, challenges arise due to the lack of ideal square wave signals to drive the PA resulting in soft switching, and low PAE attributed to switching losses [5], [12]. It is also difficult to obtain ideal Class-E efficiency since the operating frequency is close to devices' f_T. However, an almost Class-E operation can still be obtained [13]. This paper discusses the application of a switched mode Class-E PA implemented in 22 nm FDSOI technology. The Class-E PA relies on switching not only the input device, but also the stacked device with a 50% duty cycle signal in order to minimize the overlap between the output voltage and current. This tweaking of the delayed phase will result in more control over the power consumption and hence the DE, and PAE. The proposed PA can be applied to QAM/OFDM signals if it is a part of a Doherty configuration as an auxiliary PA instead of the classical Class-C amplifier. Section V will conclude the paper; the rest of the paper is organized as follows: Section II will cover the stacking technique and current state of the art designs specifically related to switching PA's, followed by Section III which discusses the switched-cascode class-E PA design and architecture. Finally, Section IV will present the implementation and measurement.

II. STACKING TECHNIQUE

The stacking technique involves stacking equal size transistors where only the bottom device is driven by the input. The stacked devices turn on and off due to the swing of the intermediate nodes. The output matching network is connected to the drain of the top-most (cascode) device. In the stacking technique, the maximum AC swing becomes $\approx$ N $*$VDD where N is the number of stacked devices, VDD is the nominal supply voltage of the technology [4]. Therefore, theoretically, the output voltage swing can be N times higher for N number of stacked devices since the stress is shared similarly among the stacked devices. In consequence, we get more power and improved DE and PAE. The cascode device is a common gate device with a DC bias and AC ground; it acts as a load to increase output impedance. A small capacitor can be connected to the gate to allow some swing. In a stacked configuration, the gate of the stacked device is connected to the DC bias through a resistor and to GND through a capacitor. The stacking technique employed for RF frequencies in FDSOI and SOI devices has been studied in multiple papers. This is due to the fact that SOI technologies do not suffer from the junction breakdown voltage issues present in bulk CMOS technologies. The stacking technique in SOI technologies has been explored in linear PA designs such as in [8], [9] where, in addition to stacking, a popular efficiency enhancement architecture (Doherty PA) in 45nm SOI was employed. Stacking has also been investigated in some nonlinear switching-like PA's in [4], [14], [15]. Most of these studies focus on applying the input signal only to the bottom input transistor in a stacked topology. Applying a stacked technique in a switching PA where the switching is applied to all stacked transistors is yet to be explored more extensively. Such work was presented in [16] where 45nm SOI was used to implement a multi-output stacked Class-E amplifier at 45 GHz. Each stacked device is driven by a 50% duty cycle signal where the voltage swing is divided between the devices equally. Our work, however, employs distributed elements in the form of transmission lines instead of poor- quality passive components and introduces a new delay element in the cascode (stacked) amplifier as shown in Fig. 4 which, in turn, improves the overall efficiency. In this paper; two measures of efficiency will be used. Power Added Efficiency (PAE) and Drain Efficiency (DE).

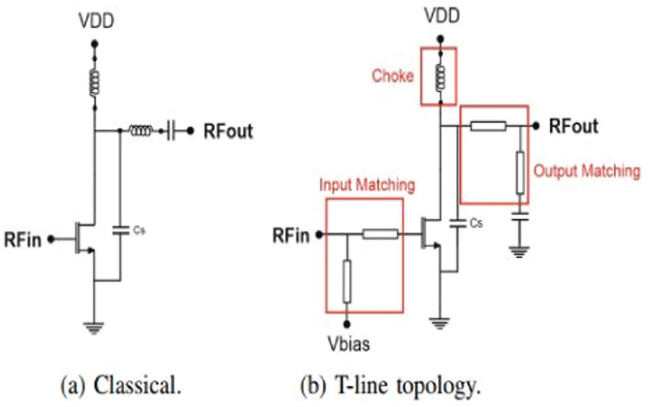

FIGURE 1. Class-E schematics.

III. POWER AMPLIFIER DESIGN AND ARCHITECTURE

A. CLASSICAL CLASS-E

The classical Class-E PA in Fig. 1 consists of three main design configurations: The input matching, output matching network needed to transform the 50 Ω load impedance to the correct impedance for Class-E operation, [17]. In an ideal class-E amplifier, the transistor acts as a switch driven with 50% duty cycle.

Traditionally, the Class-E topology uses the stray capacitance and an inductor for an output network. Transmission lines with characteristic impedance of 50Ω can be used instead of inductors, as in Fig. 1(b). One of the big disadvantages of the Class-E amplifier is that the voltage swing across the device is very large, nearly 2VDD, and hence, the stacked Class-E amplifier was explored in order to overcome this issue.

B. CASCODE CLASS-E

In the cascode Class-E topology in Fig. 2, a transistor of the same size is stacked above the input transistor. The intermediate node should be able to sustain Class-E voltage

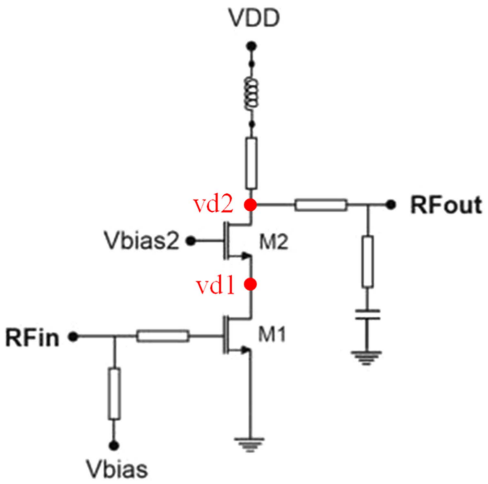

FIGURE 2. Schematic diagram of cascode class-E.

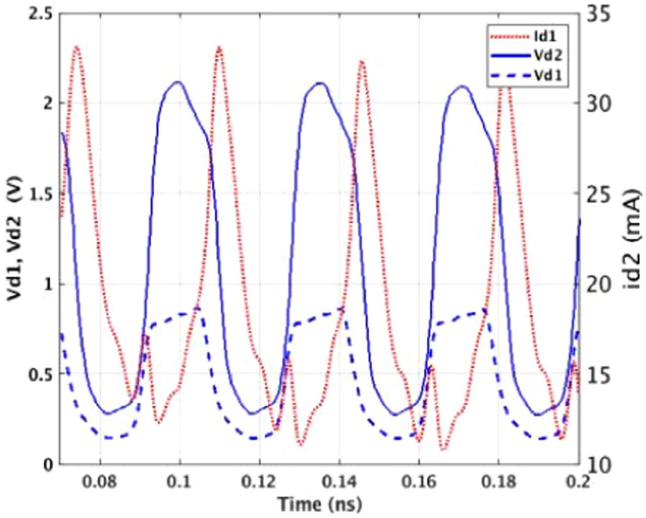

FIGURE 3. Drain current and voltage waveforms of top and bottom cascode class-E PA. The current and voltage show a non-overlapping pattern exhibiting a class-E performance. Voltage scaling is also evident from the drain voltages of the input and the stacked device.

swings. The amplitude should also be scaled in a way that the voltage is shared equally among both devices. In the 22 nm FDSOI technology, the nominal operating voltage of each device is 0.8 V. To achieve sustained device performance, the maximum swing across each transistor should never increase beyond 2xVDD. Fig. 3 shows the voltage and current swings across the cascode transistor (M2 in Fig. 2) and the voltage swing across the input transistor (M1 in Fig. 2). It can also be observed, from the waveforms, that the overlap between output voltage and current is minimal which results in a higher efficiency resembling class-E mode of operation. A tuning shunt-inductor can also be added at the intermediate node in order to improve the voltage swing to match a more ideal Class-E operation. However, this technique requires a much

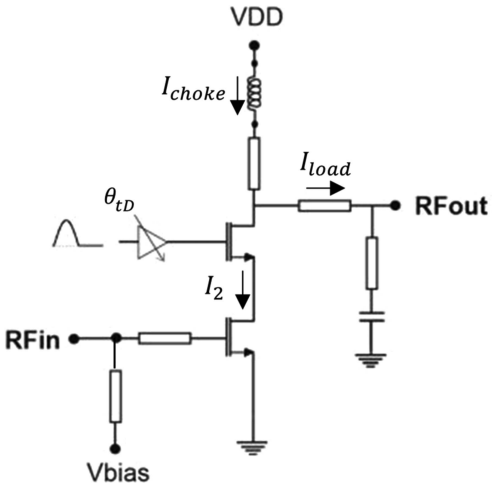

FIGURE 4. Schematic diagram of switched-cascode class-E PA. The cascode transistor has a switching input with a 50% duty cycle. The phase of the input is controlled using the delay element θ_{tD}.

bigger area (due to the inductor) which also has a limited quality factor. A series DC-blocking capacitor needs to be added, which has a poor- quality factor at mm-wave frequencies [16].

C. SWITCHED-CASCODE CLASS-E

The switched-cascode Class-E PA is based on switching not only the input transistor, but also the cascode transistor. It also includes adding a delay between the signals applied to the gates of the two transistors in such a way that varying the delay, would vary the overlap between the output voltage and current waveforms and hence vary the efficiency. The schematic of the switched cascode class-E amplifier is shown in Fig. 4. The delay element is added between the input and the cascode transistor and is varied in order to achieve a higher PAE. The cascode transistor is biased in such a way that the transistor is never fully off; hence reducing the OFF-ON switching delay. For simplistic analysis, the output and input devices are represented as lossless switches with an output capacitance of $C_{o,(12)}$ and an ON resistance of $R_{ON,(n)}$ where n denotes the nth transistor in a stack. The output capacitance $C_{o,2}$ can be represented as:

$$C_{o,2} = C_{d,2} + C_{gd,2} \tag{1}$$

where $C_{d,2}$ is the drain-to-ground capacitance of the stacked device, and $C_{gd,2}$ is the gate-to-drain capacitance of the same device. For efficiency analysis, we can define the currents through the output transistor. The load network current during the ON cycle of the transistor can be defined as:

$$I_{load} = i_2 cos\,(\omega_0 t + \theta_2 + \theta_{tD}) \tag{2}$$

Where $\theta_2$is the phase shift due to a complex load and θ_{tD} is the delay introduced by the delay element at the gate of M2.

Hence, the current through the output switch can be defined as:

$$I_2 = I_{choke} - I_{load} \tag{3}$$

TABLE 1 Comparison With State of the Art

Ref.	Technology	Freq. (GHz)	Psat (dBm)	(%)	Peak PAE (%)	Gain (dB)	FoM	Class of Operation
This work	22nm FDSOI	28	13	41	28	8.5	13.5	Class-E, Cascode
This work	22nm FDSOI	28	13	45	35	8.5	14.5	Class-E, Switched cascode
[16]	45nm SOI	47.5	19.1	24.5	16	8.2	10.6	Class-E, 2-stacked
[5]	45nm SOI	47	17.6	42.4	34.6	13	13.85	Class-E, 2-stacked
[5]	45nm SOI	47.5	20.3	23	19.4	12.8	13.46	Class-E, 4-stacked
[19]	CMOS 40nm	2.5	17.5	54	34	N/A	N/A	Class-E, Doherty
[15]	45nm SOI	45	18.6	N/A	34	9.5	10.9	Class-AB, 2-stacked
[20]	0.13 um SiGe	41	23.6	N/A	31	12.5	N/A	Class-E, 2-stacked
[13]	32nm SOI	60	12.5	N/A	30	10	N/A	Class-E

Where I_{choke} is the current through the choke inductor. The power loss through the switch can then be defined as:

$$P_{loss} = I_{RMS,2}^2 * 2R_{ON} \tag{4}$$

Where R_{ON} is the output switch ON-resistance assuming both devices are of identical size. From (3) and (4) we can define DE as:

$$DE = 1 - \frac{P_{loss}}{P_{DC}} = 1 - \frac{I_{choke} - i_2 * \cos(w_0 t + \theta_2 + \theta_{tD}) * 2R_{ON}}{V_{DD} * I_{DC}} \tag{5}$$

From (5) it may seem that by minimizing the ON resistance and increasing the device size, DE will increase. However, if the device gets too large, the input drive will need to increase which will have a negative effect on the PAE. Therefore, the device size needs to be chosen to provide a trade-off between the PAE, and DE. This way, a new term (θ_{tD}) is introduced to provide more control to achieve the best efficiency for the PA. θ_{tD} is introduced through a tunable transmission line connected to the gate of the cascode transistor. The transmission lines has been configured in a 4-2-1 structure which allows binary weighted control of the phase. Fig. 5 shows the drain and current waveforms of the PA, with varying (θ_{tD}). From Fig. 5, the overlap between the drain current and voltage varies with the varying time delay; hence, one can achieve maximum PAE by adjusting the delay to result in minimum overlap and PAE as depicted in Fig. 6.

IV. MEASUREMENT RESULTS

The implemented PA in Fig. 7 was designed and fabricated in 22nm FDSOI by GlobalFoundries and was tested using on-chip probing using the Elite 300 semi-automatic probe station. The setup was calibrated up to the probe tips using the Rhode & Schwarz ZVB8 Vector Network Analyzer (VNA). The input signals were generated using the Rhode & Schwarz SMF 100A Signal Generator.

A. SMALL SIGNAL MEASUREMENTS

The small signal measurements were done using a VNA. Figs. 8, 9 and 10 depict the measured and simulated small signal S-parameters of the cascode Class-E PA. In measurement, a peak gain of 13 dB was achieved at $\approx$ 28 GHz. A frequency shift of $\approx$ 1 GHz (3%) was observed in both S11 AND S22 due to mismatch in the modeling of some device intrinsic capacitances and inductances.

B. LARGE-SIGNAL MEASUREMENTS

Two sets of measurements were performed for the large signal measurements using a Spectrum Analyzer from Rhode & Schwarz. The first one was for the cascode Class-E PA; achieving a peak PAE of 28% and 41% DE. Fig. 11 shows the measurement versus simulation results. The switched-cascode topology achieved better efficiency since the DC power dissipated is reduced; resulting in a peak PAE of 35% and DE of 45% in Fig. 12. Different delay (θ_{tD}) values were applied and PAE was observed. The optimum delay applied was 4 ps compared to 4.5 ps in simulation. The output power and power gain of the PAs shown in Fig. 13 remains the same and show a gain of 8.5 dB.

C. COMPARISON WITH STATE-OF-THE-ART

Table 1 shows the comparison of both the cascode and switched-cascode Class-E PA to existing state of the art mm-Wave PAs. To our knowledge, the best PAE efficiency reported for a Class-E at mm-wave frequency was reported in [5] implemented in 45 nm SOI at 47 GHz. For a fair comparison, a Figure of Merit (FOM) was introduced by [16] that includes the main performance metrics and the limitations of a PA including the saturated power (P_{sat}), the gain, the PAE, and the ratio of the operating frequency f_0 compared to the f_{max} of the technology. Defined as:

$$FOM = P_{sat}\,(dBm) + Gain\,(dB)$$

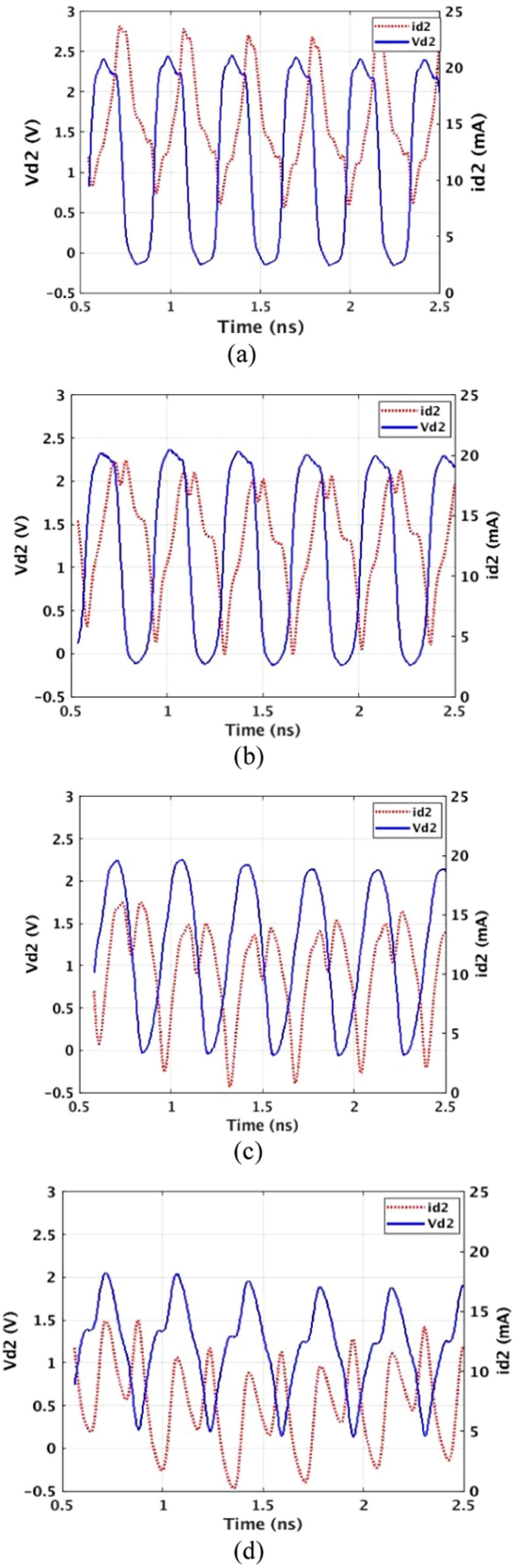

FIGURE 5. Drain current and voltage waveforms with varying θ_{tD} (a) θ_{tD}= 0, (b) θ_{tD}= 4.5ps, (c) θ_{tD}= 9ps, (d) θ_{tD}= 13.5ps. The change in the overlap between the two signals affects the PAE of the PA.

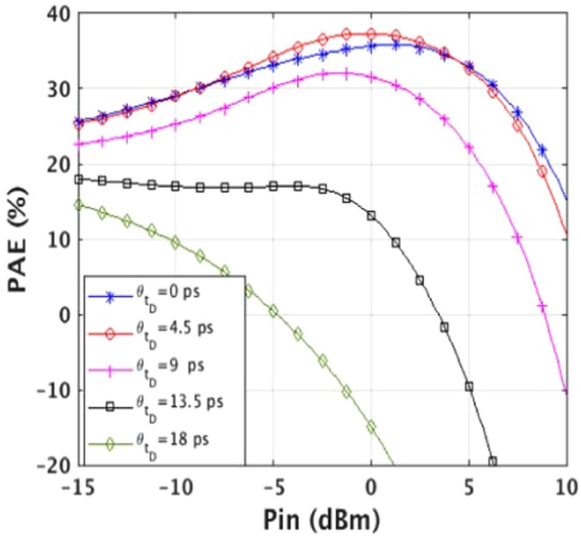

FIGURE 6. Varying PAE with varying θ_{tD}. Changing the phase of the cascode transistor input affects the PAE of the PA. Maximum efficiency was achieved without affecting the output power.

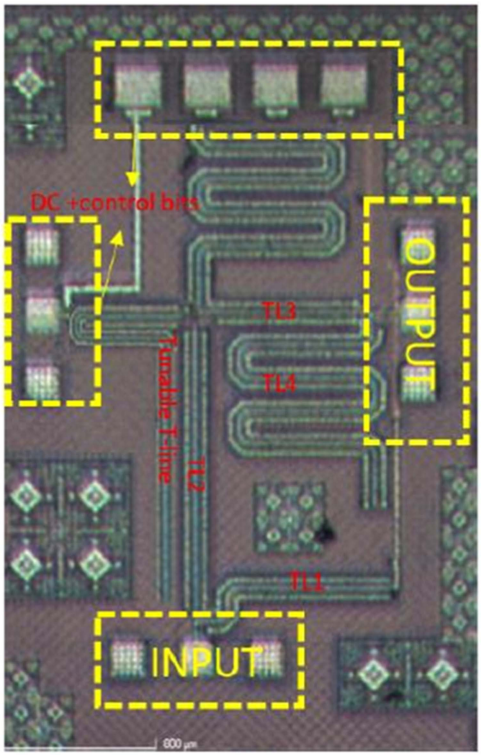

FIGURE 7. 22 nm FDSOI chip microphotograph. Total die size is 0.6 × 1 mm.

$$+ 10 \cdot log_{10}(PAE) + 20 \cdot log_{10}\left(\frac{f_0}{f_{max}}\right) \qquad (6)$$

This FOM is a modification from a previous FOM mentioned in [5] which only accounts for the operating frequency irrespective of the fmax of the device. From Table 1 we are able to report the best drain efficiency and overall performance for a fully integrated PA at 28GHz along with the best FOM

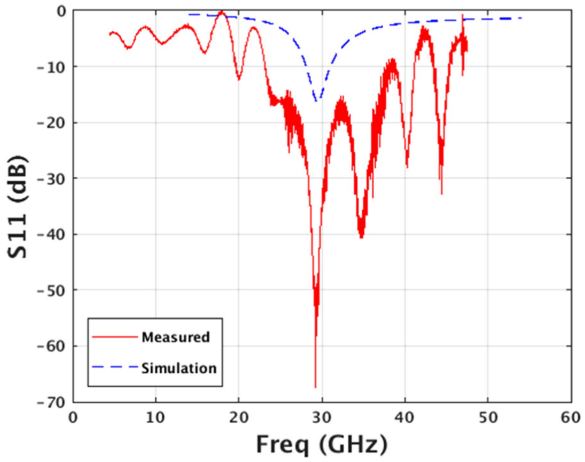

FIGURE 8. Simulated vs measured *S*11. The measured input matching achieves<−40 dB at 28 GHz.

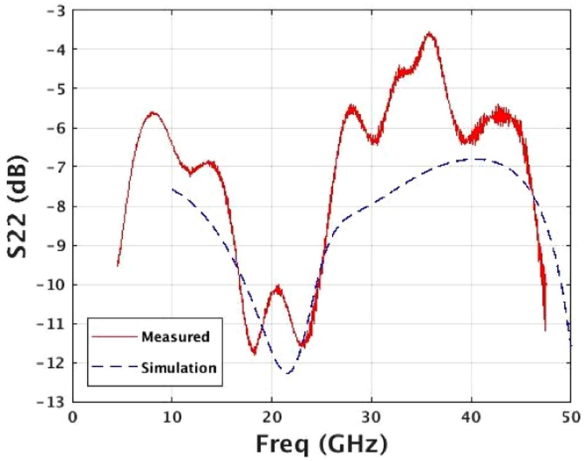

FIGURE 9. Simulated vs measured *S*22. The measured output matching is −10dB at 28 GHz.

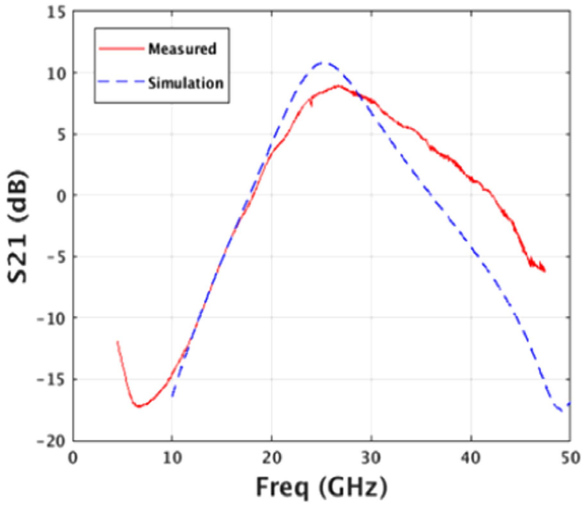

FIGURE 10. Simulated vs measured S_{21}. The measured S_{21} is 8.5 dB with ≈ 1 GHz frequency shift from the simulation.

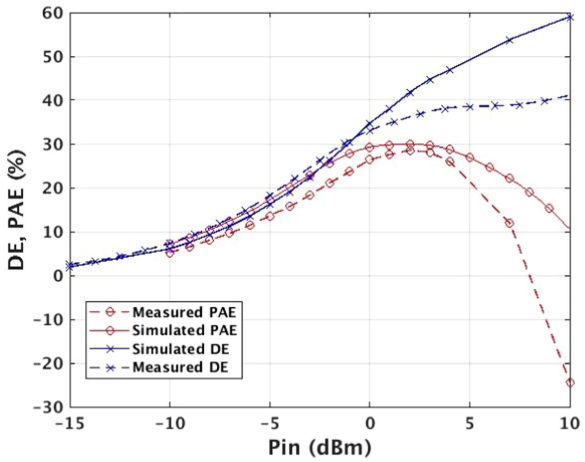

FIGURE 11. Measured and simulated PAE and DE for cascode class-E PA vs input power for cascode class-E PA. The maximum DE/PAE for the PA is 41/28%. Peak PAE is achieved at pin = 2 dBm.

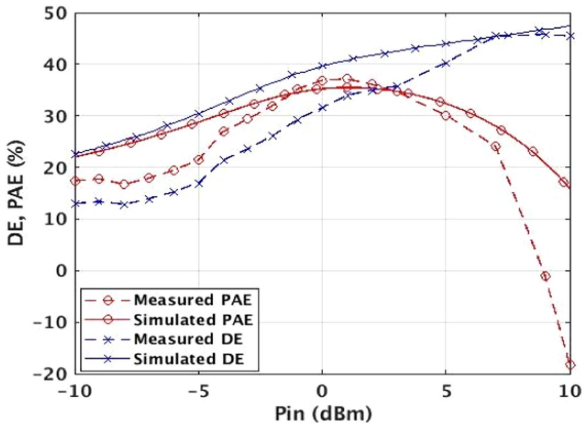

FIGURE 12. Measured and simulated PAE, and DE of switched cascode class-E PA. The maximum measured DE/PAE is 45/35%. Peak PAE is achieved at Pin = 1 dBm.

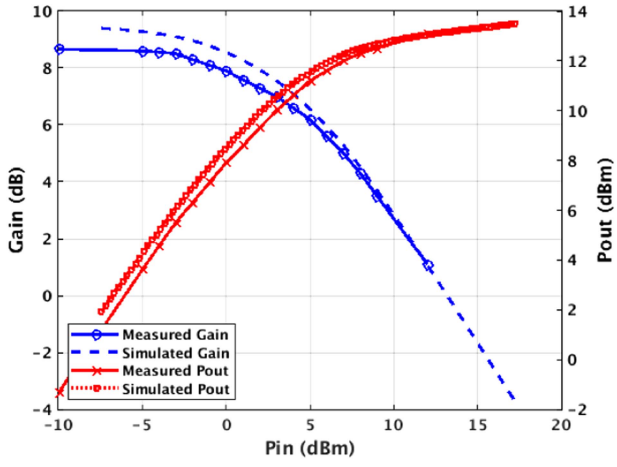

FIGURE 13. Gain vs output power for cascode class-E PA. Measured gain in 8.5 dB with a saturated output power Psat of 13 dBm.

defined in (6). For 22nm FDSOI NMOS transistor the reported fT/fmax is 347/371GHz [18].

V. CONCLUSION

This paper has presented the novel design and measurement of two cascode based Class-E PA's in 22nm FDSOI CMOS by GlobalFoundries. The first one is based on cascode topology achieving a peak PAE of 28%. The second one is based on a switched-cascode topology to achieve minimum overlap between the current and voltage waveforms at the drain of the output device. The switched cascode Class-E PA achieves a PAE of 35% and a peak DE of 45% with a saturated output power of 13 dBm. We achieved the highest FOM for switched cascode operation compared to similar PAs in the literature.

REFERENCES

[1] J. Joung, C. K. Ho, K. Adachi, and S. Sun, "A survey on power-amplifier-centric techniques for spectrum- and energy-efficient wireless communications," *IEEE Commun. Surveys Tuts.*, vol. 17, no. 1, pp. 315–333, Firstquarter 2015.

[2] P. M. Asbeck, "Will Doherty continue to rule for 5G?," in *Proc. IEEE Microw. Theory Techn. Soc. Int. Microw. Symp.*, 2016, pp. 1–4.

[3] D. Y. C. Lie, J. C. Mayeda, and J. Lopez, "A short survey on recent highly efficient cm-Wave 5G linear power amplifier design," in *Proc. IEEE 60th Int. Midwest Symp. Circuits Syst.*, 2017, pp. 13–16.

[4] A. Chakrabarti and H. Krishnaswamy, "High-power high-efficiency class-E-like stacked mm-wave PAs in SOI and bulk CMOS: Theory and implementation," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 8, pp. 1686–1704, Aug. 2014.

[5] A. Chakrabarti and H. Krishnaswamy, "High power, high efficiency stacked mm-wave class-E-like power amplifiers in 45nm SOI CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2012, pp. 1–4.

[6] K. Datta, J. Roderick, and H. Hashemi, "A triple-stacked class-E mm-wave SiGe HBT power amplifier," in *Proc. IEEE Microw. Theory Techn. Soc. Int. Microw. Symp.*, 2013, pp. 1–3.

[7] Q. Liu, V. Adrian, B.-H. Gwee, and J. S. Chang, "A class-E RF power amplifier with a novel matching network for high-efficiency dynamic load modulation," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2017, pp. 1–4.

[8] A. Agah, B. Hanafi, H. Dabag, P. Asbeck, L. Larson, and J. Buckwalter, "A 45GHz Doherty power amplifier with 23% PAE and 18dBm output power, in 45nm SOI CMOS," in *Proc. IEEE/MTT-S Int. Microw. Symp.*, 2012, pp. 1–3.

[9] A. Agah, H.-T. Dabag, B. Hanafi, P. M. Asbeck, J. F. Buckwalter, and L. E. Larson, "Active mm-wave phase-shift Doherty power amplifier in 45-nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2338–2350, Oct. 2013.

[10] C. S. Levy, V. Vorapipat, and J. F. Buckwalter, "A 14 GHz, 22-dBm series Doherty power amplifier in 45nm CMOS SOI," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2016, pp. 1–4.

[11] A. Chakrabarti and H. Krishnaswamy, "Design considerations for stacked class-E-like mm-wave high-speed power DACs in CMOS," in *Proc. IEEE Microw. Theory Techn. Soc. Int. Microw. Symp.*, 2013, pp. 1–4.

[12] O. El-Aassar, M. El-Nozahi, and H. F. Ragai, "Loss mechanisms and optimum design methodology for efficient mm-waves class-E PAs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 6, pp. 773–784, Jun. 2016.

[13] O. T. Ogunnika and A. Valdes-Garcia, "A 60GHz class-E tuned power amplifier with PAE >25 in 32nm SOI CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2012, pp. 65–68.

[14] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, "A 33-dBm 1.9-GHz silicon-on insulator CMOS stacked-FET power amplifier," in *Proc. IEEE Microw. Theory Techn. Soc. Int. Microw. Symp.*, 2009, pp. 533–536.

[15] A. Agah, H. Dabag, B. Hanafi, P. Asbeck, L. Larson, and J. Buckwalter, "A 34 % PAE, 18.6dBm 42–45GHz stacked power amplifier in 45nm SOI CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2012, pp. 57–60.

[16] A. Chakrabarti and H. Krishnaswamy, "Multi-output stacked class-E mm-wave power amplifiers in 45 nm silicon-on-insulator metal–oxide–semiconductor: Theory and implementation," *Inst. Eng. Technol. Microw., Antennas Propag.*, vol. 9, no. 13, pp. 1425–1435, 2015.

[17] Z. Xu and E. El-Masry, "Design and optimization of CMOS class-E power amplifier," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. I, Jun. 2003, pp. 325–328.

[18] J. Hoentschel, L. Pirro, R. Carter, and M. Horstmann, "22FDSOI technologies for ultra-low power IoT, RF and mm-wave applications," *Composants Nanoelectroniques*, vol. 2, pp. 35–42, Jan. 2019.

[19] M. Hashemi, L. Zhou, Y. Shen, and L. C. N. de Vreede, "A highly linear wideband polar class-E CMOS digital Doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 10, pp. 4232–4245, Oct. 2019.

[20] K. Datta, J. Roderick, and H. Hashemi, "Analysis, design and implementation of Mm-wave SiGe stacked class-E power amplifiers," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, 2013, pp. 275–278.

NOURHAN ELSAYED (Member, IEEE) received the B.Sc. degree in electrical and electronics engineering from Khalifa University, Abu Dhabi, UAE, in 2014, and the MSc. degree in electrical engineering from The Petroleum Institute, Abu Dhabi, UAE, in 2016. She is currently with Global Foundries (GF), North Carolina, USA. His research interests include RF circuit design specifically high efficiency transmitter design for 5G applications. She has been working on multiple mm-wave designs from the simulation to the layout, and measurement phase.

SAEEDEH MAKHSUCI (Member, IEEE) received the B.Sc. degree majoring in electrical engineering from Razi University, Kermanshah, Iran, in 2014, and the M.Sc. degree in electrical engineering from the K. N. Toosi University of Technology, Tehran, Iran, in 2018, with the focus on "power amplifier, and Built-in self-test (BIST)". Since 2019, she has been working toward the Ph.D. degree with Wayne State University, Detroit, MI, USA. Her research interests include high-efficiency RF power amplifiers and doherty power amplifier for 5G applications.

MIHAI SANDULEANU (Senior Member, IEEE) was born in Vatra Dornei, Romania, in 1966. He received the M.Sc. and M.E.E. degrees in electronics from the University of Gh. Asachi, Iasi, Romania, and Eindhoven University of Technology, Eindhoven, The Netherlands, in 1990 and 1995, respectively, and the Ph.D. degree in electronics from the University of Twente, Enschede, The Netherlands, in 1999. From 1999 to 2001, he was with Philips Semiconductors Nijmegen, The Netherlands. From 2001 to 2007, he was with Philips Research Eindhoven, The Netherlands. While with Philips Research, he was an Adjunct Professor with the Microelectronics Group, Eindhoven University of Technology. In 2008, he spent six months with Inter-university Microelectronics Center (IMEC), Leuven, Belgium, conducting research on 60GHz transceiver design and THz electronics. From 2008 to 2013, he conducted research with the IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, in mm-wave transceivers for communication, imaging and radar, high-speed analog-to-digital converters for wired/wireless communication systems and ultra-low power radios. He is currently an Associate Professor with the Masdar Institute of Science and Technology. His research interests include wireless transceiver design for RF/mm-waves/THz communication, THz electronics, high speed communication circuits for serial input and output, high speed analog-to-digital converters, phased-array systems, imaging, fiber optic interface IC, ultra-low power radios, data and clock recovery and phase locked loop (PLL), and high accuracy/low power analog/mixed-signal circuits and systems, system on chip (SoC) design. He was an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS and *Analog and Signal Processing Journal*. Dr. Sanduleanu is also the Chairman of IEEE Microwave Theory and Techniques Society, UAE Chapter.