A D-Band Frequency-Doubling Traveling-Wave Amplifier Through Monolithic Integration of a SiC SIW and GaN HEMTs

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ABSTRACT We report a solid-state traveling-wave amplifier (TWA) realized through monolithic integration of transistors with a SiC substrate-integrated waveguide (SIW). The TWA uses a stepped-impedance microstrip line as the input divider, but a low-loss, high-power-capacity SIW as the output combiner. The input signal is distributed to four GaN high-electron mobility transistors (HEMTs) evenly in magnitude but with 90° successive phase delays at the fundamental frequency. The HEMTs are distributed in the SIW in a period of a half wavelength at the second harmonic frequency, so that their outputs are combined coherently at the SIW output. To overcome the limited speed of the HEMTs, they are driven nonlinearly to generate second harmonics, and their fundamental outputs are suppressed with the SIW acting as a high-pass filter. The measured characteristics of the TWA agree with that simulated at the small-signal level, but exceeds that simulated at the large-signal level. For example, under an input of 15 dBm at 70 GHz, the output at 140 GHz is 38-dB above that at 70 GHz. Under an input around 70 GHz and 20 dBm, the output around 140 GHz is 14 dBm with a 3-dB bandwidth of 6%. This is not only the first D-band frequency multiplier based on the GaN HEMT technology, but also one with the highest output power and the lowest fundamental leakage among all D-band multipliers of different transistor technologies. This proof-of-principle demonstration opens the path to improve the power, gain and efficiency of sub-terahertz TWAs with higher-performance transistors and drive circuits. Although the demonstration is through monolithic integration, the approach is applicable to heterogeneous integration with the SIW and transistors fabricated on separate chips.

INDEX TERMS Frequency multipliers, millimeter wave, MMICs, power combiners, substrate integrated waveguides, traveling wave amplifiers.

I. INTRODUCTION

With the operating frequencies of 6G wireless communications and next-generation automotive radars extending above 110 GHz, D-band (110–170 GHz) high-power transmitters are needed [1], [2], [3]. However, conventional microwave monolithic integrated circuits (MMICs) based on coplanar or microstrip transmission lines suffer from high loss, significant crosstalk, and limited power capacity above 110 GHz. For example, the output power of D-band MMICs is presently limited to the order of 20 dBm by not only the speed of transistors, but also the loss of power combiners [4]. In particular, the loss of conventional power combiners increases significantly with the number of interconnected transistors, resulting in diminishing return for combining more transistors. By contrast, substrate-integrated waveguides (SIWs) [5] have low loss, minimum crosstalk, and high power capacity.

However, because the size of an SIW is on the order of the guided wavelength λ_{SIW} in the SIW, SIWs are usually implemented at the board level as interconnects and transitions [6], filters [7], [8], antennas [9], or power combiners [10] for hybrid integration with transistors.

SIW-based monolithic integration becomes feasible when the frequency exceeds 110 GHz, so that $\lambda_{SIW} < 1$ mm in typical semiconductors as Si, GaAs, GaN and SiC. This paper reports monolithic integration of an SIW power combiner with transistors, which can lead to D-band power amplifiers with higher power and efficiency. The SIW-based power amplifier can in turn be monolithically integrated with SIW-based filters and antennas [11] to realize a single-chip RF front end. Note that SIW antennas have been monolithically integrated on SiGe transceivers [12], [13].

At the board level, SIW power combiners have been demonstrated in corporate, series, radial, Wilkinson, and Gysel structures [14]. However, these structures when scaled to the D band are too large for monolithic integration. Therefore, we propose a traveling-wave power combiner by embedding transistors in an SIW as illustrated in Fig. 1(a). It can be seen that the propagating wave in the SIW is bounded by two rows of through-substrate vias (TSVs) interconnecting the top and bottom ground planes. Embedded along the middle of the SIW are four "hot" (isolated from the top and bottom ground planes) TSVs separated by $\lambda_{SIW}/2$ from each other. Each hot TSV, when driven by a transistor, can act as an antenna to radiate into the SIW with their radiations coherently combined at the right end of the SIW. The left end of the SIW is shorted by another row of grounded TSVs $\lambda_{SIW}/4$ from the nearest hot TSV, so that the backscattered wave is reflected and adds constructively to the forward propagating wave.

For a D-band SIW traveling-wave power combiner of 50-μm-thick SiC and Au metallization, Fig. 1(b) shows the HFSS-simulated power-combining loss is 0.7 dB (88% efficiency), which is significantly better than D-band on-chip power combiners based on coplanar or microstrip transmission lines [15], [16], [17]. In an ideal 4:1 combiner, each branch should contribute 1/4 (-6 dB) of the output power. The simulation shows the actual contribution is -6.7 dB around the center frequency of 140 GHz. The efficiency of the SIW power combiner can be further improved because it is presently limited by metal loss instead of dielectric or radiation loss [18], [19].

For high-power GaN-on-SiC MMICs, SIWs are especially attractive because transistors can be monolithically integrated on a SiC SIW without additional process complexity. SiC is an excellent SIW material which offers high dielectric constant for compact size, high electrical resistivity and low loss tangent for low loss, high breakdown strength for high power capacity, strong mechanical toughness for robust fabrication, and high thermal conductivity for heat dissipation [20].

Despite the relatively high power capacity of GaN HEMTs, their speed is limited. To overcome the speed limit of GaN HEMTs, they can be driven nonlinearly to generate harmonics at higher frequencies. For example, GaN frequency doublers
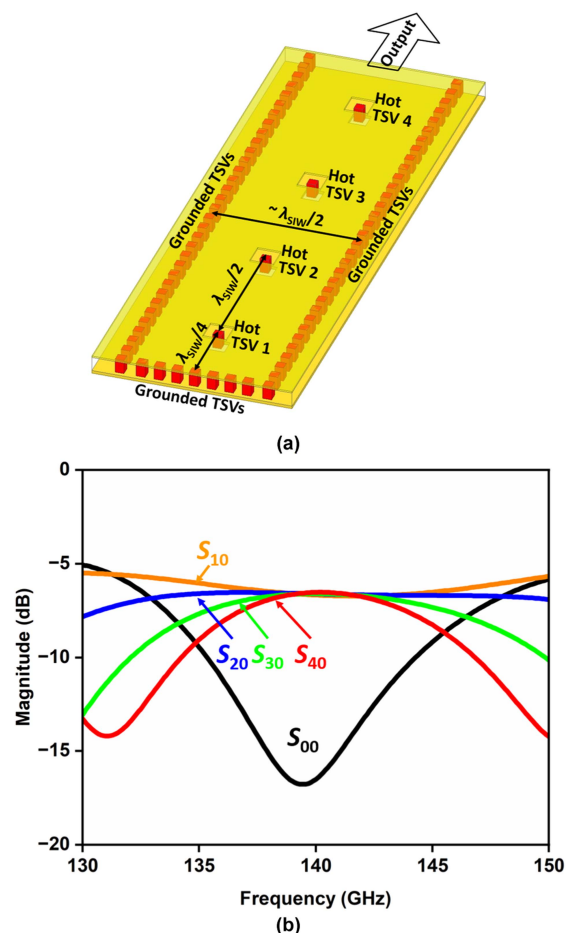

FIGURE 1. (a) Schematics and (b) simulated scattering parameters of the proposed SIW power combiner. The four hot TSVs are designated as port 1, 2, 3 and 4, while the output port is designated as port 0.

have been demonstrated at 77 GHz with 5-dB conversion loss and 10-dBm output power [21], and at 100 GHz with 4-dB conversion gain and 14-dBm output power [22]. A frequency-multiplying power amplifier can lessen the demand on the transistor cutoff frequency as well as the baseband frequency.

To demonstrate the novel frequency-doubling power-combining concept, the present traveling-wave amplifier (TWA) is designed with the input divider made of a microstrip line but the output combiner made of an SIW. Besides being low loss with high power capacity, SIW is intrinsically a high-pass filter to suppress the fundamental leakage. The $\lambda_{SIW}/4$ short at the second harmonic frequency on the left end of the SIW also helps suppress odd harmonics. Based on these innovations, we have reported the first D-band frequency doubler based on GaN HEMTs which is also the first SIW-based MMIC power amplifier [23]. This paper expands [23] mainly in design details.

II. DESIGN

The present TWA is designed for fabrication in HRL's T3 40-nm GaN-on-SiC HEMT technology with cutoff frequen-
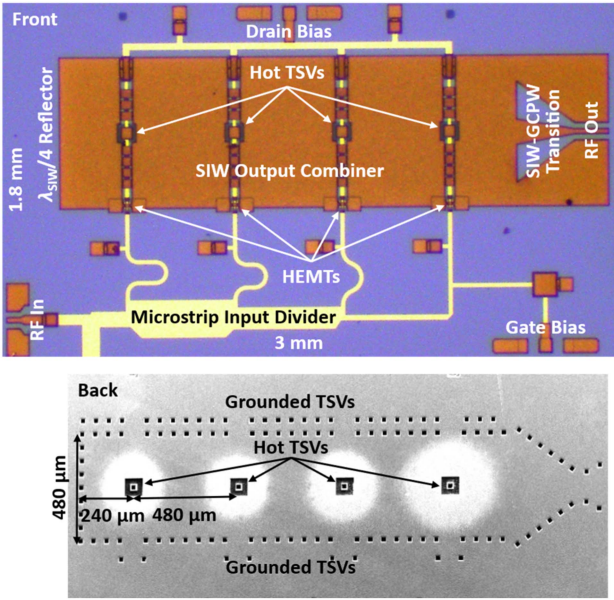
FIGURE 2. (Top) front and (bottom) back micrographs of a TWA chip.

FIGURE 3. Simulated electric field of the SIW power combiner.

cies $f_T \sim 200$ GHz and $f_{MAX} \sim 400$ GHz [24]. The SiC substrate is 50-μm thick.

Analytical equations for dielectric-loaded waveguides can be used to design an SIW by using an effective width w_{EFF} for a cutoff frequency f_{TE10} [25]

$$w_{EFF} = \frac{c}{2f_{TE10}\sqrt{\varepsilon_\parallel}}, \tag{1}$$

where c is the speed of light and $\varepsilon_\parallel$ is the relative permittivity perpendicular to the substrate. In the case of c-axis 4H-SiC, we have experimentally determined that $\varepsilon_\parallel = 10.2 \pm 0.1$ [18], [19], so $w_{EFF} = 467$ μm for $f_{TE10} = 100$ GHz. The actual width w of the SIW can then be calculated by solving [26]

$$w_{EFF} = w - 1.08\frac{d^2}{s} + 0.1\frac{d^2}{w}, \tag{2}$$

where $d = 30$ μm is the TSV diameter and $s = 60$ μm is the TSV spacing center-to-center. Thus, $w = 483$ μm.

From $\varepsilon_\parallel$, λ_{SIW} can be calculated by [25]

$$\lambda_{SIW} = \frac{\lambda_0}{\sqrt{\varepsilon_\parallel \left(1 - f_{TE10}^2/f^2\right)}}, \tag{3}$$

where λ_0 is the free-space wavelength and f is the frequency. At the center of the D band, $f = 140$ GHz and $\lambda_{SIW} = 954$ μm.

Fig. 2 illustrates the 3 mm × 1.8 mm TWA chip. It can be seen that the right end of the SIW is transitioned to a grounded coplanar waveguide (GCPW) to facilitate wafer probing [11]. The input signal is distributed through a microstrip line to each HEMT evenly in magnitude but with 90° successive phase delays at the input frequency $f_{IN} = 70$ GHz. Limited to two metal interconnect layers, GCPW lines are laid out in the first metal layer to connect each hot TSV to a HEMT and a common drain bias V_{DD}. The drain bias line is shunted
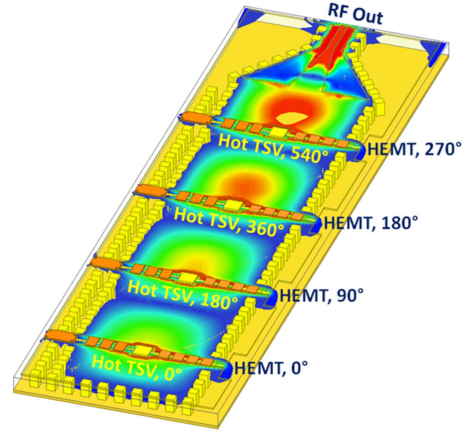
after $\lambda_{GCPW}/4$ by a metal-insulator-metal (MIM) capacitor to prevent RF leakage, where λ_{GCPW} is the wavelength in the GCPW line. Airbridges are designed in the second metal layer to connect the top ground plane of the SIW across the GCPW line. HFSS simulation confirms that the airbridges have little effects on the SIW characteristics. The simulation also confirms that as the wave propagates towards the RF output, its electric field progressively increases (Fig. 3).

The input and output impedances of each 2×25 μm HEMT are optimized through source- and load-pull simulations using HRL's HEMT model in ADS. Under a class-C gate bias of $V_{GG} = -1$ V, a drain bias of $V_{DD} = 12$ V, and an input power $P_{IN} = 10$ dBm at 70 GHz and $(12 + j80)$ Ω, each HEMT can supply an output power $P_{OUT} = 6.4$ dBm at 140 GHz to a hot TSV with an optimum load impedance $Z_{OPT} = (25 + j60)$ Ω. The load impedance presented by each hot TSV is adjusted by tuning its gaps with the top and bottom ground planes, as well as the length (250 μm) and characteristic impedance (22 Ω) of the GCPW line connecting each HEMT to its respective hot TSV.

Fig. 2 also illustrates the input divider consisting of a stepped main line and four delay lines branching out from the main line to each HEMT. The input of the divider is designed to match the optimum source impedance while the outputs of the divider provide even magnitudes with successive phase delays to the HEMTs. Broadband phase synchronization between the microstrip divider and the SIW combiner is challenging because quasi-transverse-electromagnetic (TEM) waves travel in the microstrip line whereas transverse-electric (TE) waves travel in the SIW, the latter being more dispersive [25]. Nevertheless, the SIW and the microstrip line can be designed to ensure phase synchronization for both 70-GHz quasi-TEM waves in the microstrip line and 140-GHz TE waves in the SIW as shown in Fig. 4 and detailed below.

The design of the divider starts with the width of the gate feed of each HEMT, which is fixed at 20 μm by the foundry. Therefore, the gate feed is connected to the divider through a
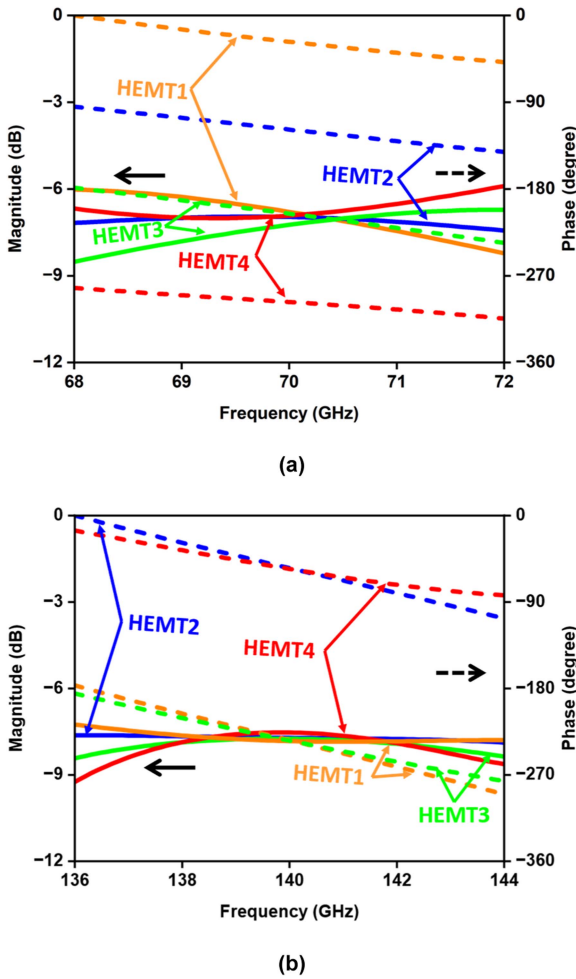
FIGURE 4. HFSS-simulated magnitudes and delays (a) from the input of the input divider to the input of each HEMT (dash) and (b) from the output of each HEMT to the output of the output combiner (solid).

TABLE 1. Different Sections of the Input Divider

From	To	Z_0 (Ω)	Width (μm)	θ (°)	Length (μm)
MIM0	Shunt Line	50	70	21	150
Shunt Line	Open	38	80	31	150
Shunt Line	Branch1	41	70	39	150
Branch1	Branch2	24	170	111	470
Branch2	Branch3	34	100	107	480
Branch3	Branch4	66	25	96	470
Branch1	MIM1	72	20	118	512
Branch2	MIM2	72	20	92	425
Branch3	MIM3	72	20	78	380
Branch4	MIM4	72	20	68	300
MIM1,2,3,4	HEMT1,2,3,4	72	20	33	150
HEMT1,2,3,4	TSV1,2,3,4	22	18[a]	90	250

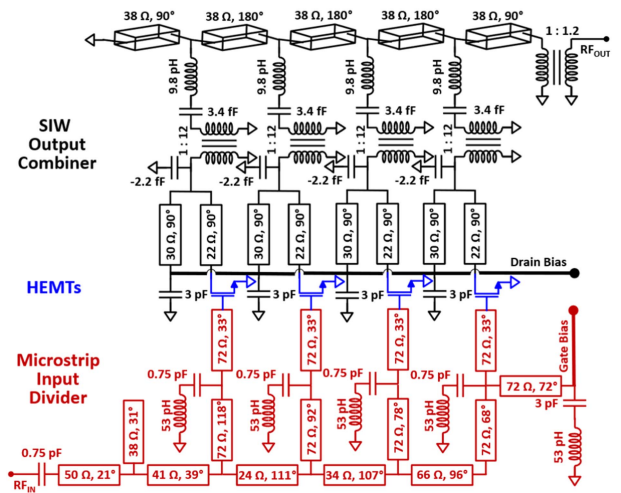[a] GCPW with a 12-μm gap ground-center conductor.

FIGURE 5. Equivalent circuit of the TWA.

The phase difference at each HEMT is then optimized by the lengths of the 72-Ω branch lines. Together with the delays along the main line, the total phase differences at HEMT1, HEMT2, HEMT3, and HEMT4 are 0°, 90°, 180° and 270°, respectively. Because discontinuities in the main line introduce additional phase changes, HFSS simulation is used for the optimization.

At the input to the divider, a 70-μm-wide, 150-μm-long series line, together with an 80-μm-wide, 150-μm-long shunt line and a 0.75-pF series capacitor (MIM0) transforms the impedance of the loaded divider to 50 Ω. The simulated input and output voltage-standing-wave-ratios at 70 GHz and 140 GHz are 1.02 and 1.20, respectively. The 0.75-pF series capacitor also decouples the gate bias from the RF input.

Fig. 5 shows the TWA equivalent circuit extracted from the HFSS simulation. It can be seen that each hot TSV is modeled with a shunt capacitor corresponding to the gap with the top ground plane, and a transformer converting the electric field of the quasi-TEM mode in the GCPW to that of the TE mode in the SIW. Additionally, an inductor and a capacitor in series represent the TSV inductance and the gap with the bottom ground plane, respectively [27]. With gaps of 13 μm and

20-μm-wide (characteristic impedance $Z_0 = 72$ Ω). A 150-μm-long line (phase delay $\theta = 33$°) with a 0.75-pF shunt capacitor transforms the input impedance of each HEMT from $12 - j80$ Ω to a real 72 Ω to ease subsequent impedance matching and phase synchronization. For example, different lengths of 72-Ω branch lines before the shunt capacitor can be used to finetune the phase at each HEMT without affecting impedance matching (Table 1).

As shown in Fig. 2, the main microstrip line has a stepped width (impedance) to broaden its bandwidth and to compensate for its loss, so that the input signal is distributed to the four HEMTs evenly in magnitude. Since the impedance of each branch line presented to the main line is 72 Ω, Z_0 of each stepped section in the main line should be 24, 36, and 72 Ω before branching out to HEMT2, HEMT3, and HEMT4, respectively. After optimization by HFSS, the final width of the main line is stepped from 41 Ω to 24 Ω, 34 Ω, and 66 Ω, respectively. Lower impedances of 34 Ω and 66 Ω rather than 36 Ω and 72 Ω, respectively, are used to compensate for the loss as the input signal travels along the main line.
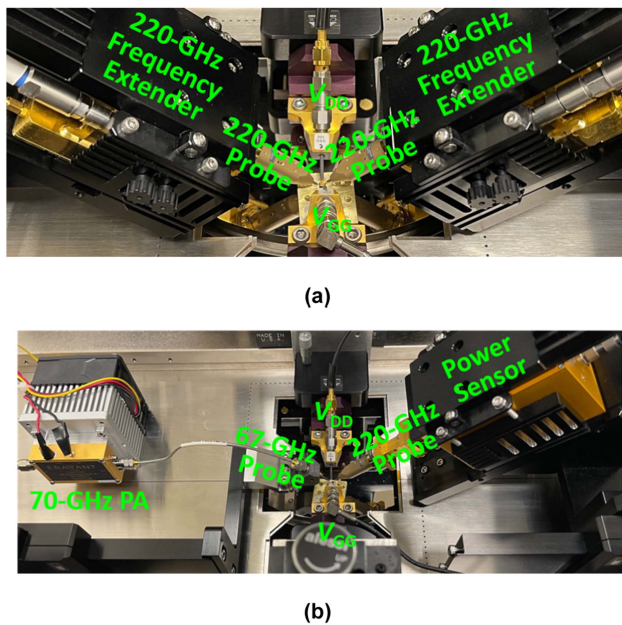
FIGURE 6. (a) Small- and (b) large-signal measurement setups.

25 μm to the top and bottom ground planes, respectively, a hot TSV has an impedance of $(2.4 - j6.8)$ Ω, which is further transformed to Z_{OPT} through a 22-Ω, 90° GCPW. The gate bias line is also shunted by an MIM capacitor after 90°.

III. MEASUREMENT

Scattering parameters are measured in a single sweep from 1 to 220 GHz using an Anritsu ME7838G vector network analyzer, with two Anritsu MA25400A frequency extenders and two MPI TITAN T220A-GSG050 probes [Fig. 6(a)] [28]. Tier-1 calibration establishes the reference planes at the probe tips, using the load-reflect-reflect-match method [29], [30] and the MPI TCS-050-100-W impedance standard substrate. Output spectra are measured from 1 to 220 GHz with the input frequency extender replaced by an Eravant SBP-5037033522-VFVF-S1 50–70-GHz, 22-dBm power amplifier and the input probe replaced by an MPI TITAN T67A-GSG0075 67-GHz probe. A Rohde & Schwarz NRP110T 110-GHz power sensor is used to calibrate the input power through a 150-μm-long coplanar through line with 0.1-dB loss [30]. Output powers are measured around 140 GHz with not only the input reconfigured as for spectrum analysis, but also the output frequency extender replaced by an Erickson PM5B power meter [Fig. 6(b)]. Similar to small-signal measurements, large-signal measurements are calibrated to the probe tips through the low-loss through line. Chips are mounted on a copper carrier hollowed out beneath hot TSVs. Large-signal simulations are performed by using HRL's models up to the seventh harmonic. The simulations use both HFSS and ADS in conjunction with the equivalent circuit of Fig. 5.
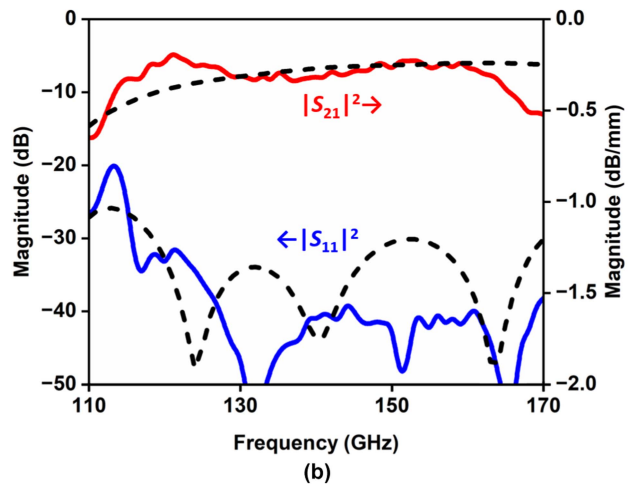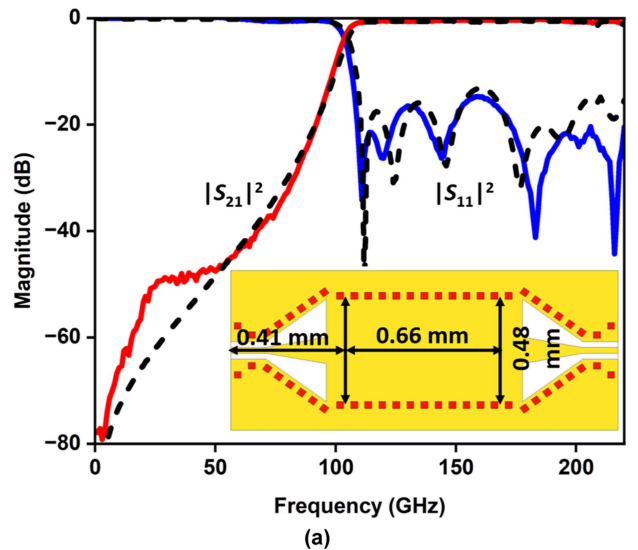

FIGURE 7. (a) Measured (solid) vs. HFSS-simulated (dash) scattering parameters of a GCPW-SIW-GCPW series with its layout shown in the inset. (b) Measured (solid) vs. HFSS-simulated (dash) scattering parameters of the SIW after de-embedding the SIW-GCPW transitions.

IV. RESULTS
A. SIW AND TWA SMALL-SIGNAL CHARACTERISTICS

Fig. 7(a) shows the scattering parameters of a 660-μm-long SIW sandwiched between two 410-μm-long SIW-GCPW transitions, which is fabricated on the same chip as the TWA. It can be seen that the measured and HFSS-simulated results agree across the entire 220-GHz bandwidth, even when the insertion loss approaches 80 dB. Across the D band, the measured return loss is greater than 15 dB, confirming that both the SIW and the SIW-GCPW transition are broadband. The best agreement with measured data is achieved by using a dielectric constant of 10.3 for SiC, which is within the range of our experimentally extracted value of 10.2 ± 0.1 [18], [19], but higher than the foundry-supplied value of 10.

Fig. 7(b) shows the scattering parameters of the 660-μm-long SIW section after de-embedding the SIW-GCPW
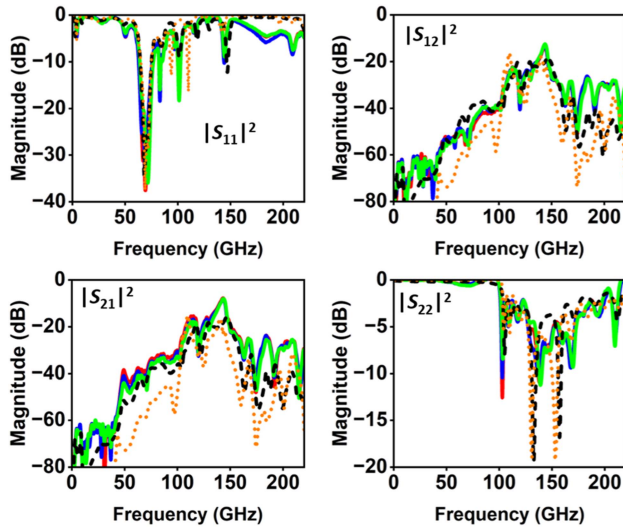
FIGURE 8. Measured (solid) vs. HFSS-simulated (dashed) and ADS-simulated (dotted) small-signal characteristics of three TWA chips (red, blue, and green). $V_{GG} = -1$ V; $V_{DD} = 12$ V.

FIGURE 9. Measured input and output spectra of a TWA under an input power of 15 dBm at 70 GHz. $V_{GG} = -1$ V; $V_{DD} = 12$ V.

transitions. The de-embedding is through a tier-2 calibration using the through-reflect-line method [31] and the SIW impedance standards fabricated on the same chip [11]. Across the D band, the average insertion loss is 0.3 dB/mm, which is higher than the 0.2 dB/mm value we previously reported [11]. This is mainly because the present substrate thickness is 50 μm (vs. 100 μm in [11]) and the metallic loss of an SIW increases inversely proportional to the substrate thickness [25]. On the other hand, the de-embedded insertion loss of the SIW-GCPW transition remains at 0.2 dB independent of the substrate thickness [28].

Fig. 8 shows that the scattering parameters across the ultrawide bandwidth of 220 GHz of three TWA chips from the same design and wafer. As designed, $|S_{11}|^2$ has a minimum around 70 GHz, $|S_{21}|^2$ and $|S_{12}|^2$ both peak around 140 GHz, and $|S_{22}|^2 > -1$ dB below 100 GHz. It can be seen that the measured values agree with each other as well as that simulated by HFSS. The ADS simulation based on the equivalent circuit reasonably mimics the measurement and HFSS simulation. This help to validate HRL's small-signal model and our measurement and simulation techniques.

B. TWA LARGE-SIGNAL CHARACTERISTICS
Fig. 9 shows the ultra-wideband 220-GHz input and output spectra of a TWA under $P_{IN} = 15$ dBm. From the input spectrum, it can be seen that the 140-GHz harmonic is 36 dB below the 70-GHz input signal, indicating the input signal do not have significant harmonic content and the driver amplifier is linear. (We believe the spurious modes at 35 and 60 GHz are from band-stitching issues in the receiver itself rather than the signal source or driver amplifier.) The ratio is reversed in the output spectrum, so that the 140-GHz P_{OUT} is 38-dB higher than the 70-GHz P_{IN}, validating the frequency doubler. The third harmonic of 210 GHz is 27 dB below that at 140 GHz.
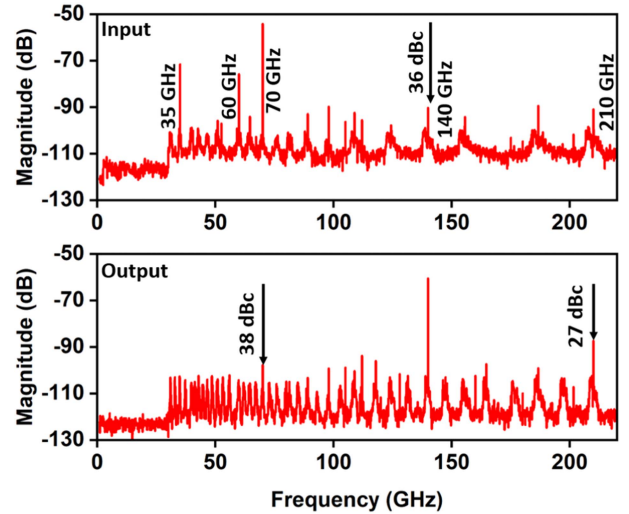
The noise floor of the output spectrum is approximately 10 dB lower than that of the input spectrum, probably because the SIW power combiner also suppresses the noise below 100 GHz.

Fig. 10(a) shows the power-sweep characteristics of a TWA with f_{IN} as a parameter. Although the Erickson PM5B power sensor is broadband, its measured power of the TWA output is mainly due to the second harmonic around 140 GHz, because the fundamental and third harmonics are < -30 dB below the second harmonic. The WR6 waveguide connecting the TWA to the power sensor also cuts off signals below 110 GHz. It can be seen that P_{OUT} tends to saturate around 14 dBm. For example, under $P_{IN} = 20$ dBm at 68 GHz, $P_{OUT} = 14$ dBm at 136 GHz with a DC power consumption of 882 mW. This P_{OUT} at 136 GHz is comparable to that of [22] at 100 GHz, but significantly higher than that of [21] at 77 GHz. Unlike the small-signal model, HRL's large-signal model does not seem to fully capture accurately harmonic generation under gain compression. In the future, the large-signal model can be improved by using our newly established ultra-wideband capability for large-signal characterization of a 70-GHz transistor up to its third harmonics in a single sweep of frequencies. Fig. 10(b) illustrates the bandwidth of the TWA. It can be seen that with $P_{IN} = 18$ dBm, $P_{OUT} > 10$ dBm from 132 to 140 GHz, corresponding to a 3-dB bandwidth of 6%. Near the band center, the conversion loss is 5–6 dB.

V. DISCUSSION
Table 2 compares the present D-band frequency multiplier with those reported for different transistor technologies [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51]. It can be seen that this work not only is the first D-band frequency multiplier based on the GaN HEMT technology, but
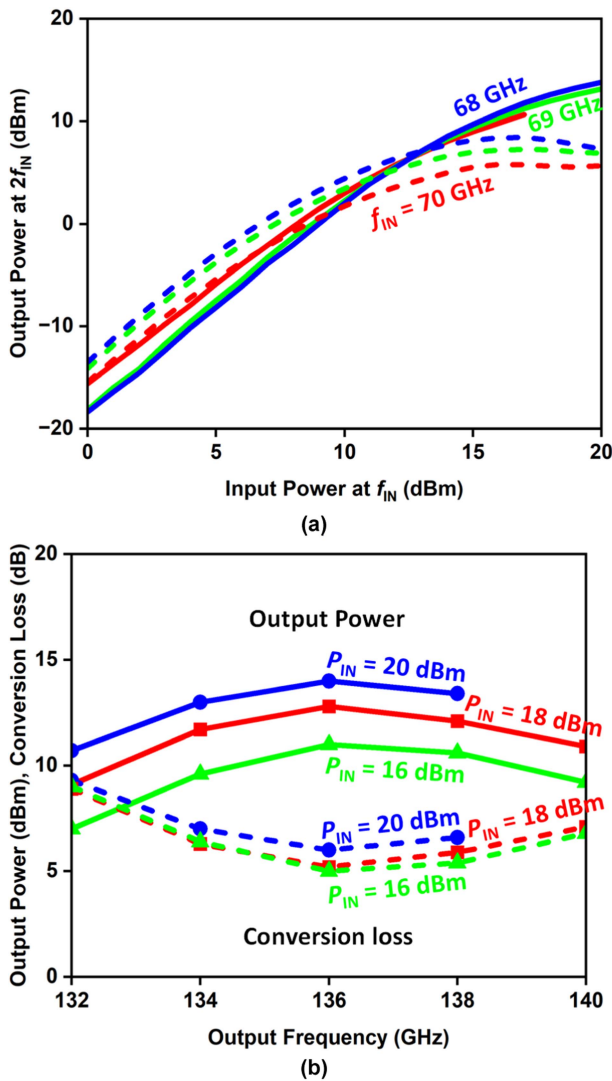
FIGURE 10. Measured (solid) vs. simulated (dash) output power as a function of (a) input power and (b) output frequency. $V_{GG} = -1$ V; V_{DD} = 12 V.

TABLE 2. D-Band Frequency Multipliers

Frequency (GHz)	Tech-nology	Multi-plication	P_{IN} (dBm)	P_{OUT} (dBm)	GAIN (dB)	f_{IN} Leak (dBc)	P_{DC} (mW)	Ref.
110–130	GaAs	×2	2	5	3	−25	65	[32]
119–135	InP	×3	3	10	7	−30	45	[33]
134	CMOS	×2	15	4.2	−3.1	NA	790	[34]
138–170	SiGe	×2	3	5.6	4.9	−37	36	[35]
117–129	CMOS	×3×3	10.3	6.3	−2.5	−25	328	[36]
130–154	SiGe	×2×2	8	10	5	−20	610	[37]
120–158	InP	×2	7	4.2	−2	−23	19	[38]
115–147	SiGe	×3×2	4.3	4.5	0.2	−12	310	[39]
129–171	SiGe	×2×2	2	2.2	5	−30	100	[40]
99–132	SiGe	×2×2	3	8.5	12	−30	79	[41]
140–180	InP	×3×2	6.3	4.6	−1.7	−13	100	[42]
108–155	SiGe	×2	0	8.1	13	NA	98	[43]
128–140	SiGe	×2	15	9.4	−1	−20	72	[44]
127–162	FDSOI	×3×2	0	5.1	6.9	NA	47	[45]
110–170	SiGe	×4	5	2.5	11	−29	100	[46]
125–145	FDSOI	×2	11.7	4.1	−5.5	NA	25	[47]
131–145	CMOS	×2×2×2	0	-2.5	−1	−34	41	[48]
137–159	CMOS	×3×2	15.5	-1.2	−0.7	−20	93	[49]
112–125	CMOS	×2	10	7.8	−0.5	NA	88	[50]
118–155	SiGe	×2×2×3	-14	3.5	19	−25	640	[51]
132-140	GaN	×2	20	14	−5	−38	842	This Work

a significant undertaking because HEMTs of different sizes will need to be designed, fabricated, characterized, and modeled before they can be incorporated in the TWA design. Then, because the impedance of hot TSVs is fixed, different impedance-matching networks will need to be synthesized to match HEMTs of different sizes.

Many D-band frequency multipliers are based on diodes instead of transistors, including those based on GaN diodes [52]. They may be replaced by transistor-based frequency multipliers as transistors are scaled up to the same operating frequency, because transistors are more linear and less noisy than diodes are.

From simulations, the present 6-dB conversion loss can be attributed to the 3.5-dB conversion loss of the HEMT, the 1-dB loss of the divider, and the 1.5-dB loss of the combiner. The 1.5-dB combiner loss is comparable to a typical D-band power combiner but 0.8 dB higher than that simulated in Fig. 1. This excess loss arises because in Fig. 1 we assume the transistors are directly embedded in the SIW, whereas in the present implementation the transistors are connected from the edge of the SIW to the hot TSVs through GCPWs with 0.6-dB loss. This interconnect loss can be minimized by heterogeneous integration of the transistors directly on top of the SIW. For example, Si MOSFETs have been bonded on D-band SIWs fabricated in Si interposers [53], [54]. The remaining 0.2-dB difference is due to the GCPW-SIW transition at the TWA output. The transition is necessary for on-wafer probing of the TWA by itself. The transition will not be necessary when the TWA is monolithically integrated with an SIW antenna.

VI. CONCLUSION
At the D band, SIWs are small enough to replace coplanar or microstrip transmission lines as a power combiner for

also has the highest output power and the lowest fundamental leakage among all D-band frequency multipliers of any transistor technology. This shows the power of the GaN technology and the benefit of the high-pass of the SIW. It is remarkable that such high output power is achieved by combining four simple 2×25 μm HEMTs, whereas most others use multistage driver amplifiers. Therefore, by combining larger transistors and multistage driver amplifiers through the high-power-capacity SIW, higher power, gain, and efficiency can be expected by using the present approach. In addition, the output power, gain and efficiency can be further improved by adding a second-harmonic reflector at the gate of each HEMT to prevent reverse leakage [44].

In the design presented here, all four HEMTs are the same size. In the future, their widths can be tapered to increase not only the output power, but also the bandwidth. It will be

high-power MMICs. For a proof of concept, a novel power-combining concept has been demonstrated through monolithic integration of GaN HEMTs with a SiC SIW. Taking advantage of the lower loss and higher power capacity of the SIW than that of planar transmission lines, much higher output power can be achieved by replacing the present HEMTs with higher-performance transistors and drive circuits. Although the SiC SIW provides an easy entry because of its mechanical strength, the present power-combining concept can be implemented in Si where the SIW is fabricated in an interposer before integration with CMOS chiplets.

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