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A D-Band Phased-Array Chain Based on a Tunable Branchline Coupler and a Digitally Controlled Vector Modulator

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(Regular Paper)

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ABSTRACT Wireless communication and sensing applications seek higher frequencies to enable higher data rates or more precise localization using a wider modulation bandwidth. Particularly, 6G and autonomous driving research projects focus on the D-band. With higher frequencies, antennas can be placed closer together, allowing for more antennas in the same area and creating a narrower beam. However, a greater number of channels increases system complexity. Each antenna typically requires one vector modulator in a phased-array system, which entails four analog control voltages and four DACs. Consequently, increasing the frequency and utilizing more channels can result in an enlarged system size due to the complex PCB design. This article presents a phased-array chain consisting of a tunable branchline coupler based on varactor diodes, a digital vector modulator, and a power amplifier. The combination of varactor diodes and the VM enables coarse phase changes through 4-bit digital switching and precise phase adjustment through varactor tuning. This approach demonstrates that a four-element array only requires two DACs instead of 16 to cover the entire angular range. The phased-array chain was designed and manufactured using B11HFC silicon-germanium technology from Infineon Technologies AG.

INDEX TERMS 6G, automotive, B11HFC, BiCMOS, BPSK, branchline coupler, CDM, code-division, D-band, MIMO, multiple-input multiple-output, phase-shifter, phased-array, power amplifier, PA, radar, radar-communication, RadCom, SiGe, silicon-germanium, TDM, time-division, tunable, varactor diode, vector modulator, VM.

I. INTRODUCTION

Nowadays, the spacial detection of objects using radar is not limited to military and automotive applications but is also increasingly utilized in a wide range of non-military and non-automotive domains. In a radar system, the bandwidth, array size, and the number of antennas play crucial roles in achieving precise localization and distinguishing different objects in three-dimensional space [1, p. 8] [2]. By employing higher center frequencies, it is possible to increase the absolute bandwidth while maintaining the same relative bandwidth using frequency multiplication, as well as accommodate a greater number of antennas within a given area. These factors have led to a growing focus on radar systems in the D-band in recent research endeavors. Moreover, research is also being conducted on exploring frequency ranges beyond the D-band, such as the THz range, using silicon technologies [3], [4], [5], [6].

However, the D-band also presents significant challenges. Firstly, the gain of transistors decreases as the frequency increases [7, p. 154]. Secondly, the free-space path loss increases in this frequency range [8, p. 5]. Additionally, the use of off-chip transitions for antennas on the RF PCB becomes progressively more lossy [9]. These factors can

be partially or fully compensated for by employing large phased-arrays [10], [11], [12]. This allows for an increase in transmitted power and improvement in the system's signal-to-noise ratio (SNR) [13], [14], [15]. Moreover, this approach can be combined with the widely used MIMO technique, known as phased-MIMO [16], [17], [18], [19]. However, it is important to note that the utilization of numerous antennas will lead to an increase in system complexity, particularly on the PCB. To address this, we propose a novel approach to mitigate the complexity.

Beamsteering requires components that can modify the output phase such that multiple beams can be combined to a strong one. In our phased-array chain, we employ two components to achieve the desired beamsteering capabilities: a tunable branchline coupler and a digital vector modulator (VM) that has been previously published [20]. The VM is utilized to generate coarse phase steps ($\approx 45°$), while the tunable branchline coupler generates smaller phase steps (less than $1°$). Together, they enable phase steps ranging from $0°$ to $360°$. Although this approach slightly increases the complexity of the monolithic microwave integrated circuit (MMIC) compared to conventional methods employing a $90°$ hybrid coupler and analog VM, it offers significant advantages. For instance, it enables the generation of steerable phase-modulated continuous wave (PMCW) signals by inverting the constellation points in the digital VM [21], [22], [23]. Additionally, the VM facilitates joint radar-communication (RadCom) capabilities [24], [25]. The digital VM only requires fast input-output (IO) signals for generating phase-modulated signals, eliminating the need for fast digital-to-analog converters (DACs) and reducing system complexity. Furthermore, the impact of varactor diodes on phase changes exhibits low sensitivity, allowing for the use of cost-effective 8-bit DACs. As demonstrated later in this article, a significant reduction in the number of DACs required can be achieved while maintaining full angular coverage and minimizing PCB complexity.

Typically, vector modulators consist of Gilbert cells [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41] or multiple variable gain amplifiers [42], [43], [44], [45], [46], [47], where the gain and phase are adjusted using mostly four analog control voltage. However, this approach introduces significant complexity that needs to be managed either on the MMIC or the PCB. In a system with four antennas, a total of 16 DACs are required. In future D-band systems, it is highly likely that the number of antennas, and consequently the number of DACs, will increase. To address this issue, we propose the utilization of a digital VM and the generation of the required in-phase (I) and quadrature-phase (Q) signals using a tunable branchline coupler. Through careful system design, the number of DACs can be significantly reduced without compromising important system characteristics.

In this article, we begin by presenting the simulation and measurement results of the breakout MMIC and its constituent components in Section II. Subsequently, in Section III, we showcase the measurement results of the complete phased-array chain, including an in-depth analysis of the tuning behavior. Section IV focuses on the analysis of the phased-array properties and the beamsteering capability. Finally, we conclude the article in Section V.

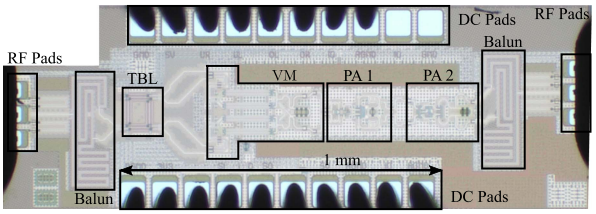

FIGURE 1. Photograph of the breakout MMIC containing RF pads, baluns, and the chain with the tunable branchline coupler, the digital vector modulator and the two-stage PA.

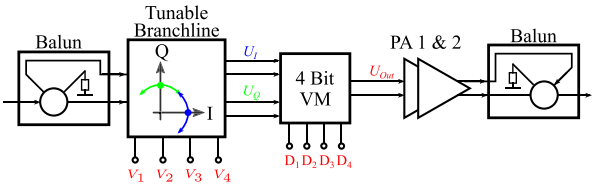

FIGURE 2. Block diagram of the breakout MMIC containing RF pads, baluns, and the chain with the tunable branchline coupler, the digital vector modulator and the two-stage PA. The operating principle of the branchline coupler is highlighted in green and blue and can be controlled using V1 to V4.

II. BREAKOUT DESIGN

The breakout MMIC (measuring $1815 \times 620\,\mu\text{m}^2$) of the phased-array chain is depicted in Fig. 1 and the corresponding block diagram is shown in Fig. 2, respectively. It contains single-ended RF pads, rat-race baluns, a tunable branchline coupler, a digital VM, and a two-stage PA. The inclusion of baluns is necessary for characterizing the chain using single-ended D-band probes. The tunable branchline coupler generates IQ signals, which get superimposed and/or inverted by the vector modulator (U_{Out}). While the tunable branchline coupler employs four analog tuning voltages (V1-V4), the VM utilizes only four digital 3.3 V signals (D1-D4), thereby reducing the number of required DACs. Finally, the signal is amplified by the two-stage PA. The breakout MMIC was designed and manufactured using the B11HFC silicon-germanium technology from Infineon Technologies AG. This technology offers an f_t/f_{max} of 250/370 GHz [48].

A. TUNABLE BRANCHLINE COUPLER

While the tuning of output phases using varactor diodes is not a new technique, it has primarily been applied within couplers up to the S-band frequency range [49], [50], [51], and as a tunable load outside the coupler up to the W-band [52], [53], [54], [55], [56], [57], [58], [59], [60]. In this work, we expand the utilization of varactor diodes inside a coupler to

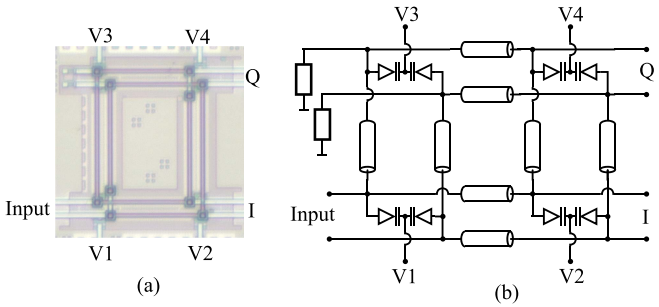

FIGURE 3. Photograph of the tunable branchline coupler (a) and the simplified schematic consisting of TRLs and varactor diodes (b).

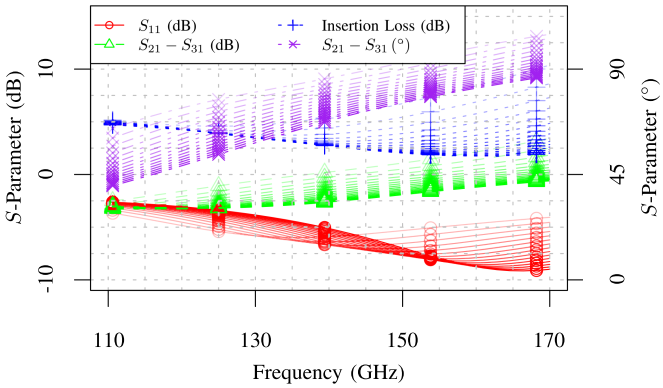

FIGURE 4. Simulation results of the tunable branchline coupler when every varactor diode is tuned evenly. The varactor diodes include RC parasitics and the TRLs are full-wave simulated.

the D-band frequency range, despite their relatively lower Q-factors. By incorporating varactor diodes, we are able to modify the phase in this higher frequency range.

The developed tunable branchline coupler, illustrated in Fig. 3, is based on a lumped-element approach. In this design, we replace the quarter wavelength 50 Ω and $50/\sqrt{2}\,\Omega$ transmission lines (TRLs) with inductors and capacitors. To overcome the design rule challenges associated with implementing tiny differential inductors in the D-band, we employ short and straight (66 μm and 94 μm) TRLs with an impedance of 107 Ω. To achieve this, we utilize the top and second-lowest metal layers in the metal stack and make the TRLs as narrow as possible. The length of the TRLs, and thus their inductance, is selected to satisfy the equations specified in [61, p. 232].

In contrast to MIM (Metal-Insulator-Metal) capacitors, we utilize differential varactor diodes to adjust the phases of the coupler's IQ outputs. The varactor diodes are positioned below the ground plane of the 107 Ω TRLs. Remarkably, considering the center frequency of 125 GHz (on-chip wavelength of $\lambda_{Si} \approx 1.2$ mm), the overall size of the coupler is only $150 \times 150\,\mu\text{m}^2$.

The Figs. 4 and 5(a)–(f) present the simulation results of the coupler. In our simulations, we included all metal structures and the 50 Ω resistors using Sonnet 18.52. Additionally, we

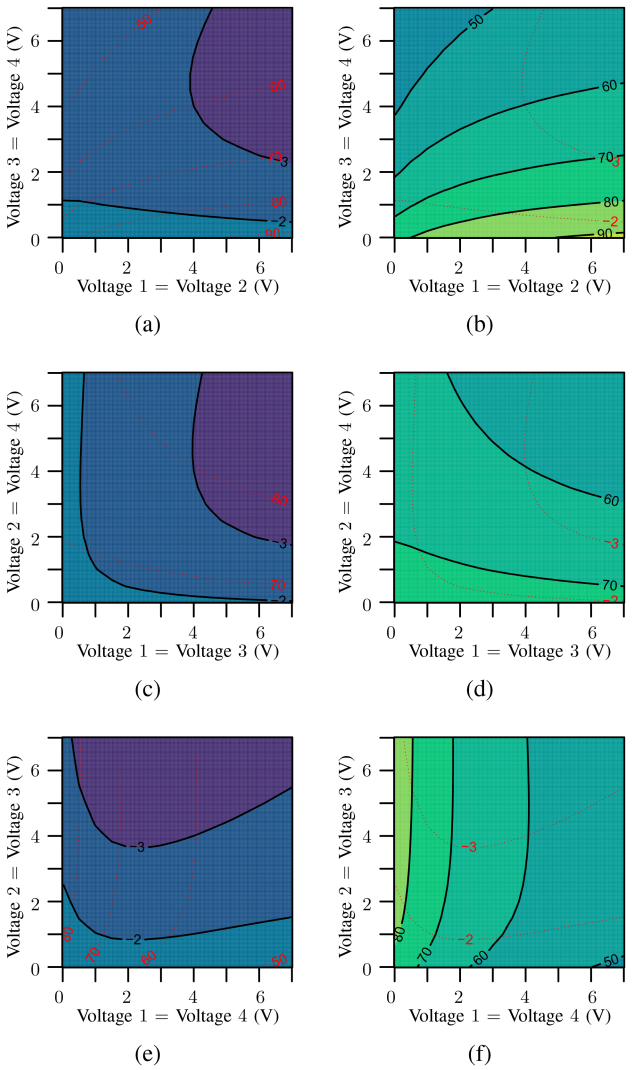

FIGURE 5. Simulation results of the tunable branchline coupler at 125 GHz when two varactor diodes share one tuning voltage. The varactor diodes include RC parasitics and the TRLs are full-wave simulated. On the left side (a), (c), and (e), the amplitude imbalance is shown (dB) and on the right side the phase imbalance (°) at the outputs of the branchline coupler (b), (d), and (f). The contour lines of the other plot are shown in red dashed lines. From top to bottom, we are changing the used tuning voltages.

incorporated the varactor diodes, along with their RC parasitics, into the Cadence S-parameter simulation. Due to the limitation of visualizing a component with four inputs, we can only present cutting planes of the $\mathbb{R}^4$. In Fig. 4, we illustrate the scenario where all analog inputs are evenly tuned from 0 V to 7 V with steps of 0.5 V. The transparency of the lines and markers indicates the amplitude of the tuning voltage.

While analyzing the characteristics, including input matching, amplitude imbalance, and insertion loss, we observe a wideband behavior in the lower half of the D-band. These parameters vary less than 3 dB in the lower half of the D-band ($\approx 25°$ from 110 − 140 GHz). But, the phase difference indicates more changes over frequency, particularly within the lower half of the D-band. However, the adjustable phase

difference at a given frequency is slightly larger in the lower D-band than in the upper, which fits our goal of tuning the phase. The ideal 90° phase difference and 0 dB amplitude imbalance are only reached in the upper D-band. From this, one could conclude that the transmission lines and capacitors are too small. However, the TRL length and varactor size influence the insertion loss. We wanted to avoid amplitude variation when targeting phased-array operation. Therefore, we have chosen the TRL length and varactor size so that the insertion loss and amplitude imbalance shows minor variation while still maintaining $\approx 90°$ phase difference. As shown later in the article, satisfactory beamsteering can be achieved even with an IQ phase difference of $< 90°$.

In Fig. 5(a)–(f), we present the tuning of the four varactor diodes using two different voltages. To provide an enhanced visualization, we utilize contour plots at the frequency of 125 GHz. In these plots, one of the parameters, either the amplitude or phase imbalance, is displayed, while the other parameter is represented by red dashed lines within the same plot. By adjusting the tuning voltage, we observe that the phase difference can be modified by over 40°, accompanied by an amplitude variation of ≈ 2 dB.

B. VECTOR MODULATOR DESIGN

The branchline coupler is followed by the VM, which can shift the signal in $\approx 45°$ steps. The control is purely digital with 0 V or 3.3 V control signals. The VM has four control signals, which results in eight different states in the constellation diagram - similar to an 8-PSK. Internally, the VM consists of four very compact integrated PAs sharing an inductive load. Due to the vector superposition, the states where both I and Q are active are ≈ 3 dB larger. Up to ≈ 6.5 dB gain can be achieved. The complete article containing all results of the VM can be seen in [20].

The use of a digital vector modulator offers several advantages. Firstly, fast modulation schemes do not require high-speed DACs. Although only low-complexity modulation schemes are supported, the digital VM simplifies system design. Additionally, it reduces power consumption, as silicon-based DACs operating in the speed range of $1-3$ GS/s typically consume approximately $68-430$ mW and occupy an area of $0.16-0.825$ mm^2 [62], [63], [64], [65], [66]. As the number of channels increases, the integration of fast DACs can pose significant challenges in system design. To circumvent this issue, we employ an approach that avoids the need for fast DACs and instead relies on fast IO signals (e.g., from an FPGA).

C. POWER AMPLIFIER

The last stage with active circuits is the two-stage PA with a size of $510 \times 140\,\mu$m^2. We made a separate breakout MMIC to analyze the S-parameters of the PA. The photo of the MMIC is shown in Fig. 6, and the schematic of the PA is in Fig. 7. We have chosen a topology with a common-emitter and a common-base stage for both PA stages but using larger transistors in the second stage. Both PAs are connected via

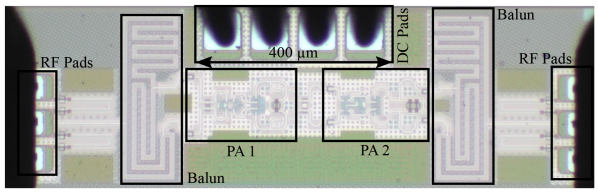

FIGURE 6. Photograph of the breakout MMIC containing dc pads, RF pads, baluns, and the two-stage PA.

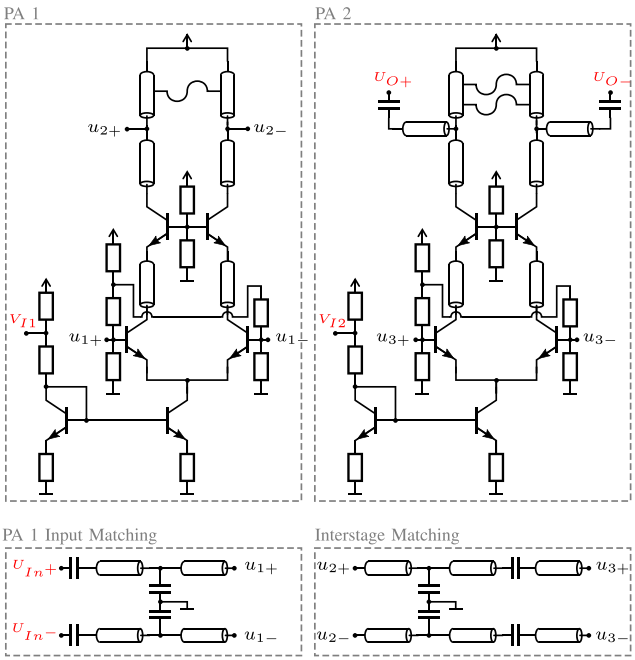

FIGURE 7. Circuit diagram of the two-stage PA. The output matching and, therefore, the S_{21} behavior can be adjusted by cutting laser fuses. Both PAs share the same topology but with differently dimensioned HBTs and dc currents.

an interstage matching network to ensure best power transfer. Both PAs can be tuned via analog control voltages to adjust the dc current inside the PA (V_{I1} & V_{I2}). However, changing the dc current was not necessary to achieve the highest possible gain.

Both stages have an inductive load consisting of TRLs and laser fuses. By cutting the laser fuses, the length of the TRL and, therefore, its inductance can be changed after manufacturing so that the center frequency can be changed downwards. We achieved the best results when the first PA was not changed, and both fuses were removed from the second PA. This way, we achieved a wideband S_{21}. The S-parameters are shown in Fig. 8. The losses of the RF pads and baluns were determined with a back-to-back structure and subtracted from the S_{21} parameter (cf. [20]). Since the output matching of the last PA stage was designed for broadband S_{21}, we decided not to apply de-embedding using $ABCD$-parameters, which would cause major errors [67].

The PA is measured with a Keysight PNA-X N5247B, VDI D-band extenders, and Formfactor Infinity probes, which

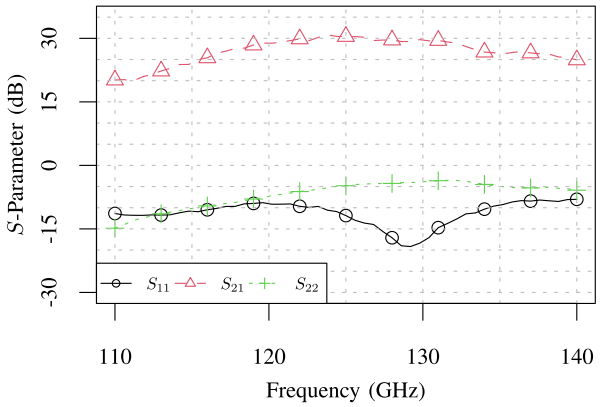

FIGURE 8. Measurement results of the two-stage PA after subtracting the S_{21} losses of a pad and balun back-to-back structure. In the second PA we cut two fuses to match the center frequency to 125 GHz.

were calibrated with a SOLT substrate. The extender on the input side is equipped with an attenuator set to 25 dB. The center frequency of the PA chain is 123.7 GHz, where a gain of 31.2 dB is obtained. We achieve a 3/6 dB bandwidth of 13.4/24.7 GHz and 10.9/19.9%, respectively. The power consumption of the two PAs is 197.5 mW at a supply voltage of 5 V. Also, we simulated an input referred 1 dB compression of −20.98 dBm and a saturated output power of 6.8 dBm using RC parasitics and a device temperature of 80 °C. In particular, the gain is very competitive compared to the current PA survey [68].

III. PHASED-ARRAY CHAIN RESULTS

Now that all individual components have been characterized, the behavior of the entire chain is analyzed. For this purpose, we show the constellation diagrams at 125 GHz, when all varactor diodes are tuned identically (Fig. 9) or differently (Fig. 10). In the first case, we use 100 mV steps starting with 0 V and ending with 7 V. In the latter case, we use 0 V, 0.5 V, 1 V, 2 V, and 7 V. While smaller steps would give more insights into the chain's behavior, the number of analog tuning steps N increases the measurement time exponentially (4^N).

When characterizing the phased-array chain, we used the same measurement setup as for the PA. The whole chain has a power consumption of 355 − 441 mW depending on the VM's used states. The chain has a peak gain of 32.1 dB when tuning the varactor diodes evenly (cf. Fig. 9) and 32.9 dB when tuning the varactor diodes differently (cf. Fig. 10).

When all varactor diodes are tuned evenly, the analog tuning voltage shifts the constellation points. However, not every constellation point is shifted in the same amount. While I and $I + Q$ show excellent tuning behavior, Q does not. Only minor phase changes are noticeable when increasing the voltage. The tunable branchline coupler causes this effect since the I and Q outputs behave differently when the varactor diodes capacitance is changed evenly. The tuning behavior of the Q state is visible only if the varactor diodes are tuned differently.

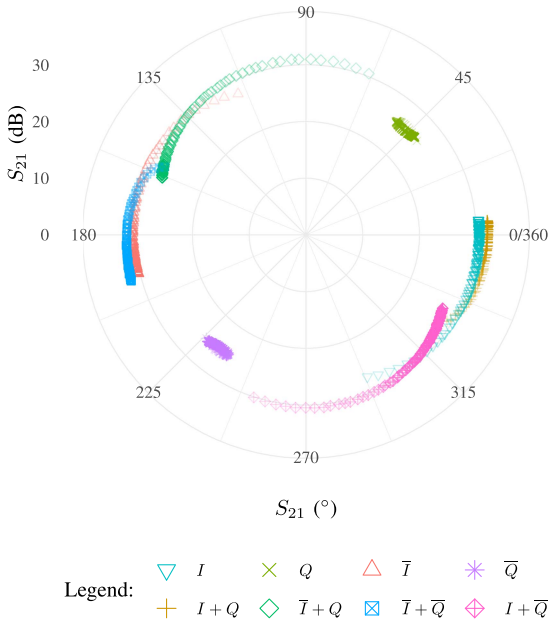

FIGURE 9. Constellation diagram of the 125 GHz phased-array chain when all varactor diodes are tuned evenly. The eight different states of the digital VM are highlighted using different markers and colors. The level of the tuning voltage is mapped with the color intensity.

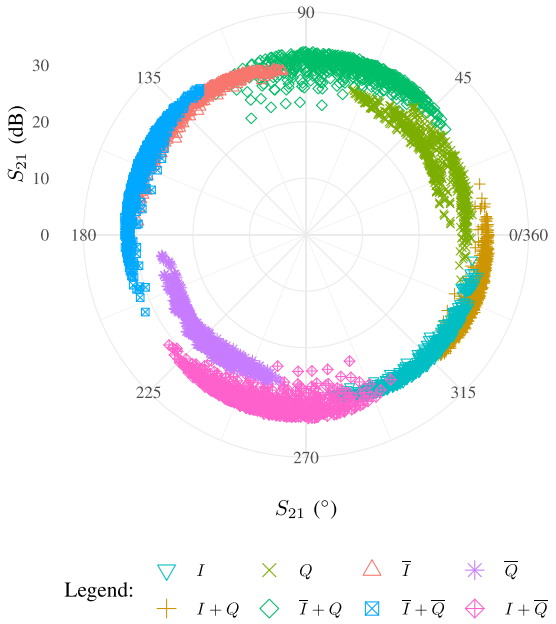

FIGURE 10. Constellation diagram of the 125 GHz phased-array chain when all varactor diodes are tuned differently. The eight different states of the digital VM are highlighted using different markers and colors. No voltage to color intensity mapping is applied.

In this case, output phases in the complete angular range are achievable.

A. COMPARISON

A direct comparison between different phased-array chains is challenging due to the varied weighting of criteria depending

on the specific approach employed. Furthermore, different techniques and components are utilized in each chain, making a one-to-one comparison impractical. Nevertheless, we provide examples of phased-array chains operating in a similar frequency range using SiGe technology.

In [26], a 125 GHz chain is presented, which achieves 18 dB peak gain and uses a 360° analog phase shifter and a PA (core size: 400 × 250 μm^2; P_{dc} = 195 mW). At 150 GHz, [11] achieves 15 dB gain and uses two amplification stages and an analog phase shifter. The four-channel TX MMIC has a size of 1760 × 1570 μm^2 and consumes 1100 mW. At the same frequency, [69] shows 16 dB peak gain using two VMs and two PAs. This chain consumes 330 mW and has an MMIC size of 1560 × 1260 μm^2.

IV. BEAMSTEERING SIMULATION

As circuits and antennas in D-band shrink due to the smaller wavelength compared to commercial 77 GHz radar sensors, several challenges arise. The free-space path loss increases, the gain of transistors decreases, and the effective antenna area reduces. To compensate for these effects, attempts are made to increase the number of channels and, consequently, the number of antennas. However, this introduces a significant challenge for D-band phased-array systems.

The size of backend components, such as ADCs and DACs, does not scale with frequency. Moreover, the number of these components increases with the higher channel count. This results in a complex system design. Typically, vector modulators require four analog control voltages. For a system targeting four transmit channels, this would necessitate the use of 4 × 4 = 16 DACs. As future systems may scale to eight or even 16 channels, up to 64 DACs would be required. Consequently, in this section, we demonstrate that our approach enables beamsteering and simplifies analog control.

Our proposed topology is shown in Fig. 11 and consists of $M = 4$ antennas in a parallel-fed structure with just two tunable branchline couplers and four digital VMs. Each coupler uses one analog tuning voltage (cf. Fig. 9), which results in just two analog tuning voltages for the complete array. In summary: 87.5% of the DACs become unnecessary compared to a conventional system design with four DACs per antenna. In addition, we have planned 0.5 dB insertion loss per Wilkinson power divider (WK) to make the system analysis as realistic as possible.

We have evaluated every possible state combination of the four digital VMs ($8^4 = 4096$) using the measured VNA data and analyzed the beam steering when both couplers are tuned independently using 100 mV steps. Therefore, a total number of $71 \cdot 71 \cdot 4096 = 20.647.936$ array factors were calculated using (1) [70, p. 293].

$$F_{dB}(\theta) = 20 \cdot log_{10}\left[\sum_{m=1}^{M} A(m) \cdot e^{j\psi(m)} \cdot e^{j \cdot k_0 \vec{r}(m) \cdot sin(\theta) \cdot cos(\varphi_0)}\right] \quad (1)$$

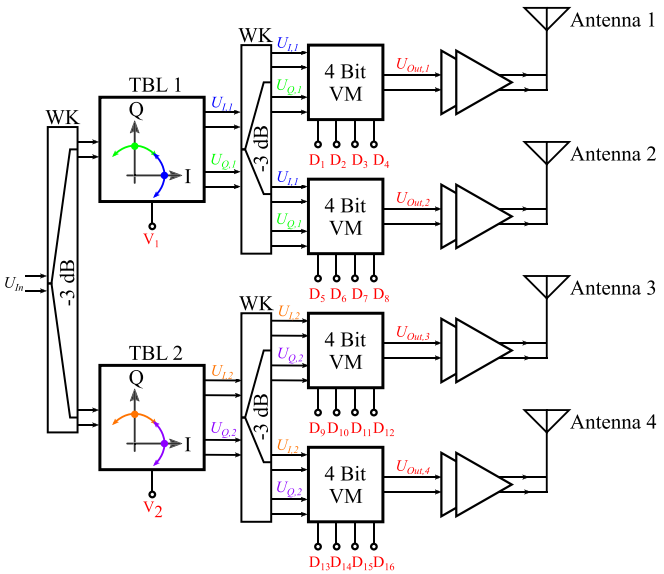

FIGURE 11. Block diagram of the investigated phased-array topology using four antennas with a λ/2 spacing. The *IQ* signals of the four channels are generated using two tunable branchline couplers and two tuning voltages, respectively. Therefore, inside each branchline coupler the varactor diodes are tuned evenly.

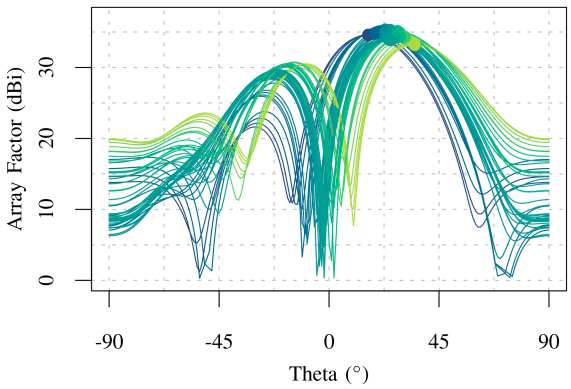

FIGURE 12. Simulation results of the phased-array topology using the S_{21} VNA measurement results. The array factor from Fig. 13(e) and (f) is plotted over θ using 1 V steps.

$A(m)$ is the measured S_{21} (dB) parameter in linear representation, ψ is the measured S_{21} (°) parameter, $k_0 = 2\pi/\lambda_0$ is the wave number, θ is the spatial angle at which the beam is steered, and φ_0 is a constant angle.

The evaluation of the combination was automated, and the best combinations are shown in Fig. 13(a)–14(f). The left plot shows the array factor and the right plot shows the angle of the beam. The contour lines of the other plot are shown in red dashed lines. We have interpolated the calculated array factors so that the tuning voltages have a step size of 27.3 mV, which represents a low-cost 8-bit DAC (0 to 7 V) [71].

A combination of states must be used to cover the entire angle spectrum. When choosing the right states of the VMs, the angular range can be roughly defined, and with the two analog

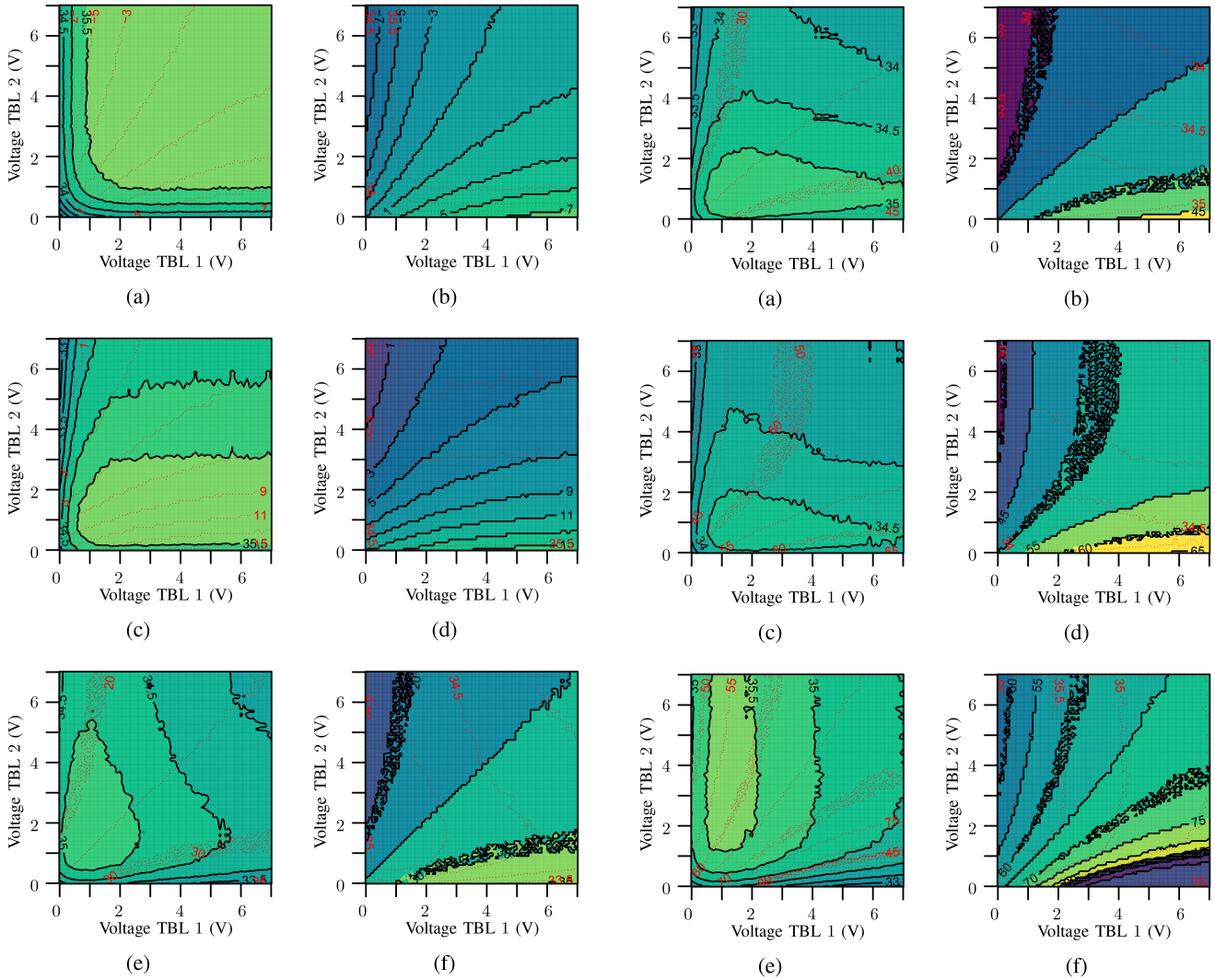

FIGURE 13. Simulation results of the phased-array topology using the S_{21} VNA measurement results. Just two analog tuning voltages are used for the four element array. The side-by-side plots show the tuning behavior for all voltage combinations (array factor (dBi) on the left (a), (c), and (e) and steering angle (°) on the right (b), (d), and (f). The states of the VMs are changed from top to bottom to cover specific angular ranges ((a) and (b): −7° − 7°, (c) and (d): 0° − 15°, and (e) and (f): 15° − 30°).

FIGURE 14. Simulation results of the phased-array topology using the S_{21} VNA measurement results. Just two analog tuning voltages are used for the four element array. The side-by-side plots show the tuning behavior for all voltage combinations (array factor (dBi) on the left (a), (c), and (e) and steering angle (°) on the right (b), (d), and (f). The states of the VMs are changed from top to bottom to cover specific angular ranges ((a) and (b): 30° − 45°, (c) and (d): 45° − 60°, and (e) and (f): 60° − 90°).

tuning voltages, the beam can be controlled in tiny steps. This allows for compensating small manufacturing tolerances without changing the pre-calculated states of the VMs.

In Fig. 12 we show the behavior of the beam angle as a function of the two tuning voltages. The states of the VM are chosen so that the angular range from 15° to 30° is covered (cf. Fig. 13(e)). For a better overview, the step size of the voltage is only 1 V. The maximum array factor was marked with a dot, and the color scheme is the same as in Fig. 13(e). It can be seen that with a variation of the tuning voltages, the beam can be steered while maintaining a nearly constant array factor.

In a phased-array system, the phase difference between every antenna determines the beam direction. When the state of every VM is inverted by 180°, the beam direction stays the same since the actual phase difference between each antenna stays the same (cf. (1)). Therefore, combining a tuneable branchline coupler and a digital VM is also suited for steerable phase-coded transmit signals. An in-depth look into the phase inversion properties of the VM can be found in [20].

V. CONCLUSION

This article presents a phased-array chain operating at a frequency of 125 GHz and introduces a novel approach to reduce the number of DACs and minimize system complexity. The branchline coupler used for vector modulation is enhanced by incorporating varactor diodes to refine the coarse 45° phase

steps of the VM. The tunable and varactor-based branchline coupler, measuring $150 \times 150\ \mu m^2$, enables analog phase control, while the digital vector modulator provides digital phase control. The signal is then amplified by a two-stage PA with a maximum gain of 31 dB.

When the varactor diodes are evenly tuned, the phased-array chain covers almost the entire angular spectrum. However, by individually tuning each varactor diode, the chain covers the complete angular spectrum, showing significant overlaps between the states of the VM.

To investigate the system properties, a parallel-fed phased-array topology was developed, requiring only two analog control voltages and, consequently, only two DACs. In contrast, conventional approaches typically demand 16 DACs, eight times more than the proposed method. The reduction of 87.5% in the number of DACs is particularly crucial when dealing with large arrays.

Moreover, the combined approach of analog tuned varactor diodes and a digital vector modulator not only reduce the number of DACs but also facilitates the generation of phase-coded signals for PMCW radar or communication applications. This is accomplished by appropriately inverting the digital states of the vector modulator.

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