IEEE Journal of Microwaves

Received 12 June 2023; revised 10 August 2023; accepted 14 August 2023. Date of publication 1 September 2023; date of current version 9 October 2023.

Digital Object Identifier 10.1109/JMW.2023.3307630

A Broadband Asymmetrical Doherty Power Amplifier With Optimized Continuous Mode Harmonic Impedances

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(Regular Paper)

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This work was supported by Engineering and Physical Sciences Research Council, funded by the Centre for Doctoral Training in Future Communications under Grant EP/L016656/1.

ABSTRACT This article presents a design methodology for an asymmetrical Doherty Power Amplifier (DPA) which achieves a high average efficiency at back off across its operating bandwidth. It is shown that by combining continuous modes with post matching techniques, it is possible to achieve excellent efficiency performance whilst maintaining broadband operation. Analysis is provided on how the knee effect can reduce the effective potential efficiency of Class J and Continuous Inverse Class F modes. An optimum combination of 2nd and 3rd harmonic impedances is then proposed for the carrier PA which can minimise this knee effect impact on efficiency performance. Also, it is shown how the drain supply can be used to improve the bandwidth over which an intrinsic optimum load can be maintained. Based on this analysis, a simple iterative design procedure is then presented which can be directly implemented with standard RF design tools. This design procedure is then verified in the design and manufacture of a prototype DPA using the Wolfspeed CG2H40010F GaN HEMT. The realised PA operates between 2.1 and 3.2 GHz with a peak power output of between 43.9 and 44.5 dBm. The PA achieves a high average drain efficiency of 64.7 % at 8–9 dB of back off. The DPA has been tested with and without digital pre-distortion (DPD) by considering a 60 MHz LTE OFDM signal with 9 dB peak-to-average power ratio (PAPR). When DPD is enabled, the presented DPA achieves a drain efficiency of between 52.1–64.3 with an adjacent channel power ratio (ACPR) of between −42.2– −44.1 dB over the bandwidth of 2.1–3.2 GHz.

INDEX TERMS Doherty power amplifier, continuous modes, high efficiency, class J, gallium nitride (GaN), continuous inverse class F, digital pre-distortion (DPD), load modulation, wideband.

I. INTRODUCTION

Wireless mobile communication standards are ever evolving, looking to provide higher data rates to users. To achieve these data rates more complex modulation schemes are being used along with larger bandwidths and more frequency bands. The complex modulation schemes used tend to feature waveforms with high Peak-to-Average Power Ratios (PAPRs). These bandwidths and complex waveforms put extra demand on the performance requirements of Radio Frequency Power Amplifiers (RF PAs). Firstly, it is often difficult to match a transistor device within a PA to a 50 Ω system over a significant bandwidth while maintaining sufficient efficiency performance, due mostly to the quality factor of matching circuits used. Secondly, high PAPR waveforms cause the efficiency of the PA to degrade due to the PA operating in output power back-off (BO). This has lead to various techniques to try to improve efficiency at BO including Sequential Power Amplifiers (SPAs) or load modulated amplifiers such as Doherty Power Amplifiers (DPAs) and Load Modulated Balanced Amplifiers (LMBAs). These load

modulation techniques operate on the same fundamental principle which is to change the impedance presented to the transistor device at BO to minimise DC losses and increase efficiency.

One promising technique is a DPA, though with the traditional implementation there can be bandwidth limitations. Traditional DPAs feature impedance transformations using quarter wave transmission lines which are inherently limited in the bandwidth in which they can transform a given load. Also, traditional DPAs tend to be limited to 6 dB in BO. Therefore, to overcome this, the peaking and carrier amplifiers within the DPA need to be designed to deliver different power levels at Peak Output Power (POP), to then create asymmetrical operation and a high BO level which approaches modern PAPRs, which are typically in the range of 9 to 14 dB. To overcome the bandwidth issue there have been various techniques proposed which aim to use other ways of providing impedance transformation, where [1] gives a good review of these techniques. A promising technique to improve bandwidth is known as Post Matching (PM) which improves bandwidth by replacing the impedance inverter and impedance transformer within a traditional Doherty. Device parasitics are typically absorbed in the impedance inverter whilst an impedance transformer known as the Post Matching Network (PMN) is implemented as a higher order transformer to improve bandwidth. There are plenty of examples of PM in [2], [3], [4], [5], [6], [7], [8], with high BO operation achieved in [5], [6], [7], [8].

To improve the efficiency and bandwidth performance of the DPA, Continuous Modes (CM) can be introduced into the design. These modes can theoretically achieve high efficiency over a large bandwidth. There are multiple examples of implementing CM in a DPA within literature with [9], [10], [11], [12], [13], [14], [15], [16], [17], where CM have been combined with the PM technique in [12], [13], [14], [15], [16], [18]. All of the examples however are limited to 6 dB in BO. In the particular cases of [12] and [16], there is some resistive loading of the harmonics, around 5–10 Ω, which can reduce overall efficiency. There is one example where a CM DPA achieves greater than 6 dB of BO in [17]. This approach achieves a good average drain efficiency of 57.2 % at BO, 36 % fractional bandwidth with 9–10 dB of BO.

When examining the use of CMs further, Class J is used in [12], [13], [14], [15], [16]. With [17], Continuous Class F (CCF) mode is used, where it can be difficult to achieve the required 3rd harmonic open circuit over the reported fractional bandwidth of 36 %. In some instances the PA could therefore be operating closer to Class J, where there is a likelihood that the 3rd harmonic is terminated within the short region of the smith chart over parts of the bandwidth. As will be demonstrated in this article when analysing CMs under the influence of a real device model, the use of the Class J mode with alpha (α) values approaching zero can greatly reduce efficiency. Also, with CMs it is often thought that the 3rd harmonic termination has little effect on efficiency performance, [13], [19], and can therefore be ignored to ease the complexity of design. This is usually the case when careful consideration is made in the design to avoid knee clipping, such as the introduction of clipping contours in [20] and [21]. In this article it is found that considerations can be made on the 3rd harmonic impedance which can then play a role in the achievable efficiency with the particular transistor model used. This has been touched upon in [21] where the 3^{rd} harmonic impedance is offset to effect 2nd harmonic clipping contours. In other words, there are potentially some optimum 3rd harmonic impedances which can help avoid knee clipping from occurring, and in turn improve performance, which is further corroborated in this article.

To improve on the state-of-the-art for CM DPAs, a solution is proposed to improve BO efficiency whilst maintaining a high level of fractional bandwidth. The main novelty behind this solution is the use of the combination of Class J and Continuous Inverse Class F (CCF^{-1}) modes for the carrier within the DPA, which avoids using Class J with α values close to zero, as seen in previous works. It is shown in Section II-A that efficiency performance can be impacted by the knee region with a real device for Class J at these α values. Also, as stated, there is typically a misconception that the 3rd harmonic has little effect on efficiency. As will be demonstrated in Section II-B, by controlling the 3rd harmonic impedance the PA can be driven further into saturation without knee clipping occurring, allowing for high efficiency to be achieved. As stated with previous works in literature, a high intrinsic target impedance at BO is often used which could cause bandwidth performance loss with some DPAs. The supply voltage is therefore proposed as a design variable in Section II-C, in an effort to reduce the quality factor of the required match for the carrier PA, and hopefully allow for a intrinsic load closer to the target load. A stable intrinsic load is important in a DPA, as any variance can either cause a PA to compress early and produce less power, or move further away from compression and therefore lose efficiency. Typically within a CM DPA the harmonics are matched by the PMN, though for the first time in this article a harmonic impedance buffer close to the transistor device is used to appropriately terminate the 2nd harmonic, alleviating issues in resistive loading of harmonics seen in previous work, but also allowing for more control to achieve a particular set of harmonic impedances. The solution proposed by this article is also simple in its implementation and can remove the many complexities due to asymmetrical load modulation, and therefore the extended analysis needed to describe the interaction between both carrier and peaking amplifiers. To simplify the design and maintain high bandwidth and efficiency performance, both carrier and peaking amplifiers are designed in a simple step by step manner. This process provides an superior first run design which can then be tuned for performance within the simulator. Through the novel combination of modes used, along with optimised 3rd harmonic impedance terminations, implemented through the use of a harmonic impedance buffer, a DPA with high average BO efficiency has been realised. To the best of the author's knowledge, the proposed CM-DPA

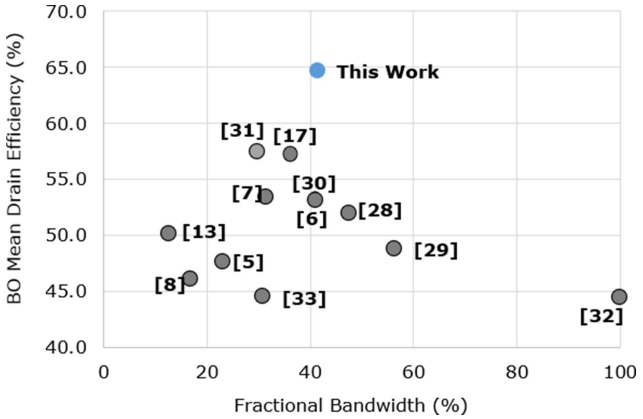

FIGURE 1. State of the art BO Average Efficiency vs. Fractional Bandwidth, with values calculated from data read from graphs. All amplifiers referenced feature BO levels greater than 8 dB.

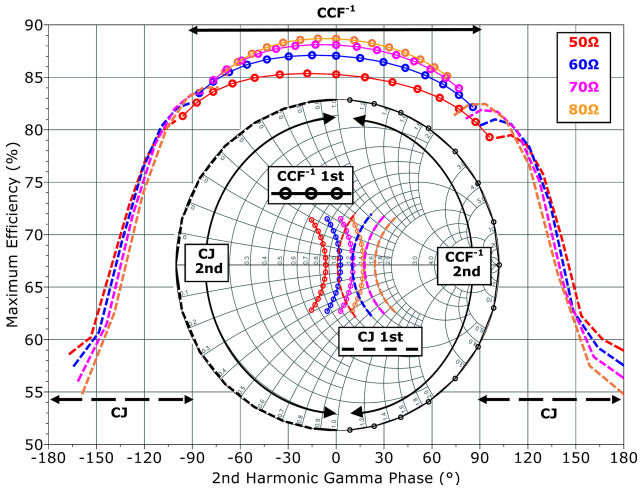

FIGURE 2. Maximum achievable efficiency based on the variation of 2nd harmonic phase, covering both Class J and CCF^{-1} optimum impedances for different Ropt values. Results are obtained by presenting optimum package impedances to the Wolfspeed CGH40010F large signal model with a harmonic balance simulation at 2 GHz.

shows the highest average drain efficiency seen in literature, at BO levels greater than 8 dB, as also depicted in Fig. 1.

II. THEORETICAL ANALYSIS

A. CONTINUOUS MODE ANALYSIS FOR OPTIMUM EFFICIENCY

Continuous Modes (CM) can be used to design a highly efficient broadband RF PA. These modes introduce a parameter α which allows for an extension on conventional modes, e.g. Class B or F. This α parameter allows for different combinations of reactive fundamental and harmonic terminations whilst still having similar efficiency performance to the more conventional underlying mode. When different PA modes were introduced, and then also their extension into CM, the waveforms of these modes often assume that there is an allowable full voltage swing which can reach zero to minimise overlap with the current waveform. Within a device such as a HEMT however, there is a knee voltage which needs to be sustained across the drain-source junction so that a given amount of drain current can flow. The impact of the knee effect on the CCF mode has been studied previously in [22] where drain efficiency was shown to drop to around 70% for α values approaching zero, instead of the theoretical 90%. Here, some analysis is provided on the Class J and CCF^{-1} modes, which extends on the initial analysis provided by the author in [23].

Theoretically, Class J should be able to achieve the same drain efficiency as Class B of around 78% across all α values, whilst for CCF^{-1} efficiency is closer to 90%. The impedances for the fundamental and second harmonic for Class J are

$$Z_{Class-J}(f_0) = R_{opt} + jR_{opt}\alpha \tag{1}$$

$$Z_{Class-J}(2f_0) = 0 - j\frac{3\pi}{8}R_{opt}\alpha \tag{2}$$

with the corresponding admittances for the fundamental and second harmonic for CCF^{-1} are

$$Y_{CCF^{-1}}(f_0) = \frac{2}{\sqrt{3}}G_{opt} + jG_{opt}\alpha \tag{3}$$

$$Y_{CCF^{-1}}(2f_0) = 0 - j\frac{7\pi\sqrt{3}}{24}G_{opt}\alpha \tag{4}$$

To examine these modes more practically under the influence of a real transistor device, and therefore examine any knee region effects on efficiency performance, a harmonic balance simulation is run with the ideal impedances of both modes presented at the intrinsic plane of the Wolfspeed CGH40010F large signal model. In all cases a perfect 3rd harmonic short is provided, with simulations run at a carrier frequency of 2 GHz. The resulting drain efficiency for varying 2nd harmonic phase of both modes for different intrinsic load values is shown by Fig. 2. With Class J, as the 2nd harmonic phase approaches a short, i.e. a Γ phase of +/- 180°, the efficiency of this mode drops to between 55-60%. For either extreme of 2nd harmonic phase for Class J however, at a phase of around +/- 90°, this efficiency increases up to 79-82%. Efficiency for CCF^{-1} remains relatively high across all values of 2nd harmonic phase and intrinsic load values, achieving between 79 to 88 %.

The voltage and current waveforms for different α values for Class J are further examined, as shown in Fig. 3. These waveforms show the mechanism behind Class J, where for increasing values of α, more 2nd harmonic voltage is induced to narrow the peak of the voltage, offsetting any increased overlap in current and voltage due to some fundamental imaginary impedance. However this same mechanism also stops the voltage from falling below the knee threshold, through some voltage trough boosting and phase shift in where the voltage minima occurs. This 2nd harmonic can therefore change the amount of knee clipping occurring which impacts the amount of 3rd harmonic current generation, shown by the broadening of the current waveform in Fig. 3. This broadening causes more overlap with VDS and therefore causes the lower

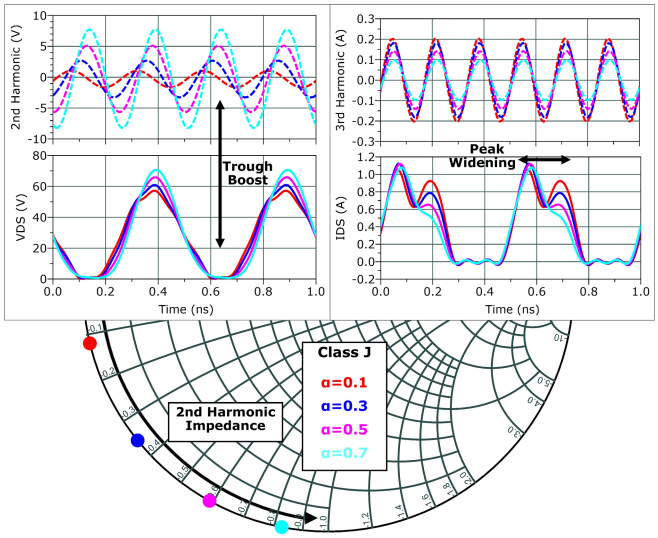

FIGURE 3. Impact of varying α for Class J mode on resulting intrinsic current and voltage waveforms, with a look at how the 2nd harmonic voltage gives the overall intrinsic voltage a trough boost to minimise knee clipping. This results in a current waveform with a narrower peak due to less 3rd harmonic content from reduced knee clipping at higher α values.

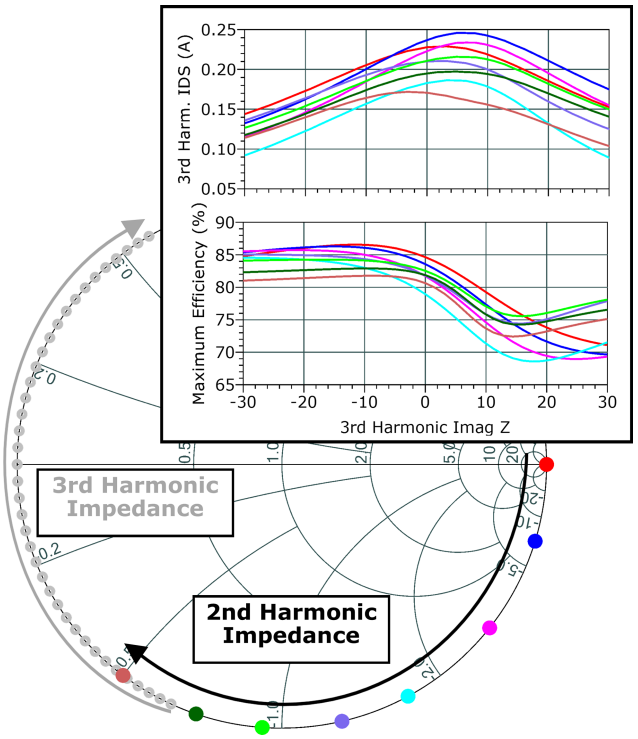

FIGURE 4. Effect of varying 3rd harmonic impedance between +/- 30 Ω on the 3rd harmonic content of the current waveform and maximum achieved efficiency.

efficiency for α values approaching zero for Class J, seen previously. In theory, the current waveform is typically assumed to be a half-rectified sinusoid with only even harmonic content [22]. However as demonstrated here, 3rd harmonic content within the current waveform can impact efficiency. To then examine the knee effect theoretically, a new definition of the current waveform is needed. However this becomes very complex as the amount of 3rd harmonic current has a multitude of dependencies, including input drive level, phase at which the voltage drops below the knee threshold and the impedance presented to the 3rd harmonic. To therefore arrive at a solution where high efficiency is maintained across a broad frequency range, a simple practical approach was taken in [23] where CCF^{-1} and Class J combined at particular α values to maintain high average efficiency. This approach is extended here in this article through some examination of the impact the 3rd harmonic impedance has on achievable efficiency.

B. THIRD HARMONIC IMPACT ON EFFICIENCY

In theory, for both CCF^{-1} and Class J modes, a perfect 3rd harmonic short is usually provided. In reality however, to provide this ideal short over a wide frequency band can be difficult. The 3rd harmonic impedance is therefore likely to vary when considering a broadband PA. As demonstrated previously, the amount of 3rd harmonic content in the current waveform can impact efficiency. However this was only studied for the case when the 3rd harmonic is perfectly shorted. For that reason, the impact the 3rd harmonic impedance has on efficiency needs to be examined. This is achieved through another harmonic balance simulation with the ideal impedances of both modes presented at the intrinsic plane of the Wolfspeed CGH40010F large signal model. This time however, for each combination of fundamental and 2nd harmonic impedance, the 3rd harmonic is swept fully around the edge of the smith chart at the intrinsic plane.

The impact of any variance of 3rd harmonic impedance is first examined on the amount of 3rd harmonic content within the current waveform, along with the maximum achieved efficiency for a range of 2nd harmonic impedances, shown in Fig. 4. By observing the 3rd harmonic content, this can give an indication of the amount knee clipping occurring. It shown that by terminating the 3rd harmonic with some imaginary impedance between -30 to -10 Ω, a lower amount of 3rd harmonic current is generated, along with a higher achieved efficiency. This is further demonstrated through plotting intrinsic efficiency contours for the 3rd harmonic impedance in Fig. 5. Again, these load pull contours show that improved efficiency can be achieved by offsetting the 3rd harmonic impedance away from the traditional short. However, the considerable significance to all of these observations is the feasibility of being able to achieve this particular combination of 2nd and 3rd harmonic impedances in practise, due to the natural rotation of 2nd harmonic into the 3rd harmonic design space.

To therefore confirm these observations over a frequency range of 2.1–3.2 GHz, this combination of modes with the 3rd harmonic impedance offset are then verified with a harmonic balance simulation, where for each frequency a different CM α value is chosen and the phase of the 3rd harmonic reflection coefficient is varied between -130° to -152°. The

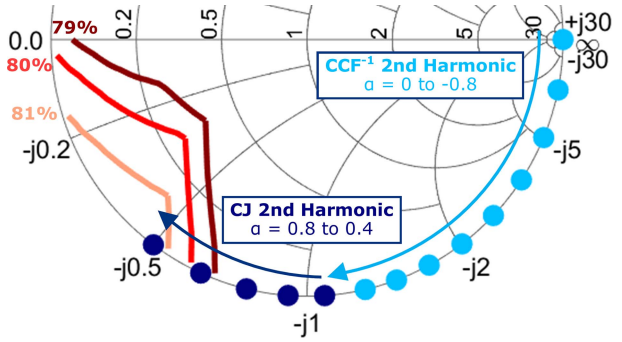

FIGURE 5. 3rd Harmonic intrinsic efficiency contours based on the plotted combination of 2nd harmonic impedances of Class J and CCF^{-1} at 2 GHz. Any 3rd harmonic impedance bound by the contour line guarantees an efficiency equal to or greater than that of the contour line, for all plotted 2nd harmonic impedances.

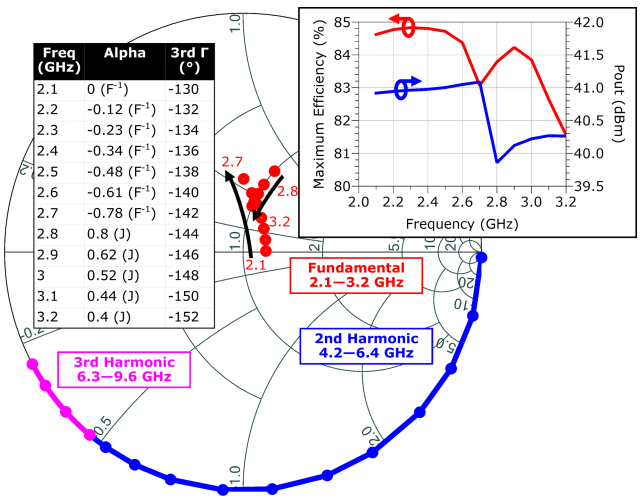

FIGURE 6. Proposed combination of Class J and CCF^{-1} modes between a fundamental frequency of 2.1 to 3.2 GHz, along with a 3rd harmonic impedance offset for improved efficiency. These target impedances are validated with a harmonic balance simulation with the results for drain efficiency and power plotted against frequency.

impedances presented over this frequency range and the resulting efficiency and power performance is shown in Fig. 6. These results show the benefits of using these harmonic impedances for efficiency performance. Therefore, the carrier amplifier within the DPA in this article is designed to these optimised CM harmonic impedances in an effort to achieve high BO efficiency.

C. DRAIN SUPPLY AS A DESIGN PARAMETER IN DPAS

When designing a DPA for asymmetrical operation, the amount of power the carrier and peaking PAs provide becomes unequal and therefore require a separate design. This means that careful considerations must be made on the optimum load which each PA is matched to, and supply voltages used for each PA. However, as will be demonstrated here, a consideration also needs to be made on how the supply voltage affects the quality factor of the required matching impedance. This is of particular importance when looking to maintain asymmetrical operation over a wide bandwidth. This can be achieved by means of the relationships between output power, optimum load and supply voltage. The average power generated by the PA can be calculated with the integral of the maximum voltage and current, namely

$$P_{avg} = \frac{1}{T}\int_0^T V_{avg}\sin(\omega_0 t)\cdot I_{avg}\sin(\omega_0 t)dt \tag{5}$$

where $\omega_0 = 2\pi f_0$ is the angular frequency of the RF carrier. By solving this integral, the optimum load in relation to voltage and power can be represented as

$$R_{opt} = \frac{(V_{supply} - V_{knee})^2}{2\cdot P_{avg}} \tag{6}$$

By rearranging this optimum load equation, the required supply voltage for a given load and output power can be obtained as follows

$$V_{supply} = \sqrt{2R_{opt}P_{avg}} + V_{knee} \tag{7}$$

These equations will be employed in the design of the DPA in Section III where a specific optimum load will be specified based on a particular output power level for the carrier and peaking amplifiers. Based on this optimum load the required supply voltage can then be determined.

Packaged devices tend to have a significant amount of parasitics between the intrinsic plane and the external package plane. When considering different intrinsic load values, these parasitics cause a large impedance transformation at the transistor package plane. It is therefore important to understand the impact that these package parasitics will have on the quality factor of a match and the ability to maintain a particular load over a given bandwidth. With previous works such as in [17] the optimum load proposed at BO is greater than 200 Ω, which can greatly increase the quality factor of the match required. This means it can be difficult to maintain the target load over the full frequency band of the PA, either causing early compression of the carrier PA, or no compression at all. This can be inferred from measured efficiency and gain plots, where at particular frequencies there is no gain compression at BO along with low efficiency, indicating a lower intrinsic load than required at that particular BO power level. This typically occurs at the extremes of the PAs operating frequency band, with evidence of this non-optimal BO intrinsic load seen in other reported CM PM DPAs [13], [14], [15], [16].

Here, the quality factor of the required match is examined based on different supply voltages. This is done by calculating the required optimum loads at different supply voltages for a peak output power of 10 W, with a back off power level of 3.5 W, which are both typical of the DPA designed for this article. The package parasitics are then embedded to observe the required package impedance needed between 2.1–3.2 GHz, to achieve the intrinsic optimum load. The required intrinsic and package impedances for different supply voltages at the power levels stated previously are plotted in Fig. 7, along with

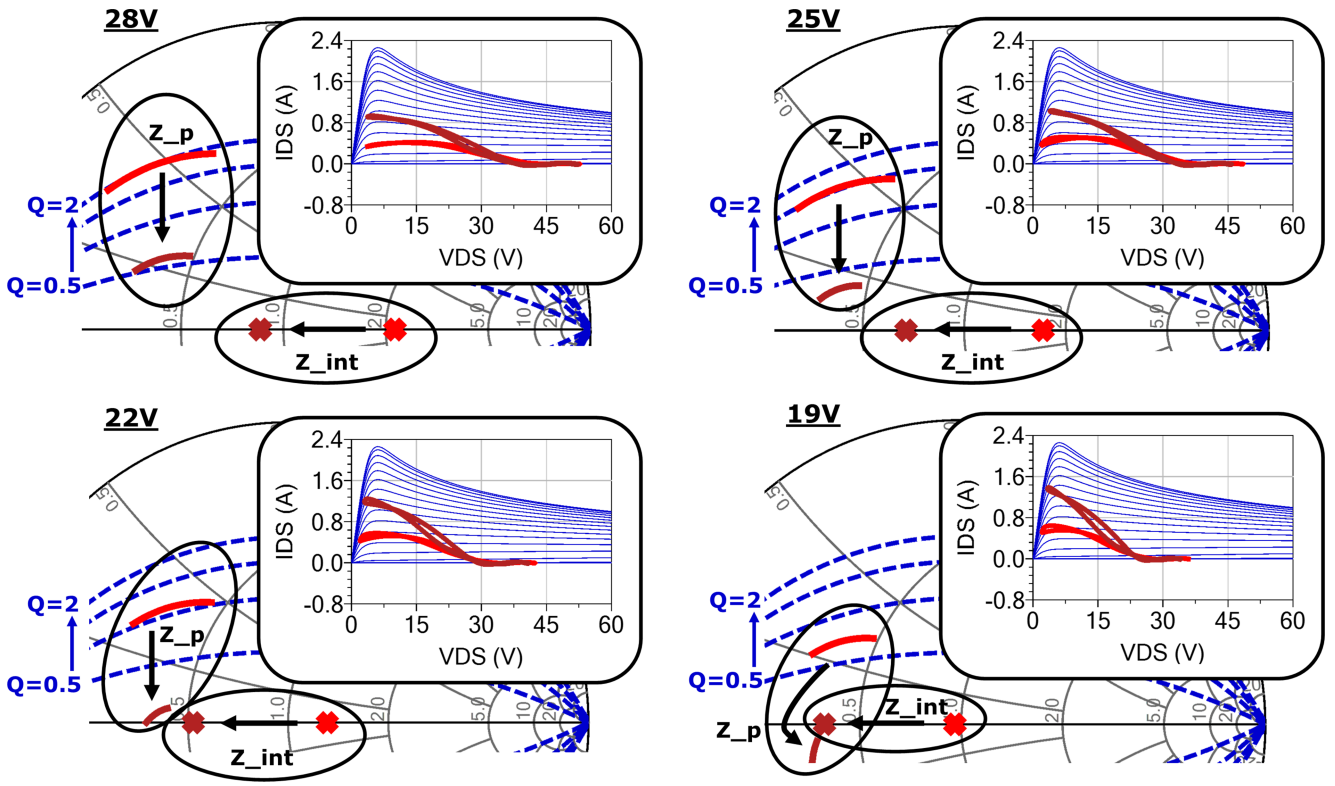

FIGURE 7. Required impedance transformation at the package plane, Z_p, and intrinsic plane, Z_{int}, for different supply voltages for a power output of 3.5 W at BO (red) and 10 W at POP (brown). It is shown that by reducing the supply voltage, and in turn reducing the required intrinsic load value, the quality factor of the required package impedance transformation can be reduced.

the Class B loadline for each power value in each case. It is shown that by reducing the supply voltage, and in turn reducing the required intrinsic load value, the quality factor of the required package impedance transformation can be reduced. As stated previously, R_{opt} values at BO in literature have been seen to range anywhere from 100 and 200 Ω, therefore potentially reducing the ability to maintain a given intrinsic load. Any variance in load can either cause early compression with less output power, or less compression and therefore a loss in efficiency. Another issue with an unbalanced intrinsic load is the difference in peaking gate voltage needed to allow the carrier PA to go into compression, which could become a varying quantity with frequency. In this article a lower supply voltage is used for the carrier PA to better maintain a given intrinsic load, in an effort to improve efficiency performance.

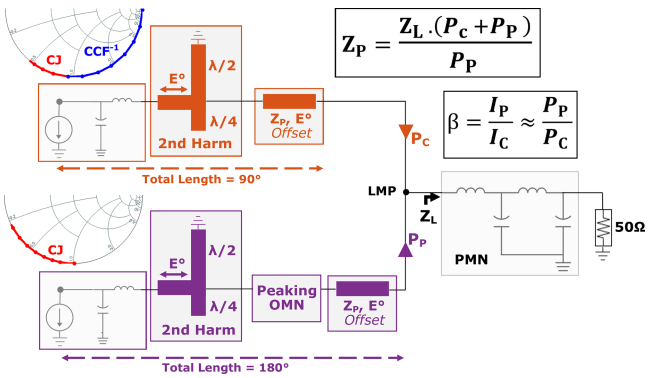

FIGURE 8. Overall schematic of the PM technique used, along with impedance buffers for 2nd harmonic harmonic loading and target 2nd harmonic impedances for both carrier and peaking PAs. The carrier branch is highlighted in orange and the peaking branch in purple.

D. ASYMMETRICAL CM DPA DESIGN PROCESS

The block diagram for the asymmetrical Post Matching (PM) technique used in this article is shown by Fig. 8. PM is a well known technique for improving bandwidth, achieved through the replacement of the impedance inverter and transformer within a traditional DPA. Impedance inversion for the carrier amplifier is implemented by absorbing device parasitics along with an offset line to ensure impedance inversion at the Load Modulation Point (LMP). Impedance transformation is then achieved through the Post Matching Network (PMN) which is then used to provide an impedance Z_L at the LMP. As demonstrated previously in [24] and [15], maintaining the carrier and peaking networks to the minimum length of 90° and 180° respectively can ensure best possible bandwidth performance. To meet these criteria of phase for both carrier and peaking networks, an offset line of impedance Z_P is added to both branches, also shown by Fig. 8. The same impedance is used for both lines to avoid discontinuity in line

width, making conversion from schematic modelling into EM simulations easier. As in [6] and [8], a component termed β is defined as the current ratio of the carrier and peaking branches leading into the LMP. In this article this is approximated by the ratios of power being delivered by the carrier and peaking PAs.

The main novelty of the PM approach taken in this article is that optimised harmonic impedances defined previously, which are used for both PAs. For harmonic matching, impedance buffers are used as in [25] then later in [26] with the design of a CCF PA, where in this article only the 2nd harmonic is matched. This ensures that the 2nd harmonic is properly loaded close to the device to ensure optimum efficiency performance, whilst also minimising electrical length added between the device and LMP, which can also greatly impact bandwidth performance. As also demonstrated by Fig. 8, a combination of Class J and CCF^{-1} is used for the carrier PA, whilst Class J is used for the peaking amplifier. A higher supply voltage will be used for the peaking PA, where using this class of operation within a given range of α values can still generate good efficiency, but also limit the peak intrinsic voltage from overreaching the breakdown voltage. Another novelty is a simplified design process for the design of a PM DPA, which is summarised below. With PM it can be complex to analytically solve the required impedances of all matching networks, such as the co-design proposed by [5]. It is also difficult to achieve the required phase delay needed in the carrier circuit for impedance inversion over any significant bandwidth. This can result in imperfect impedance inversion with frequency, where low-order impedance inverters are used in [3] to alleviate this issue. This therefore makes maintaining any specific optimum impedance difficult over bandwidth. For that reason the power ratio becomes a frequency dependent quantity. However, various circuit parameters around the different carrier and peaking circuits rely heavily on the current ratio β. It can therefore become a complex problem to find analytically these impedances. In this article a simple design flow is proposed which can deliver a wideband DPA with high BO drain efficiency. This process will be further expanded on with the design of a DPA combining continuous modes with the post matching technique in Section III. The summarised steps are as follows:

1) Overall circuit diemnsions are calculated, particularly the maximum power delivery of the carrier and peaking PAs, such that the the PMN Z_L is defined and Z_P can be calculated.
2) The next process is to add an impedance buffer for harmonic matching to the carrier amplifier along with the required delay line to achieve the necessary 90° for impedance inversion when connecting into the LMP and PMN.
3) A load pull is then conducted on the carrier amplifier circuit including the harmonic match and impedance inversion to find the optimum frequency-dependent impedance the PMN needs to present to carrier amplifier for best efficiency performance at BO.

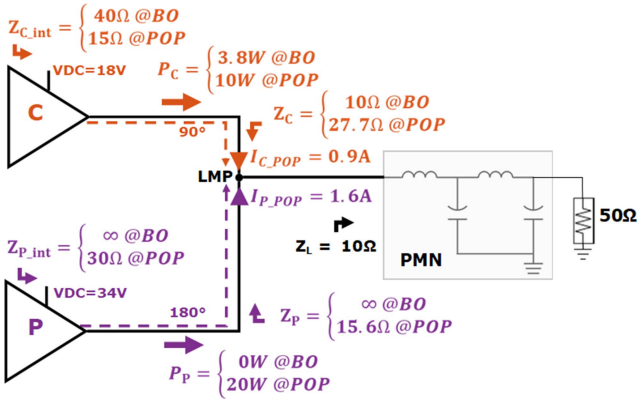

FIGURE 9. Post matching diagram of calculated impedances, supply voltages, power and currents. The two impedances cases correspond to peak output and backoff power.

4) Once the carrier amplifier and PMN has been designed, the impedance which is presented to the peaking amplifier at the LMP is calculated. This is based on an estimated frequency-dependent current ratio taken from the simulated measured current from the carrier amplifier at the LMP. This impedance is then used to design the peaking amplifier for best efficiency performance.

III. DESIGN PROCEDURE FOR A POST MATCHING CONTINUOUS MODE DOHERTY PA

A. CIRCUIT SPECIFICATIONS AND DIMENSIONING

Before proceeding with an accurate design, the overall DPA design specifications, i.e. output power, current, supply voltages, are determined. For this design, the DPA is designed to provide a peak power of 45 dBm with an efficiency peak at 9 dB BO. For peak power, the total power is split between 10 W for the carrier and 20 W for the peaking, resulting in a total of 30 W. For the carrier, the CG2H40010F is chosen as 10 W is needed at POP. The datasheet of the CG2H40010F specifies that it can deliver a saturated power of 17 W [27], where a slightly higher supply voltage can be used to achieve the required 20 W. To avoid any additional parasitics associated with a larger device, and therefore the reduction in bandwidth performance that could cause, the CG2H40010F device is also chosen for the peaking PA. Based on the defined split of power at POP between carrier and peaking PAs, the power ratio β is determined to be 1.8. At BO, the carrier amplifier needs to deliver 3.8 W (35.8 dBm). Using these defined metrics, the various impedance, drain supply and power values can be calculated for both amplifiers, shown by Fig. 9.

For the PMN, a Z_L of 10 Ω was chosen which is close to the optimum package impedance of a load pull of Class J impedances. With this Z_L value and using the current ratio $\beta = 1.8$, at POP the impedance the carrier sees looking into the LMP becomes 27.7 Ω whilst the peaking amplifier sees 15.6 Ω. Based on these calculated impedances, and the power defined previously at POP, the carrier and the peaking will provide a peak current respectively of 0.9 and 1.6 A to the

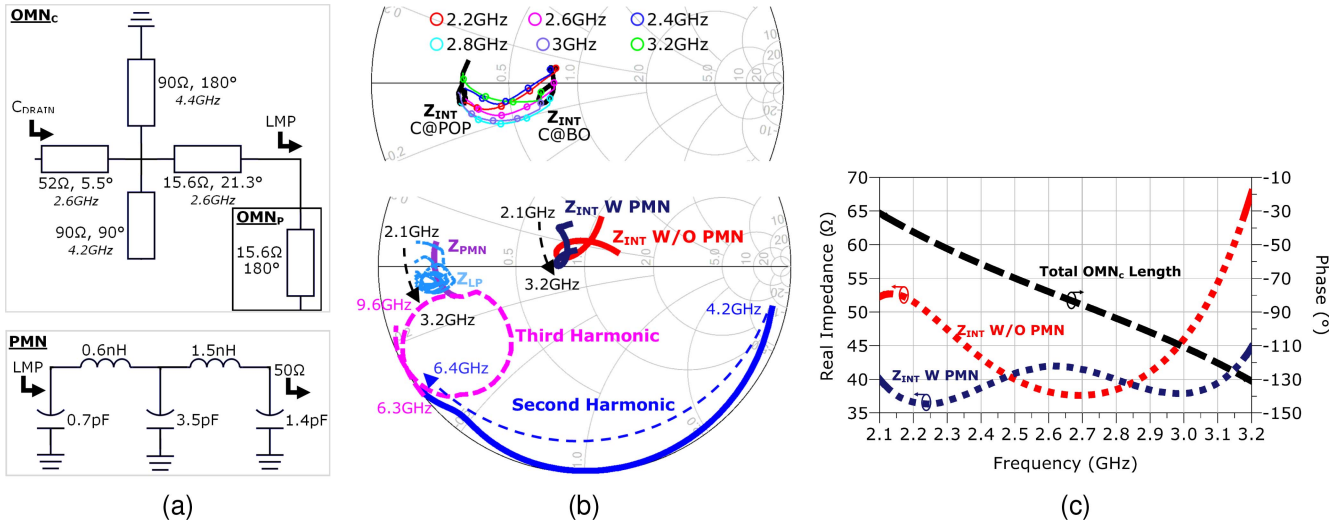

FIGURE 10. (a) Carrier harmonic stub and inversion circuit, with peaking approximation in the square box, and PM circuit. (b) Smith chart of first, 2nd and 3rd harmonic response, including load modulation between BO and POP, along with load-pull contours of efficiency greater than 75% for PMN impedance (c) Carrier OMN length in degrees and intrinsic resistance with and without PMN.

LMP. As mentioned previously, reducing the optimum load needed at BO can help reduce the quality factor of the match needed. An intrinsic R_{opt} of 40 Ω is therefore chosen which provides room for any later modulation into lower resistance values at peak power without drawing more current than the transistor can supply. Taking this R_{opt} value and the power at BO, a drain supply of 18 V is calculated. Based on this supply voltage and a peak delivery of 10 W for the carrier, the intrinsic R_{opt} will be modulated to 15 Ω. For the peaking amplifier a drain supply of 34 V is chosen which along with the peak power of 20 W results in an R_{opt} of 30 Ω.

B. CARRIER AND PMN DESIGN

Once all circuit values have been calculated, the next step is the co-design of the carrier amplifier along with the PMN, with the first process being to match the 2nd harmonic. As demonstrated in this article, it can be beneficial to combine CCF^{-1} and Class J modes. The harmonic response between 2.1–3.2 GHz proposed earlier in this article is the target impedances for high efficiency. These impedances are achieved by adding an impedance buffer with a combined 180° shorted stub and a 90° open stub. A series line is tuned, along with the length the stubs, to provide the appropriate 2nd harmonic response. The stubs used and resulting harmonic response are shown in Fig. 10. The 3rd harmonic response once the carrier PA is loaded by the PMN is also shown to fall within the region needed for high efficiency. The next step is then to add a delay line to achieve the necessary 90° for impedance inversion when looking into the LMP and PMN. This line has a characteristic impedance of 15.6 Ω which matches the impedance the peaking amplifier sees looking into the LMP. This allows for continuity in width of the two lines combining at the LMP. The length is then tuned until 90° is achieved at the center frequency, as shown by Fig. 10. The next step is to then perform a load pull to find the impedances the PMN needs to match to for best BO efficiency performance. Before doing so, an approximation of the peaking amplifier is made with a 180° stub, thus avoiding the need to design the peaking amplifier first, but still allowing the effect it has on the intrinsic impedance to be observed during a load pull. The carrier output matching network along with the peaking network approximation is shown by OMN_C in Fig. 10(a). The resulting efficiency contours from a load pull of the OMN_C circuit is shown in Fig. 10(b). ADS' matching tool is then used to design a PMN filter to match these load pull contours to 50 Ω. The resulting effect on the carrier intrinsic impedance once the PMN is included is seen on a Smith chart in Fig. 10(b), along with the impedance being presented by the PMN. Finally, the effect the PMN has on the intrinsic resistance is shown in Fig. 10(c). This shows that the PMN has helped match the intrinsic impedance closer to the desired intrinsic R_{opt} of 40 Ω. The resulting intrinsic waveforms of the carrier PA at different frequencies once connected with the peaking PA in a harmonic balance simulation are shown by Fig. 11(a).

C. PEAKING DESIGN & COMBINATION

The final step in the design process is to design the peaking amplifier. Similar to before with the carrier, the 2nd harmonic is first matched with a combination of a 180° shorted stub and a 90° open stub. A series line is tuned, along with the length the stubs, to provide the appropriate 2nd harmonic response. The aim was to maintain the second harmonic within the Class J mode, where CCF^{-1} can cause a much higher voltage, which could potentially exceed the breakdown voltage with the high supply voltage being used for the peaking. The stubs used and resulting harmonic response are shown in Fig. 12. The next step is to then match the peaking amplifier to the load

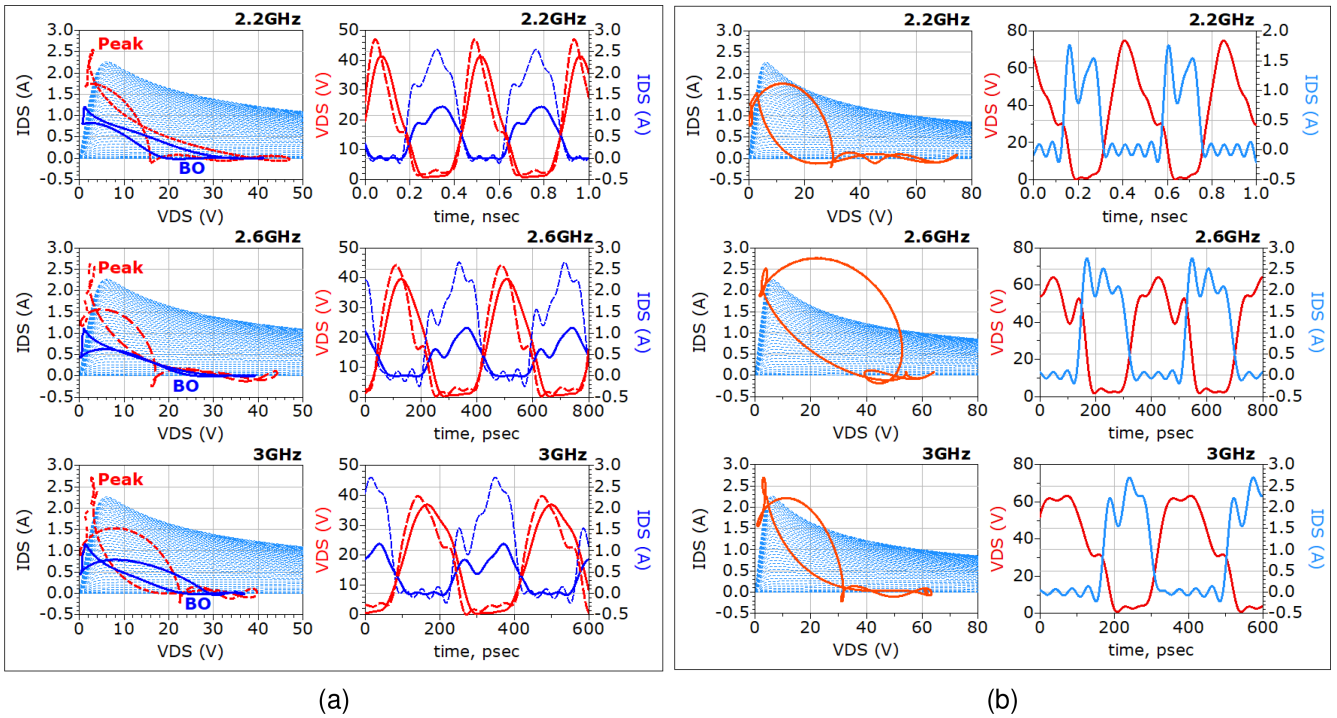

FIGURE 11. (a) Carrier amplifier intrinsic waveforms at BO and POP, with loadline waveform shown to the left and with VDS and IDS shown to the right. (b) Peaking amplifier intrinsic waveforms at POP, with loadline waveform shown to the left and with VDS and IDS shown to the right.

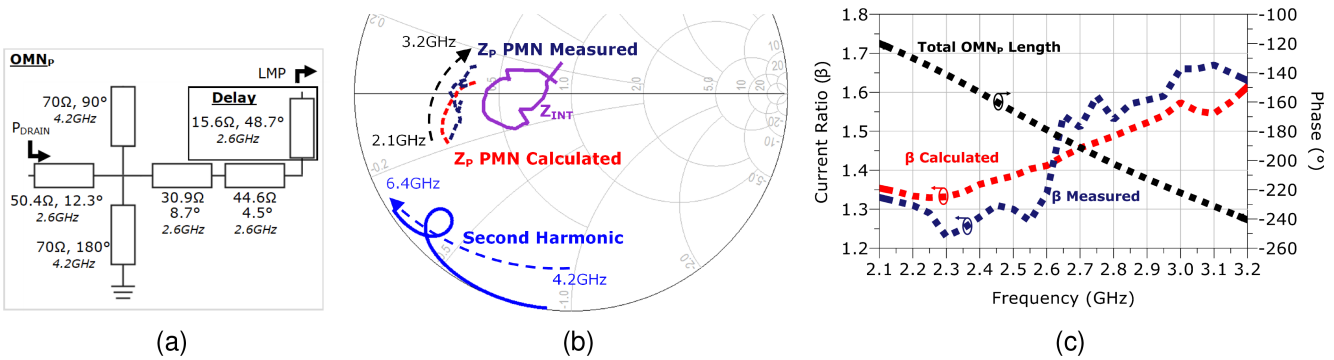

FIGURE 12. (a) Peaking matching circuit with harmonic stubs, matching and delay line. (b) Smith chart of fundamental and 2nd Harmonic response along with PMN impedance presented to peaking PA. (c) Peaking OMN length and calculated and measured power ratio β.

presented by the PMN at the LMP. To do this, a frequency dependent impedance presented by the PMN can be derived by calculating the frequency dependent power ratio. This is achieved by measuring the current delivered by the carrier amplifier into the LMP in simulations, along with assuming the the current delivered by the peaking PA into the LMP is to be 1.6 A, as calculated previously. The resulting calculated impedance presented by the PMN to the peaking PA is shown on a Smith chart in Fig. 12(b), based on the calculated power ratio, as shown by Fig. 12(c). The same figures shows the simulated power ratio and the PMN impedance presented to the peaking PA from a harmonic balance simulation with the combination of the peaking and carrier PAs into a DPA. This shows good agreement with the calculated values, demonstrating the design method has good predictability of the load to design the peaking PA once the carrier PA has been designed.

Once the PMN impedance has been calculated, the peaking OMN is designed to match an intrinsic impedance of 30 Ω to this PMN load. This OMN also features the addition of a delay line to achieve the necessary 180° to provide as much of an open circuit as possible to the carrier amplifier. This line has a characteristic impedance of 15.6 Ω which matches as close as possible the impedance the peaking amplifier sees looking into the LMP such that it has minimal effect on the match. The length is then tuned until 180° is achieved at the center frequency, as shown by Fig. 12(c). The designed

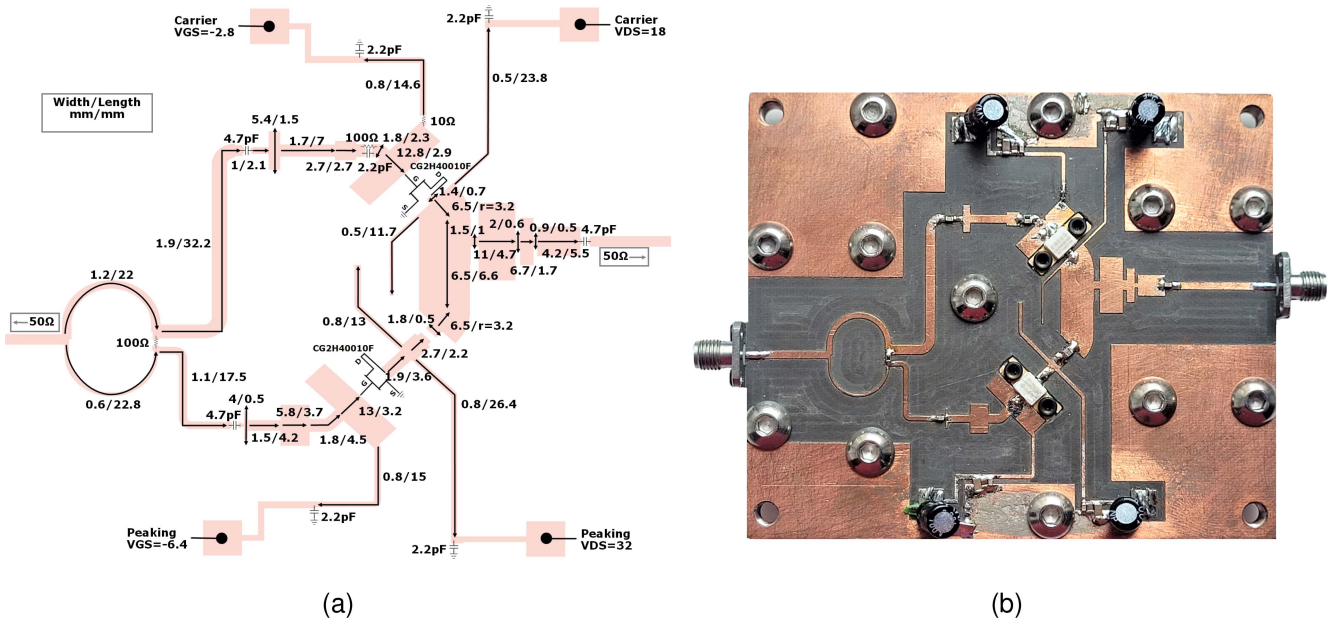

FIGURE 13. (a): layout of the PA prototype with component values and microstrip width/length annotated on it. (b): photo of the fabricated PA.

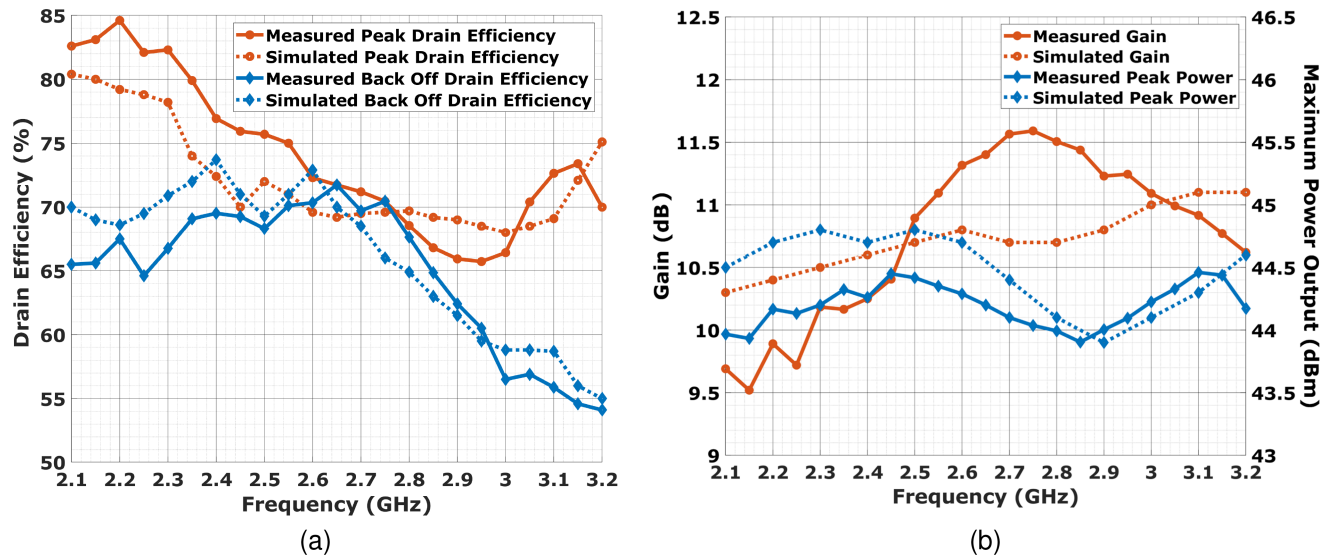

FIGURE 14. (a) Measured and simulated CW peak and BO drain efficiency performance vs. frequency, (b) measured and simulated CW maximum power output at -1 dB compression and small signal gain vs. frequency.

peaking OMN is shown by 12(a), with the resulting intrinsic impedance shown on a Smith chart of Fig. 12(b) and intrinsic waveforms at different frequencies shown by Fig. 11(b).

The final step is to then combine both carrier and peaking amplifiers into a DPA with a single harmonic balance simulation. The input of both amplifiers are matched and a Wilkinson divider is used to split the input power to both amplifiers. A delay line is added to the carrier input match to account for the extra electrical length in the peaking amplifier. This delay line is tuned until carrier and peaking currents align in phase at the LMP. The layout is then converted to microstrip components and then electromagnetically simulated, where the output match is optimised for output power, BO drain efficiency and peak drain efficiency. The final electromagnetically simulated layout is shown by Fig. 13(a). The drain efficiency resulting from an harmonic balance simulation is then shown by Fig. 14. The simulated BO drain efficiency varies between 55–74.8 % with an average of 66 %. The drain efficiency at POP varies between 68–80.4 % with an average of 72.3 %.

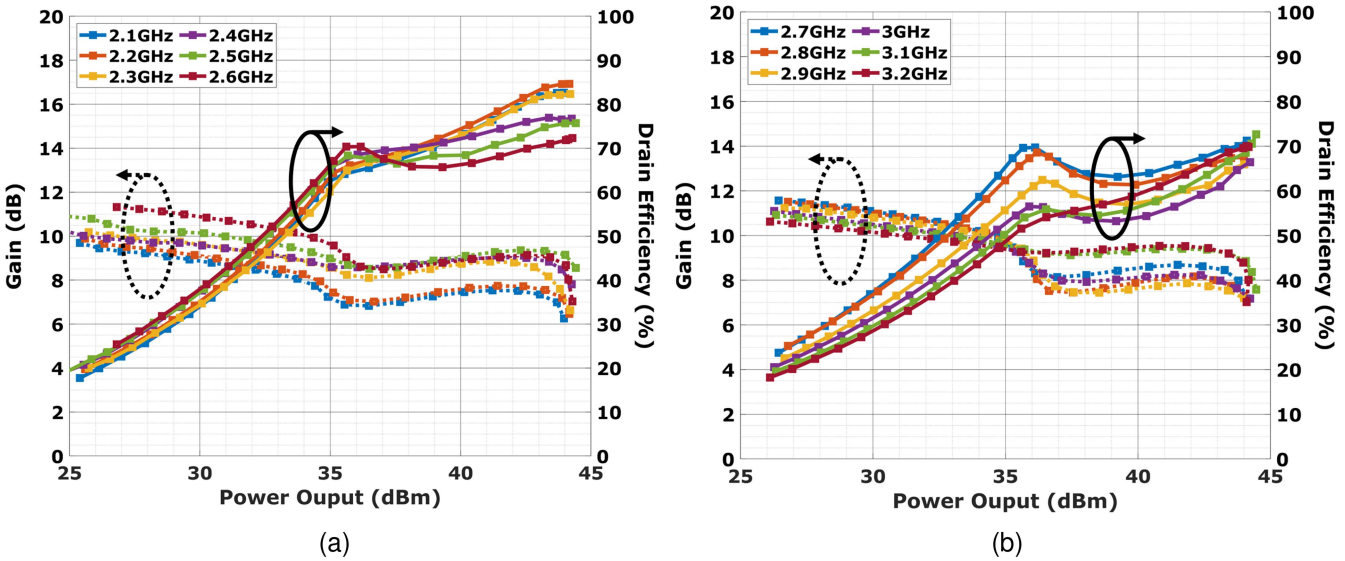

FIGURE 15. Measured CW drain efficiency and gain vs. output power, (a) 2.1–2.6 GHz and (b) 2.7–3.2 GHz

IV. EXPERIMENTAL RESULTS

The fabricated PA is shown in Fig. 13(b) and its size is 83 mm × 103 mm, using Rogers RT/duroid 5880 with 0.51 mm thickness. The PA is mounted on an aluminium heat sink to dissipate heat during operation. During measurements the carrier amplifier is supplied with a drain voltage of 18 V and a biased with a quiescent current $I_q = 40$ mA. The peaking amplifier is supplied with a drain voltage of 32 V and a gate voltage of −6.4 V which was experimentally found to ensure good BO performance. Both continuous-wave (CW) and modulated signals were used to characterise the PA, and the results are shown in this section. Digital Pre-Distortion (DPD) was also applied with modulated signals to demonstrate the ability to linearise the PA with a conventional DPD.

A. CW MEASUREMENTS

A CW measurement setup was built with with an RF signal generator (Keysight N5183B) and a 35 W driver (Empower 1178BBM58CGM) connected to the PA input. The PA input power is sensed with a coupler (Mini-Circuits ZUDC20-0283) and a power meter (Rohde & Schwarz NRP-Z18) while the PA output power is directly measured with another power meter (Rohde & Schwarz NRP-Z23) with an embedded attenuator. Scalar calibration of the test setup was performed at frequency steps of 50 MHz and power steps of 1 dB. This calibration was performed with power steps to ensure any variation in the driver amplifier was accounted for. Fig. 14(a) shows the comparison of simulated and measured drain efficiency at peak and at BO power with respect to frequency. The PA operates between 2.1 and 3.2 GHz with an average peak drain efficiency of 73.9 % across the bandwidth, with the maximum achieved of 84.9 %. The measured average efficiency achieved at between 8–9 dB BO across the bandwidth of the PA was found to be 64.7 %. Both Fig. 15 shows power sweeps of gain and drain efficiency vs. output power across the bandwidth of the PA at 50 MHz intervals.

The PA achieves a maximum power output of between 43.9–44.5 dBm and a small signal gain of between 9.5–11.6 dB. These are also shown by Fig. 14(b). There is some difference in the simulated and measured efficiency performance which can likely be attributed to the large signal model only being validated for a supply of 28 V, seen in Wolfspeed's documentation [27].

B. MODULATED SIGNAL MEASUREMENTS

After CW validation, the next step was to test the PA with a complex modulated signal such as Long Term Evolution (LTE) downlink signals which typically present a high PAPR. The presented DPA is designed to be highly efficient and therefore presents a non-linear gain characteristic and so DPD is beneficial to achieve linear operation. For this, a 60 MHz carrier-aggregated signal is generated in Matlab with a combination of three 20 MHz channels. The total PAPR of the signal was 9 dB and the same 60 MHz signal is then used to test the PA at three different frequencies (2.2, 2.6, and 3 GHz). The DPD is implemented with a simple Generalized Memory Polynomial (GMP) and has a polynomial order of 11, a memory order of 3, and symmetrical lead and lag memory order of 3.

Three different plots were used to demonstrate the PAs linearity before and after DPD: Amplitude Modulation/Amplitude Modulation (AM/AM), AM/Phase Modulation (AM/PM) and power density spectrum plots. The measurement results are shown in Fig. 16. Here, the AM/AM and AM/PM plots are shown by (a) and the power density spectrum plots shown by (b). When DPD is not used, an Adjacent Channel Power Ratio (ACPR) of between 28.4–29.4 dBc was measured. Once linearised, the PA achieved an ACPR of

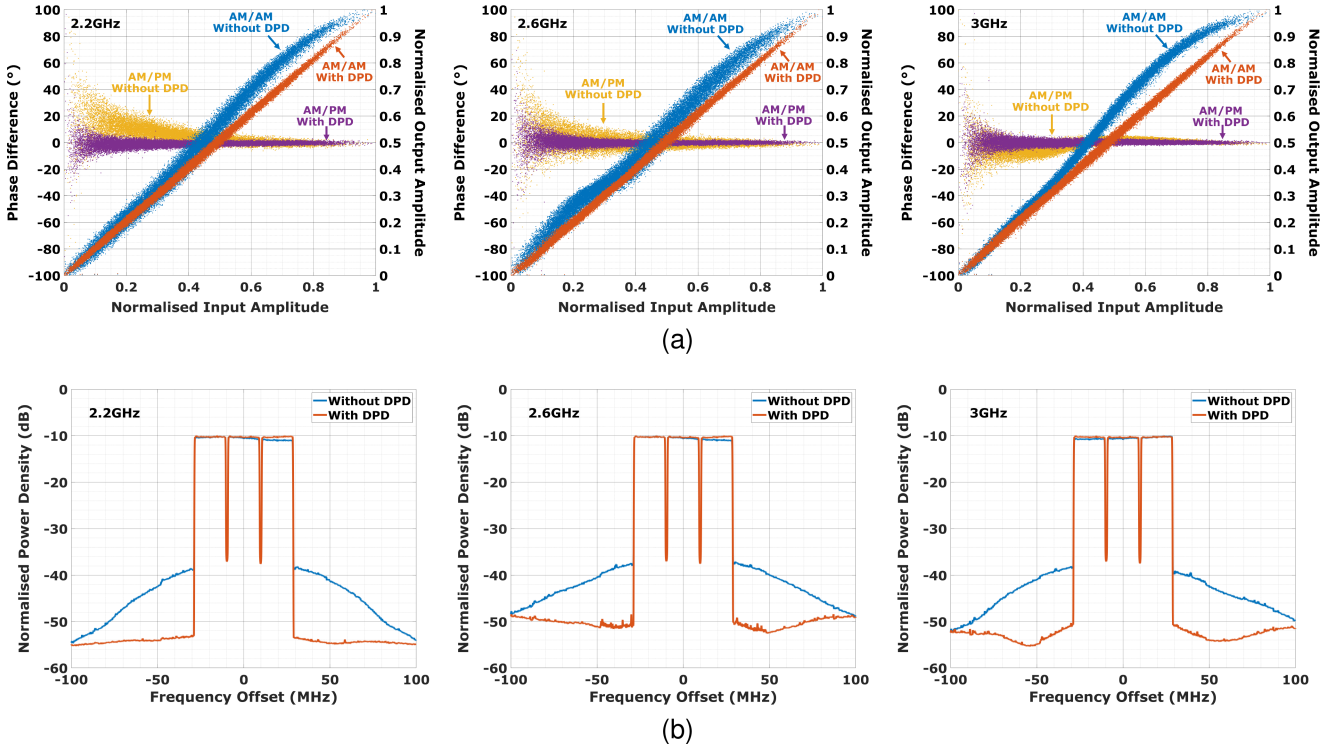

FIGURE 16. AM–AM and AM–PM (a) and output spectrum (b) of tested PA with and without DPD with a 60-MHz LTE signal at 2.2, 2.6, and 3 GHz.

TABLE 1. Comparison of State-of-the-Art High BO Wideband PAs

Ref	Technique	Freq (GHz)	FB (%)	Psat (dBm)	Gain** (dB)	Peak AE* (%)	BO AE* (%)	Signal (MHz/ PAPR[dB])	DEavg (%)	ACPR w. DPD (dBc)
[5]	PM DPA	1.9-2.4	23	44.2-49.7	11-14.2	60.4	47.6	20/9	44.2-49.7	-49.2 ∼ -50.3
[6]	PM Aysm DPA	1.55-2.35	41	43.7-45.2	8.2-10.6	62	53.1	5/8.3	-	-50.3
[7]	PM DPA	1.6-2.2	32	45.8-46.6	14.8-17	66.5	53.4	20/9.1	50.2-53.1	-48 ∼ 52
[8]	PM DPA	1.6-1.9	17	42.2-42.8	9.9-11	80	46.1	5/9.6	-	-53.3
[13]	DPA with Class J	3.3-3.75	13	48-48.8	11.8-13.5	63.9	50.1	40/8	53	-
[17]	Aysm DPA	1.8-2.6	36	44.8-45.2	8.2-13.2	61.4	57.2	20/7.6	-	-45
[30]	Modified DPA	1.35-2.05	41	41.5-42.4	11.8-14.1	70.6	53.4	40/8.9	50-53	-46.5 ∼ -51
[31]	SPA-Doherty	2-2.7	30	40-41	8-14.2	65	57.4	20/8.2	48	-39.2 -41.5
[32]	DPA-like	1-3	100	43.9-45.2	12.1-13.1	66.8	44.4	20/9	-	-48.4
[28]	3 Stage DPA	1.6-2.6	48	45.5-46	9.1-11	59.4	51.9	20/9	52-56	-54 ∼ -56
[29]	DPA Modified LM	1.4-2.5	56	44-45.9	12.1-16.3	67	48.8	60/9	47.4-53.5	-45.5 ∼ -47.4
[33]	DPA Phase Comp.	2.05-2.8	30.9	43.9-44.9	10.1-15.5	70.5	44.5	20/9	41	-45.1
This Work	Asym DPA CM PM	2.1-3.2	42	43.2-44.4	9.5-11.6	73.9	64.7	60/9	52.1-64.3	-42.2 ∼ -44.1

*Read from data points on graphs to obtain the mean, **Gain is small-signal gain

between 42.2–44.1 dBc with an average drain efficiency of 52.1–64.3 %.

C. PERFORMANCE COMPARISON WITH STATE OF THE ART

The performance of the presented DPA is compared with other published high-BO PAs in Table 1 available in the state-of-the-art literature. As it can be seen from Table 1, the proposed combination of continuous modes and post matching technique shows its benefits in considerable efficiency performance of 73.8 % at saturation and of 64.7% at 8–9 dB BO, whilst this DPA is also capable of maintaining broadband performance with a fractional bandwidth of 42 %. To the best of the author's knowledge, the proposed CM-DPA shows the highest average drain efficiency at BO currently in the literature. Some works such as [28] and [29] have been able to achieve even higher fractional bandwidths of between 48–57%, though their average BO drain efficiencies can be more than 10 % lower, i.e. 49 to 52 %, in comparison to the presented DPA. The use of continuous modes, and in particular the specific combination of Class J and CCF^{-1} modes, has allowed this high BO drain efficiency to be achieved. Additionally, by exploiting the drain supply to change optimum load values, much higher performance has been able to be achieved over a wider bandwidth.

V. CONCLUSION

This article presents a simple design methodology for an asymmetrical DPA using continuous modes and the post matching technique to achieve great BO performance whilst maintaining broadband operation. Analysis was provided on how the knee effect can reduce the effective performance of Class J and Continuous Inverse Class F modes. An optimum combination of 2nd and 3rd harmonic impedances as proposed for the carrier PA which can minimise this knee effect impact on efficiency performance. Also, it is shown how the drain supply can be used to improve the bandwidth over which can intrinsic optimum load can be maintained. The presented design procedure was verified in the design and manufacture of a prototype DPA using the Wolfspeed CG2H40010F GaN HEMT. The realised PA operates between 2.1–3.2 GHz with a peak power output of between 43.9–44.5 dBm. The PA achieved a high average drain efficiency of 64.7 % at 8–9dBs of BO. When tested with a 60 MHz LTE modulated signal with 9 dB PAPR, a drain efficiency of between 52.1–64.3 was achieved. Once digital predistortion was applied, the ACPR was reduced to between −42.2 and −44.1 dB.

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