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High-Efficiency 200-GHz Neutralized Common-Base Power Amplifiers in 250-nm InP HBT

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ABSTRACT The analysis, design, and measurement of two Indium Phosphide (InP) heterojunction bipolar transistor (HBT) power amplifier (PA) designs are presented at G-band with record efficiency. A pseudo-differential common-base (CB) stage with neutralization capacitors and low-loss coupled-line balun (CLB) improve the gain and reduce matching loss. A single-stage design achieves 8.3 to 12.7-dBm output power and 7.7 to 17.3% power-added efficiency (PAE) over 180 to 220 GHz. The use of compact baluns allows the design to occupy only 0.011mm^2 with power density of 1.69 W/mm^2. A 3-stage, 4-way power-combined PA delivers 16.6 to 19.7-dBm output power and 6.5 to 13% PAE over 185 to 210 GHz.

INDEX TERMS InP, millimeter-wave, G-band, power amplifier.

I. INTRODUCTION

G-band (140–220 GHz) has been proposed for automotive radar and future backhaul communication systems in recent years due to the high resolution for imaging and wide available bandwidth for backhaul communication [1], [2]. While the wavelength at G-band constrains antenna spacing to 0.68 mm at 220 GHz in a phased array, critical front-end components such as power amplifiers (PA), low-noise amplifiers, phase shifter, and switches must also be compact while operating at high efficiency. In [3] and [4], the trend of published array element size larger than λ/2 above 70-GHz is observed. While RF circuits benefit from the reduced passive area at higher operating frequency, additional gain stages are required due to the reduced available gain per stage and the area of front-end components remains large. Moreover, efficiency is also placed at a premium since power density is proportional to the square of operating frequency if the output power per element is fixed. For instance, P_{sat} of 17 dBm is a typical power level and 20% peak efficiency in an element of 5G 28-GHz phased array [5]. This implies that the DC power density of 0.87 W/cm^2 at 28-GHz. If we consider the same output power and efficiency at 220-GHz with λ/2 constraint, the DC power density will increase to 54.1 W/cm^2, demanding active cooling. Therefore, a high-efficiency PA at G-band is required to constrain the power density.

Several G-band PAs have been published over the past few years. Bulk or SOI CMOS processes have limited f_T/f_{max} as well as low supply voltage. In [6], [7], output power and PAE of CMOS PAs are below 10-dBm and 8%. PA designs in SiGe HBT processes have shown decent power gain with multi-stage design and high output power with power combining at lower G-band range [8], [9] but the efficiency is limited to single digits above 200 GHz [10], [11]. Compared to the SiGe HBT, the 250-nm InP HBT process has superior collector-emitter voltage breakdown, higher f_{max} for G-band PAs, and higher output power with higher small-signal gain across 140-220 GHz [12], [13], [14], [15], [16], [17]. InP HEMT or GaN HEMT are processes that can achieve high f_T/f_{max} but PA performance at G-band is still not competitive compared to SiGe or InP HBT due to increased loadline matching conditions [18], [19], [20].

In [21], we demonstrated a single-stage 180-220-GHz PA using neutralized CB design with 17.3% peak PAE in Teledyne 250-nm InP HBT process. In this expanded paper,

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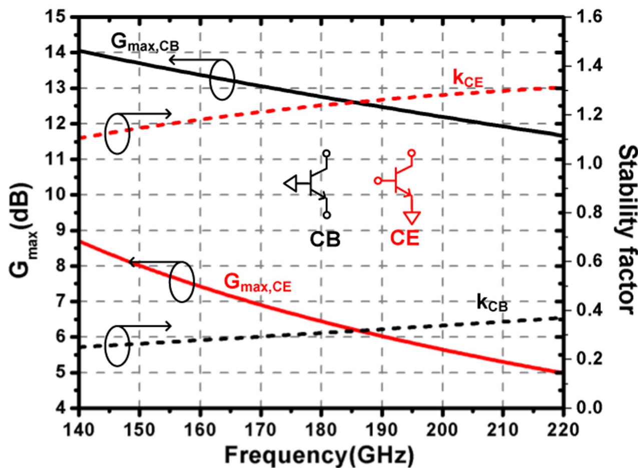


FIGURE 1. G_{max} (solid) and stability factor (dashed) of CE and CB at G-band.

TABLE 1. Simulated Parameters of CE and CB at 220 GHz

Simulated Performance at 220 GHz	CE	CB
G_{max}	5 dB	11.7 dB
Stability factor	1.3	0.4
Peak PAE	38.3 %	35.1 %
$Z_{S,opt}$	21+j*11.2 Ω (VSWR=2.5)	38-j*25 Ω (VSWR=1.9)
$Z_{L,opt}$	77+j*182 Ω (VSWR=10.7)	27+j*93 Ω (VSWR=8.7)
P_{out} @ PAE_{peak}	12.5 dBm	11.6 dBm
S_{21} @ PAE_{peak}	3.5 dB	7.6 dB
Peak PAE with 1-dB output matching loss	25.5%	26.9%
Peak PAE with 1-dB input and output matching loss	20.7%	25.5%

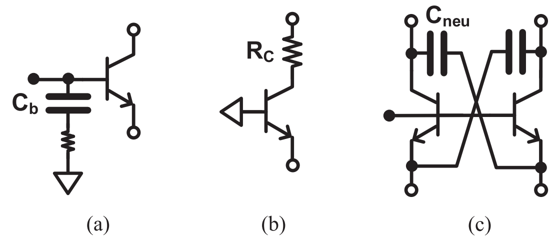


FIGURE 2. (a) Sized C_b CB stage. (b) Collector series-resistor CB stage. (c) Neutralization capacitor CB stage.

the analysis and design details are expanded along with the demonstration of a 3-stage, 4-way power-combined PA in G-band to provide a comprehensive study of this approach. The comparison of common-emitter (CE) and CB in InP HBT will be discussed in Section II. The methodology of stabilizing CB topology is described in Section III. The implementation details of two PAs are revealed in Section IV. Section V shows the simulation and measurement results for both PAs.

II. COMPARISON OF CE AND CB IN INP HBT

Transistor configurations have a dramatic impact on performance above 100 GHz due to the role of parasitics. In general, higher gain is desired for compensating input matching losses of PA. Common-emitter (CE) is commonly selected for CMOS and SiGe PA designs in millimeter-wave bands [14] but CB [12] is also a candidate for the InP HBT process due to the relatively small base-collector capacitance.

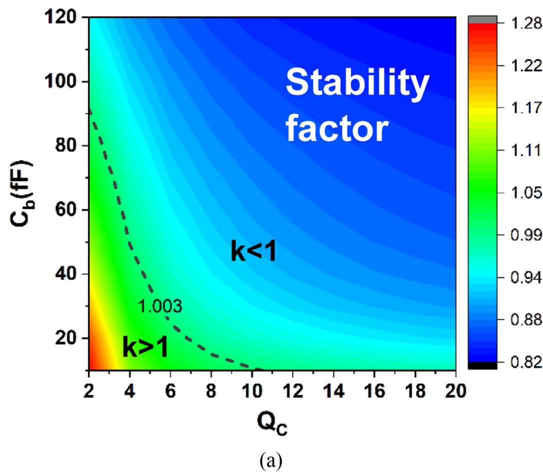
From the small-signal simulation using 2-finger, 4-μm emitter length devices in physics-based scalable model biased at a current density of 2.75 mA/μm^2, CE shows lower G_{max} across the whole G-band band compared to CB as plotted in Fig. 1. Notably the f_{max} of both configurations is identical. The performance summary of two topologies including small signal and large signal at 220-GHz is shown in Table 1. Although CE shows lower power gain than CB, the intrinsic PAE and output power of CE are both slightly better than those of CB. However, if passive matching loss is considered as shown in the last two rows in Table 1, CB designs maintain higher PAE compared to CE design. Comparing peak PAE including 1-dB input and output loss with the intrinsic PAE, PAE of CE is degraded with 17.6% while PAE of CB is only 9.6% lower. If optimum source and load impedance of two configurations are taken into consideration, both the source and load impedances of CE show higher VSWR than those of CB. Higher VSWR indicates higher matching loss, lower overall power gain and reduced highest achievable PAE is expected while implemented with real passive components. Therefore, the CE result in the table with input and output loss considered are optimistic and CB is favorable for G-band PA design.

III. STABILIZATION OF THE CB STAGE

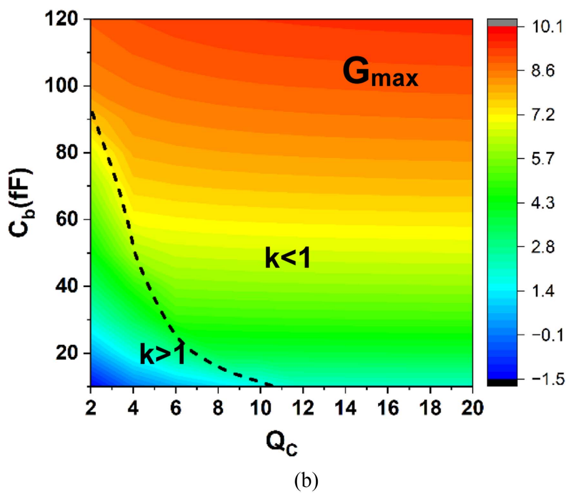
As plotted in Fig. 1, CB does not offer unconditional stability across G-band and requires additional stabilization circuitry. In [12], the authors leverage the sizing of base capacitance to linearize and stabilize CB stages as shown in Fig. 2(a). A collector series resistor is applied in [22] for stabilizing CB stages as shown in Fig. 2(b). In [23], a partially neutralized capacitor is implemented to prevent degradation on G_{max} of CB as shown in Fig. 2(c). These three topologies and the rationale for design selection will be discussed in this section. Besides the approaches mentioned above, lowering base bias point is another approach commonly used to stabilize a CB stage. However, this approach is less favorable due to reduced conduction angle and lower power gain and therefore the lower highest achievable PAE is observed. More detailed analysis will be covered in Section IV.

A. SIZING OF BASE CAPACITOR

Finite base capacitance is designed in [12] without revealing the design consideration or parameters. To understand the reasonable design parameters, simulation of stability factor and



(a)



(b)

FIGURE 3. **(a) Contour of CB stage stability factor with the sweep of base capacitor size and Q of base capacitor at 220-GHz. (b) Contour of CB stage G_{max} with the sweep of base capacitor size and Q of base capacitor at 220-GHz.**

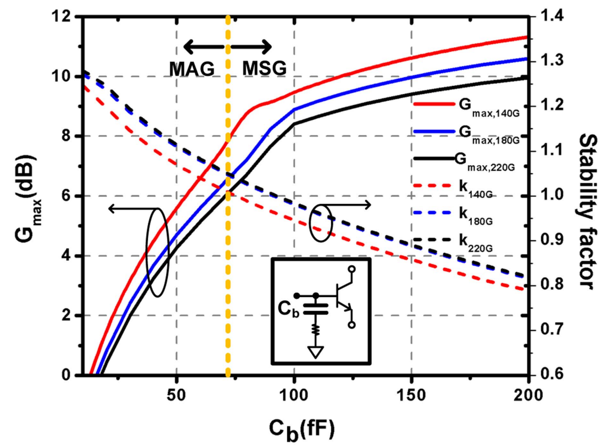


FIGURE 4. **Simulated G_{max} and stability factor of sized C_b CB stage at 140, 180, and 220 GHz.**

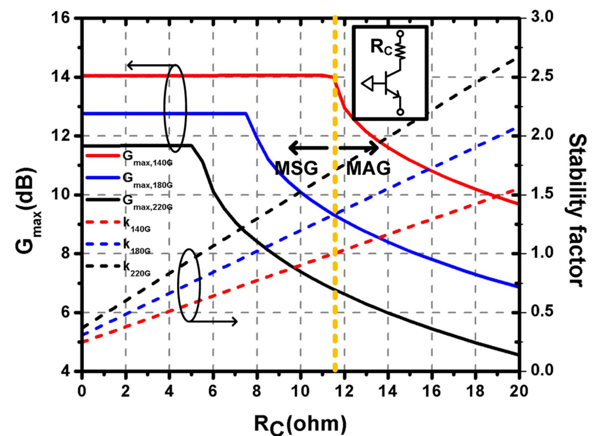


FIGURE 5. **Simulated G_{max} and stability factor of collector series-resistor CB stage at 140, 180, and 220 GHz.**

maximum gain at 220 GHz with the sweep of base capacitance and quality factor (Q) of capacitance are shown in Fig. 3(a) and (b). As observed from Fig. 3(a), Q of base capacitance should be kept below 10 for stability factor to be higher than 1. From Fig. 3(b), Q of base capacitance should be selected in the range of 2–4 for possibly obtaining higher G_{max}.

With the insight for determining Q at the base, the sweep of capacitance for 140, 180, and 220 GHz is shown in Fig. 4. The simulated results show the base capacitance lower than 70 fF with Q of 2 or de-Q resistance of 5.2Ω maintains unconditional stability. Notably, the MAG variation is less than 2 dB over the 80 GHz range suggesting that this technique is relatively wideband.

B. COLLECTOR SERIES-RESISTOR

Using conventional stabilization technique in [24], a series collector resistor is a straightforward methodology for stabilizing a CB stage [22]. The stability circles of the intrinsic device are reduced and move toward the unit circle with additional collector resistance. The simulation in Fig. 5 shows 11.5 Ω or higher resistance would stabilize over the entire G-band with higher gain at 140 GHz compared to base capacitance approach, but the gain rolls off quickly at 220 GHz suggesting that this technique will produce relatively narrowband results.

C. COLLECTOR SERIES-RESISTOR

Pseudo-differential neutralization is widely adopted in mm-wave common-source and/or CE amplifiers in CMOS and BiCMOS process [25]. A pair of neutralization capacitors are added between input and output of amplifier in cross-coupled fashion to enhance the reverse isolation and unilateralize the device for unconditional stability. However, this technique has not been widely adopted with CB mm-wave PAs. In [24], the CB neutralization technique is applied to 600 GHz in 130-nm InP HBT process for high gain but the performance for power amplifiers has not been described. This manuscript attempts

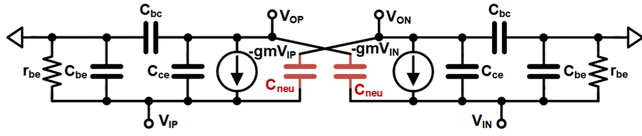


FIGURE 6. Small signal model of pseudo-differential neutralized CB stage.

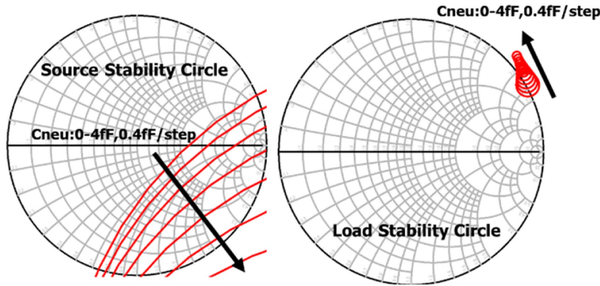


FIGURE 7. Simulated source and load stability circle with sweep of C_{neu}.

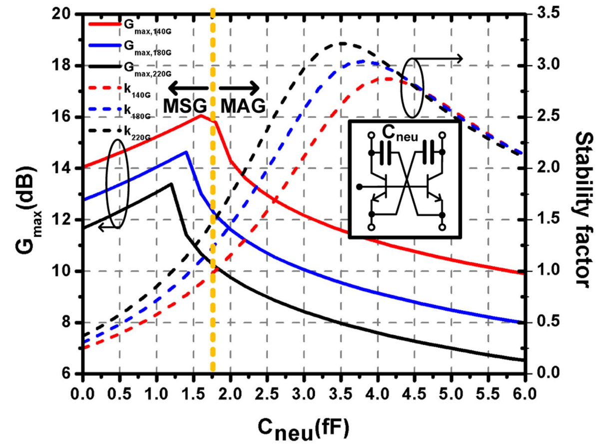


FIGURE 8. Simulated G_{max} and stability factor of collector neutralized CB stage at 140, 180, and 220 GHz.

to address this opportunity to explore collector-emitter neutralization in a CB power stage.

To understand the topology, a simplified small-signal model is shown in Fig. 6 and the Y-parameters can be written as

$$Y_{11} = g_m + \frac{1}{r_{be}} + j\omega (C_{be} + C_{ce} + C_{neu}) \tag{1}$$

$$Y_{22} = j\omega (C_{bc} + C_{ce} + C_{neu}) \tag{2}$$

$$Y_{21} = -g_m - j\omega (C_{ce} - C_{neu}) \tag{3}$$

$$Y_{12} = -j\omega (C_{ce} - C_{neu}) \tag{4}$$

where C_{neu} is neutralization capacitance. From (4), we could observe the reverse isolation will be maximized by choosing C_{neu} equals to C_{ce}. Generally, adding C_{neu} tends to push the stability circles out of the Smith chart unit circle as shown in Fig. 7. The disadvantage of this topology from (1) and (2) is the increased total input and output capacitance, which will make input and output matching network more narrowband as well as more lossy. The G_{max} and stability factor with the sweep of neutralization capacitance at 140, 180, and 220 GHz is shown in Fig. 8. From the plot, C_{neu} should be larger than 1.8fF for stabilizing the entire band while offering more gain than the other approaches.

D. COMPARISON OF TOPOLOGIES

If the in-band unconditional stability criteria of power cell are the same for all three approaches, G_{max} at 220 GHz of the base-capacitor stabilized approach drops to 6 dB, the collector series-resistor stabilization method drops to 6.8 dB, while the neutralized CB stabilization degrades to 10.2 dB. With stabilized in-band power cell, out-of-band unconditional stability is normally achieved with matching networks by avoiding conditional stability. Therefore, the neutralized CB offers higher G_{max} than the other two cases. It is also worth mentioning that adding collector series-resistor will increase the effective knee voltage and this is not favorable for PA design. Large signal simulation results of three topologies are summarized in Table 2 where the neutralized CB shows best overall performance compared to the other two topologies.

TABLE 2. Simulated Results of Three Topologies at 220 GHz

Simulated	Base C_b	Collector R_c	Collector-Emitter C_{neu}
$Z_{S,opt}$	94-j*22 Ω	33-j*19 Ω	29-j*5 Ω
$Z_{L,opt}$	35+j*133 Ω	43+j*103 Ω	30+j*93 Ω
Peak PAE	23.3 %	18.1 %	37.3 %
Pout@ PAE_{peak}	13.3 dBm	11.8 dBm	14.6 dBm
Peak PAE with 1-dB input and output loss	13.9 %	12 %	26.3 %

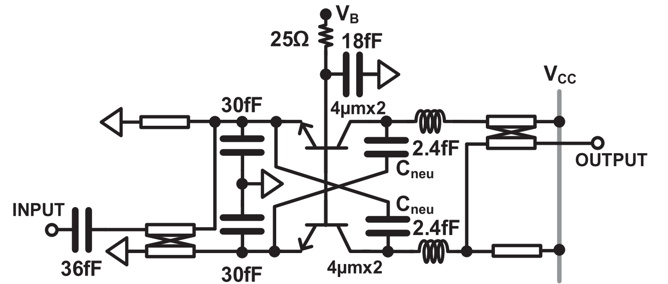


FIGURE 9. Schematic of the proposed single-stage G-band PA.

IV. CIRCUIT IMPLEMENTATION

To investigate the large-signal performance, single-stage (Fig. 9) and 3-stage 4-way-combined (Fig. 10) PAs are designed in InP HBT process. Teledyne's 250-nm InP HBT process offers four gold metal layers in Benzocyclobutene (BCB) with 75-μm thick InP substrate and through-wafer vias. Thin film resistors and metal-insulator-metal (MIM) capacitors are available in this process. Only single-finger models are available in this process and multi-finger models

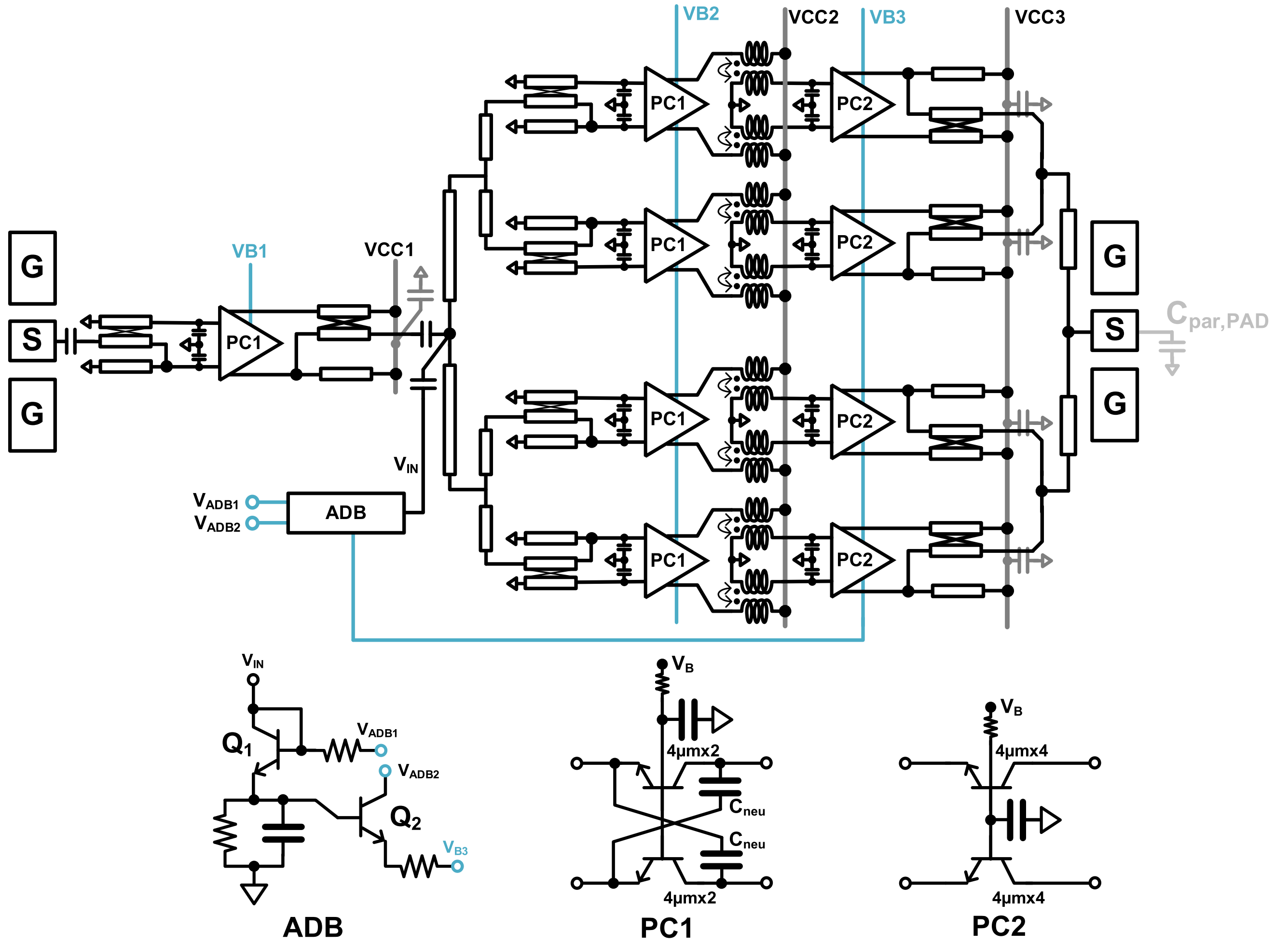


FIGURE 10. Schematic of the proposed 3-stage, 4-way-combined G-band PA.

comprise several single fingers in parallel with routing captured in EM simulation. Also, it is worth noticing there is no thermal model in this process and thus larger simulation and measurement discrepancy could be observed in high power region. Mutual heating between devices also contributes to model/hardware correlation.

The single-stage design is constructed with input and output baluns, the neutralized CB power cell, and additional matching network between power cell and balun. The output power level with optimum PAE is estimated [31], [32] with equation

$$\eta_{PAE} = \frac{1}{2} \cdot \frac{\alpha - \sin(\alpha)}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)} \cdot \left(1 - \left(\frac{f_0}{f_{max}}\right)^2 \cdot \frac{4}{L_{IMN}(1-\cos(\alpha/2))^2}\right) \cdot \left(1 - \frac{V_{knee}}{V_{dc}}\right) \cdot L_{OMN} \tag{5}$$

where

$$L_{IMN} = \frac{\sqrt{(kQ_i)^2+1}-1}{\sqrt{(kQ_i)^2+1}+1} \tag{6}$$

$$L_{OMN} = \frac{Q_o}{Q_o+Q_t} \cdot \frac{1}{1+\frac{|XC_o|}{R_L Q_o}} \tag{7}$$

The α is the conduction angle, f_0 is operating frequency, k is the coupling factor of transformer or balun, Q_i and Q_o are quality factor of passive elements at input and output while C_o is the output capacitance of power transistors. With the expression in (5), PAE contour with sweep of output power and conduction angle at 220 GHz is plotted in Fig. 11. Class-AB operation with output power level at around 17.4 mW shows the highest PAE.

The 3-stage 4-way-combined design includes both neutralized CB driver stages and non-neutralized CB final stage for higher output power. The neutralized CB is not used in final stage of high-power PA is observed through (2) and (7) where high output matching loss could be observed. Also, larger C_{neu} introduces self-resonance toward lower frequency and cause instability out-of-band. To achieve same output power as non-neutralized CB design, 8-way-combined PA will be required for neutralized CB. However, an 8-way-combined design will be difficult to fit into λ/2 constraint in a phased-array transmitter. A 4-way power splitter is added between the first and

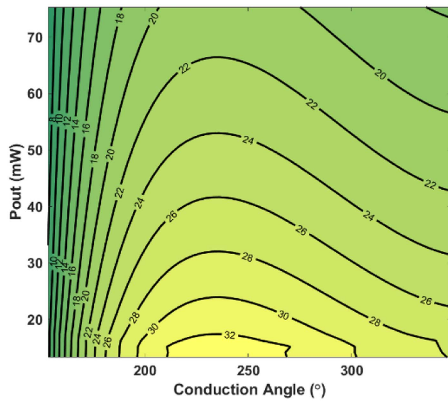
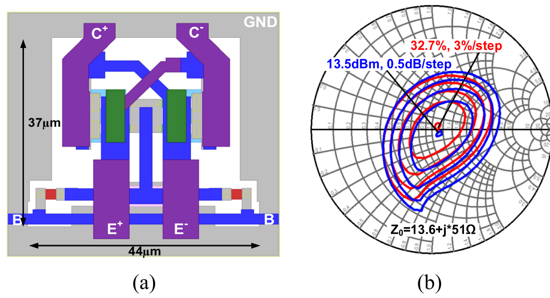


FIGURE 11. Calculated PAE contour with output power and conduction angles in 250-nm InP HBT at $f_0 = 220$ GHz.



(c)

FIGURE 12. (a) Footprint of differential 2 × 4 μm power cell. (b) Simulated PAE contours (red) and power contours (blue) of differential 2 × 4 μm power cell at 220 GHz. (c) Footprint of differential 4 × 4 μm power cell.

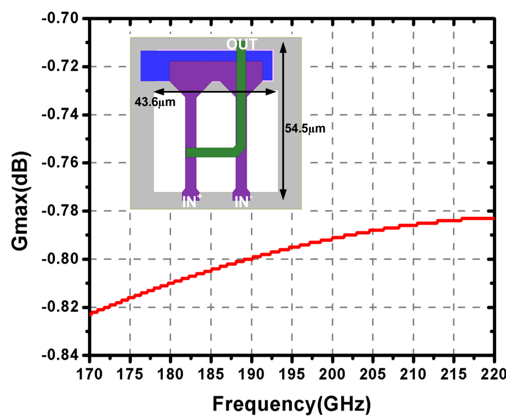
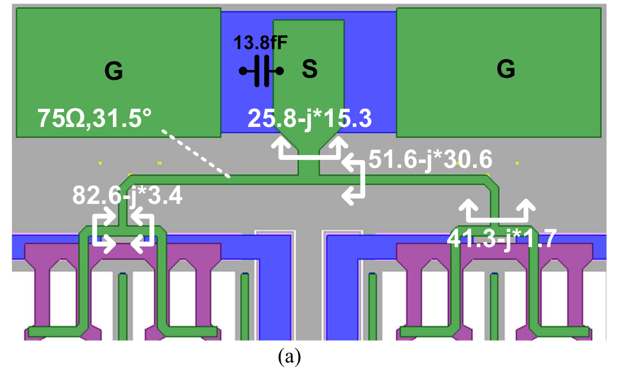


FIGURE 13. The layout of the proposed coupled line balun and the simulated G_{max}.



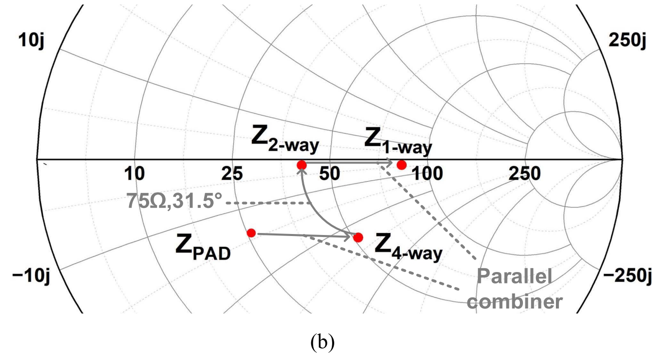


FIGURE 14. (a) Layout and impedances of four-way output combiner. (b) Trajectories of power combiner impedance transformation.

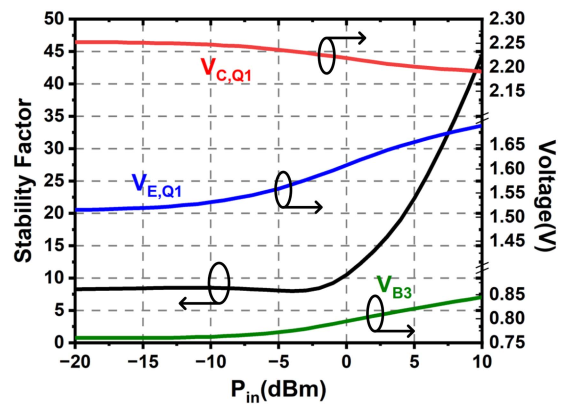


FIGURE 15. Stability factor of 3-stage 4-way-combined PA and voltages of adaptive bias circuit with sweep of input power.

second stage along with a 4-way power combiner at the output stage. The device size ratio of the three stages is 1:4:8 while the highly coupled transformers are designed between the second and last stages. Adaptive bias (ADB) is also added to ensure the last stage could be biased lower in small signal region for stability consideration while maintaining sufficient power gain at high power region.

A. POWER CELL DESIGN

The footprint of the proposed neutralized differential CB power cell is shown in Fig. 12(a) with total device size of

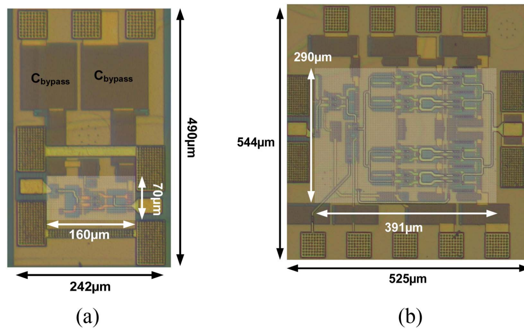


FIGURE 16. Micrograph of (a) Single-stage PA. (b) 3-stage, 4-way-combined PA.

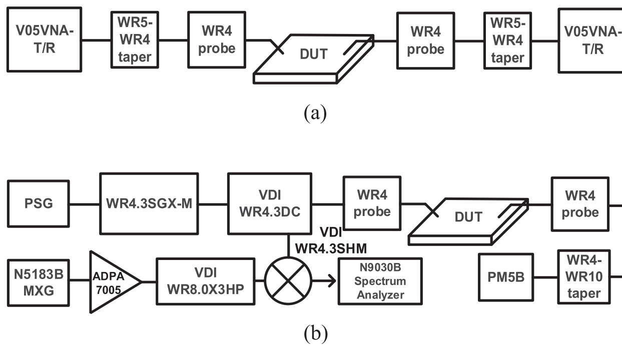


FIGURE 17. (a) S-parameter measurement. (b) WR4.3 power measurement setup.

4 μm^2 composed of a pair of 2-finger 4-μm emitter length HBTs. To further increase the output power, the last stage of the 3-stage 4-way-combined PA uses 8 μm^2 total device size periphery formed from a pair of 4-finger 4-μm emitter length HBTs as shown in Fig. 12(c). In this large power cell, the neutralization capacitor is not applied due to large additional input and output capacitance that will increase the loss of matching network and lower PAE. Both designs occupy small area, 2-finger cell is 37 μm $\times$ 44 μm and 4-finger cell is 30 μ m $\times$ 47 μm.

In both designs, the collectors are shared between different fingers for the minimum footprint as well as reducing the series inductance and phase delay between fingers. The base voltage is fed from either left or right side making it easier for multi-way power combining design. The distance between all base connections is minimized such that the ac currents have a low-impedance path between the devices while suppressing base inductances that induce instability. A secondary consideration between these cells is the self-heating between transistors.

Load-pull simulations of the G-band neutralized power cell in Fig. 12(a) are shown in Fig. 12(b) with characteristic impedance of 13.6+j51Ω at 220 GHz. The differential equivalent load impedance shows 40 pH ∥ 200 Ω is required to achieve 13.5 dBm peak power and 32.7% peak PAE at 220 GHz with 6-dBm input power.

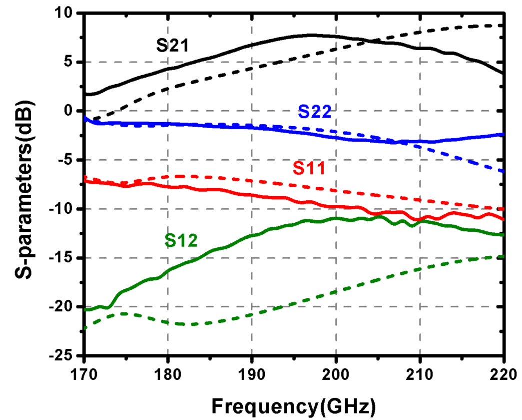


FIGURE 18. Measured (solid) and simulated (dashed) S-parameters of single-stage PA.

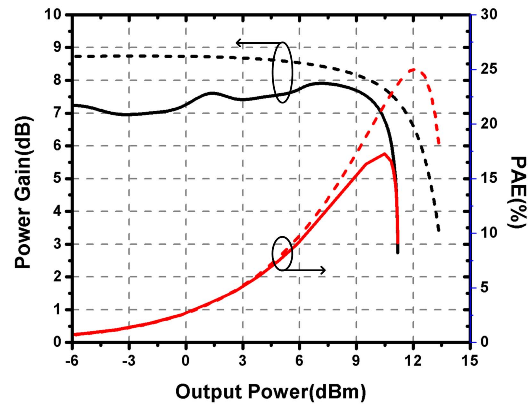


FIGURE 19. Power gain and PAE versus output power measured (solid) at 200 GHz and simulated (dashed) at 220 GHz of single-stage PA.

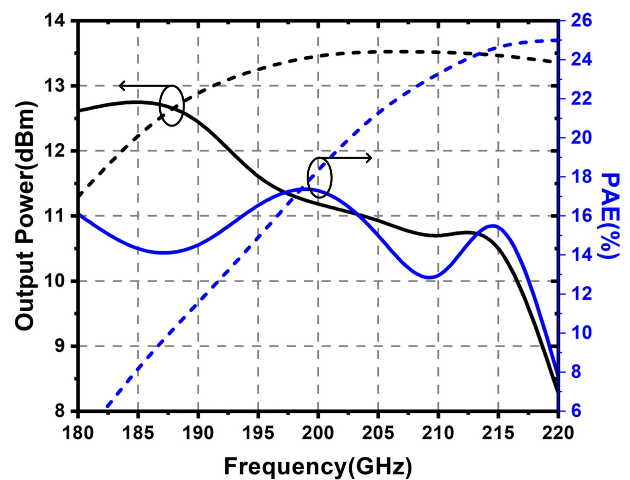


FIGURE 20. Simulated (dashed) and measured (solid) P_{sat} and PAE over 180–220 GHz of single-stage PA.

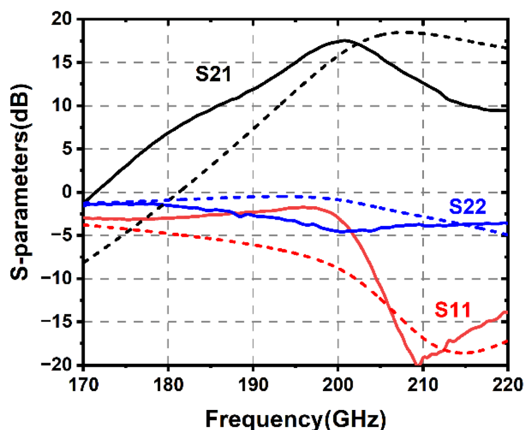


FIGURE 21. Measured (solid) and simulated (dashed) S-parameters of 3-stage, 4-way-combined.

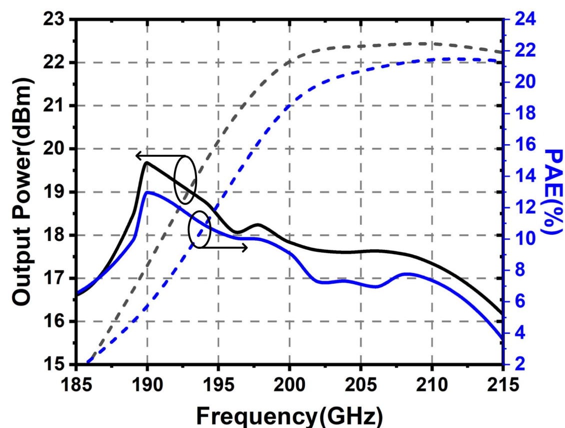


FIGURE 23. Simulated (dashed) and measured (solid) P_{sat} and PAE over 185–215 GHz of 3-stage, 4-way-combined PA.

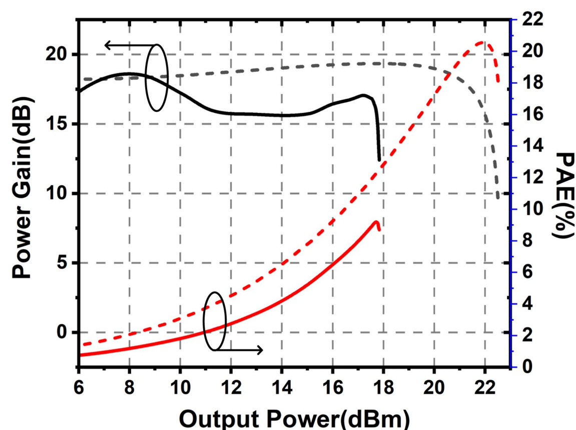


FIGURE 22. Power gain and PAE versus output power measured (solid) at 200 GHz and simulated (dashed) at 208 GHz of 3-stage 4-way-combined PA.

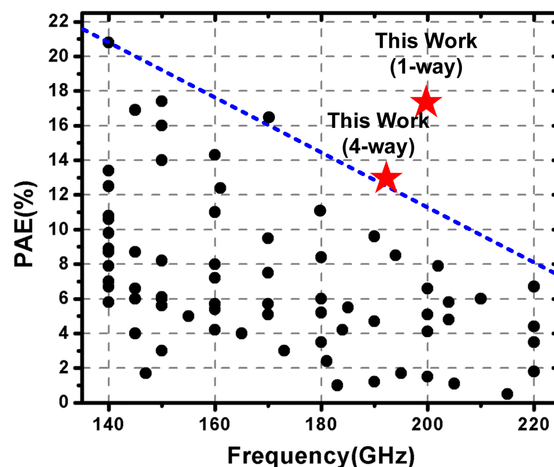


FIGURE 24. PAE comparison of published G-band PAs.

B. G-BAND COUPLED-LINE BALUN

From the analysis in Section II, the output balun loss is important to realizing high efficiency. In [26], the sub-quarter-wavelength balun (SQWB) is proposed for pseudo-differential CE PA in W-band. The loss of SQWB is low, but the area footprint remains large due to the spacing between bottom plate metal and ground metal and two bypassing capacitors. At G-band, bypassing capacitors not only occupy large area but also provide finite resistance to AC ground and, therefore, the loss of balun increases. Additionally, long dc power line introduces voltage drop and the symmetry between different power cells.

To reduce the size and improve loss, bent transmission lines leverage a virtual ground as proposed in [27] for D-band design. The design is moved to G-band for both single-stage and power-combined versions.

Fig. 13 shows the output balun design in the single-stage PA. The differential port (IN+ and IN−) is on metal 3 (M3) while the single-ended port (OUT) is on metal 4 (M4). IN+ is directly connected to OUT while the signal from IN− is coupled from M3 to M4. The simulated equivalent inductance of two coils is 45.6 pH differential and 41.1 pH on single-ended side with coupling factor of 0.58 at 220 GHz. The simulated phase error and gain error between differential ports are 3.4° and 0.12 dB while G_{max} of this CLB is −0.78 dB at 220 GHz.

C. POWER COMBINER DESIGN

Low-loss power combiner is a key for keeping high efficiency while targeting high output power. In [28], the parallel power combiner and design methodology are proposed at D-band using a CMOS SOI process. A similar approach is applied to the 3-stage, 4-way-combined PA design. The design parameters at different nodes of parallel power combiner are shown in Fig. 14(a). In this implementation, the RF pad impedance is designed to minimize the length of transmission line for compact size and lower loss. The impedance trajectories are

TABLE 3. Performance Comparison of G-Band PAs

Ref.	Technology	Frequency (GHz)	Gain(dB)	P_{sat}(dBm)	Peak PAE (%)	Core Area (mm^2)	$\frac{P_{sat}}{Area}$(W/mm^2)
This work	**250-nm InP HBT**	**180–220**	**7.8**	**12.7**	**17.3 @ 200-GHz**	**0.011**	**1.69**
This work	**250-nm InP HBT**	**194–207**	**17.6**	**19.7**	**13 @ 192-GHz**	**0.113**	**0.83**
[6]	65-nm bulk CMOS	195–209	19.5	9.4	1.03 @ 209-GHz	0.92	0.009
[7]	32-nm SOI CMOS	205–225	15	4.6	6 @ 210-GHz	0.06	0.048
[8]	130-nm SiGe BiCMOS	142–182	30.7	18.1	12.4 @ 161-GHz	0.42	0.15
[9]	130-nm SiGe BiCMOS	150–170	24	18	9.4 @ 160-GHz	0.51*	0.12
[10]	130-nm SiGe BiCMOS	200–255	12.5	12	1@ 230-GHz	0.45*	0.04
[11]	130-nm SiGe BiCMOS	200–225	25	9.6	0.5 @ 215-GHz	0.47*	0.02
[12]	250-nm InP HBT	190–210	23.5	18.3	7.9 @ 202-GHz	0.85*	0.08
[13]	250-nm InP HBT	190.8–244	35	19	6.1 @ 220-GHz	1.03*	0.08
[14]	250-nm InP HBT	150–180	31.4	21	16.2 @ 170-GHz	0.54*	0.23
[15]	250-nm InP HBT	180–260	32	21.5	5.1 @ 200-GHz	1.436*	0.1
[16]	250-nm InP HBT	181–205	22.4	12.7	9.6 @ 190-GHz	0.304*	0.06
[17]	250-nm InP HBT	160–183	23.6	21.5	9.5 @ 170-GHz	0.827*	0.17
[18]	Sub-50nm InP HEMT	200–230	17.8	18.8	3.7 @ 210-GHz	0.96*	0.08
[19]	100-nm GaN HEMT	150–189	13	15.8	2.4 @ 181-GHz	0.9*	0.04
[20]	40-nm GaN HEMT	140–205	4.5	13.8	3.5 @ 180-GHz	-	-
*Graphically estimated							

shown in Fig. 14(b) on Smith chart and the simulated loss of combiner is 0.25 dB.

D. ADAPTIVE BIAS CIRCUIT

Since the last stage of the 3-stage, 4-way-combined PA is not a neutralized CB stage, a lower bias condition, e.g., deeper class-AB, is applied for reducing the small signal gain. However, PAE drops with the lower bias condition due to low power gain at high power region. The ADB shown in Fig. 9 is formed with a BE diode-connected HBT, a RC filter and an emitter-follower. With capacitive coupling from the output of the first stage, the base voltage of Q1 drops and emitter voltage increases at high power region due to higher current flowing through the base and emitter resistors. The emitter voltage is later fed to an emitter-follower for providing isolation as well as controlling the adaptive voltage range. Simulated results of voltage at different nodes are shown in Fig. 15. The plot also shows stability factor of PA at 205 GHz is stable at low power region and is still stable at high power region with ADB.

V. SIMULATION AND MEASUREMENT RESULTS

The proposed PAs are implemented in a 250-nm InP HBT process and illustrated in the microphotograph in Fig. 16(a) and (b). The core area of two designs are 0.011 mm^2 and 0.113 mm^2 while the chip area including pads are 0.119 mm^2 and 0.286 mm^2. The single-stage base is biased with 0.82 V and the collector supply is 2.5 V. The first and second stage bases of the 3-stage, 4-way-combined PA are biased at 0.83 V with a 2.1 V collector supply. The third stage base is biased with ADB from a supply voltage is 2.5 V.

The S-parameters are measured with G-band OML frequency extender with WR5 to WR4.3 wave guide taper as shown in Fig. 17(a). WR4.375-μm pitch waveguide probes are used, and calibration is done with CS-15 calibration substrate to the probe tip. The power measurement setup is shown in Fig. 17(b) and is executed with VDI WR4.3SGX-M signal generation module as power source. The directional coupler with sub-harmonic mixer on coupled port is used to down convert the input signal for obtaining the calibration factor and tracking the input power. The output is connected to power meter with WR4 to WR10 waveguide taper. The probe loss is captured using the shortest thru line on CS-15 and therefore the calibration is also done to the probe tip for power measurement.

A. SINGLE-STAGE PA DESIGN

The measured and simulated S-parameters of the single-stage PA are plotted in Fig. 18. The measured peak gain is 7.8-dB at 197 GHz with a 182 to 218 GHz 3-dB bandwidth. The discrepancy of S12 between simulation and measurement are due to separate EM cells in simulation that does not capture the coupling between two baluns and power cell. Power measurements at 200 GHz are plotted in Fig. 19. The measured peak PAE is 17.3% at 10.5 dBm output power while still offering 5.7-dB power gain. The OP1dB at 200 GHz is 10.8 dBm. The output power and PAE across frequencies are also measured in Fig. 20. The measured output power is over 8.3 dBm and PAE is over 7.7% across a frequency range covering 180 to 220 GHz. The measured small signal gain is down-shifted 10% of simulated center frequency which is due to the segmented EM cells that is not capturing the input and

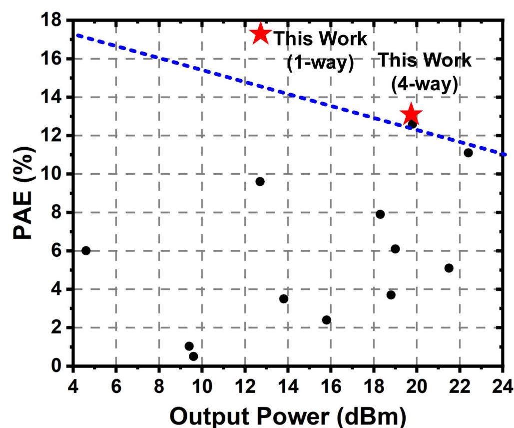


FIGURE 25. PAE vs. output power plot of published 180–220 GHz PAs.

output coupling between passive matching networks as well as RF pads. The large signal discrepancy is most likely due to self-heating that is not incorporated into HBT devices model. Similar discrepancy is also observed in [12].

B. A 3-STAGE, 4-WAY-COMBINED PA DESIGN

The simulated and measured S-parameters of the 3-stage, 4-way-combined PA are plotted in Fig. 21. The measured peak gain is 17.6-dB at 201 GHz with 194 to 207 GHz 3-dB bandwidth. Power measurements at 200 GHz are plotted in Fig. 22. The measured peak PAE is 9.1% at 17.8 dBm output power while still offering 16.5-dB power gain. Output power and PAE across frequencies are also measured in Fig. 23. The measured output power is between 16.2 to 19.7 dBm and PAE reaches 13% in the range of 185–215 GHz. The discrepancy between simulation and measurement is mainly due to model accuracy as well as the higher temperature not captured in simulation. Since ADB is highly relying on model accuracy and shifted with temperature change, the power sweep curve in Fig. 22 and the large signal performance in Fig. 23 are not close to simulation results.

VI. CONCLUSION

In this paper, we demonstrate two G-band PAs with high PAE. The neutralized CB is used in both designs for maintaining high gain and efficiency. Parallel power combining and adaptive bias circuits are also applied to the 3-stage, 4-way-combined PA. The performance summary is shown in Table 3. The PAE survey of G-band PAs is plotted in Fig. 24. The PAE and output power of 180–220 GHz PA is shown in Fig. 25 and our proposed designs show superior performance compared to the prior art.

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