IEEE Journal of Microwaves

Received 5 October 2022; accepted 1 November 2022. Date of publication 23 November 2022; date of current version 6 January 2023.

Digital Object Identifier 10.1109/JMW.2022.3221268

GaN Integrated Circuit Power Amplifiers: Developments and Prospects

REZA NIKANDISH (Senior Member, IEEE)

(Invited Paper)

School of Electrical and Electronic Engineering, University College Dublin, 4 Dublin, Ireland (e-mail: reza.nikandish@ieee.org)

ABSTRACT GaN integrated circuit technologies have dramatically progressed over the recent years. The prominent feature of GaN high-electron mobility transistors (HEMTs), unparalleled output power densities, has created a paradigm shift in the established and emerging high-power applications. In this article, we present a review on the developments and prospects of GaN integrated circuit power amplifiers (PAs). The progress of GaN transistors including improvements in their important features, i.e., supply voltage, substrate material, transistor scaling approach, and device modeling are elaborated and the current state-of-the-art processes with 20-nm gate length, 450 GHz cut-off frequency, and over 600 V supply voltage are discussed. We also investigate developments in the GaN integrated circuit PA architectures and their implementation challenges including the reactive matching PAs capable of delivering over 100 W output power and operating up to 200 GHz, PA linearity, back-off efficiency enhancement, reconfigurable PAs, and distributed PA architectures. Finally, we discuss the prospects of GaN technology and possible future improvements, in transistor and circuit levels, which can advance performance and functionality of GaN integrated circuits.

INDEX TERMS Distributed amplifier, Doherty power amplifier, Gallium Nitride (GaN), high-electron mobility transistor (HEMT), integrated circuit, mm-Wave, monolithic microwave integrated circuit (MMIC), MTT 70th Anniversary Special Issue, power amplifier (PA).

I. INTRODUCTION

GaN technology has revolutionized wide-bandgap semiconductor industry through offering transistors with remarkably high breakdown voltages, e.g., exceeding 100 V. This enables the operation of GaN transistors with high supply voltages and, as a result, impressive output power densities. GaN technology has been primarily employed for high power generation where the GaN high-electron mobility transistor (HEMT) has emerged as the dominant force in solid-state power amplifiers (PAs) [1], [2], [3], [4].

Early developments in GaN HEMT started in 1990s, where a number of two-dimensional electron gas (2DEG) of GaN/AlGaN heterojunction implementations were reported [5], [6], [7]. These preliminary processes used sapphire (Al_2O_3) as the substrate, a material with low thermal conductivity (32 W/m·K at room temperature), which was not suited for high-power applications [8]. This issue was later resolved by using silicon carbide (SiC) with excellent thermal conductivity (490 W/m·K at room temperature) as the substrate which allows high power densities be efficiently dissipated and avoids extremely high channel temperatures [1], [9]. The first GaN integrated circuits using flip-chip bonding for thermal management were reported in 1999 [10], [11]. In [10], a traveling-wave power amplifier (TWPA) was presented, where GaN HEMTs were grown on sapphire substrate with flip-chip bonding onto AlN substrate to improve the thermal management. The TWPA operated over 1–8 GHz bandwidth and delivered 4.5 W output power under 22 V supply voltage, while the power-added efficiency (PAE) was $< 15\%$. Other PAs using the same process but reactive output matching circuit architectures were presented in [11], which achieved 3–9 GHz bandwidth, 3.2 W output power, and 24% PAE. Using a similar process, later, a PA with 6–10 GHz bandwidth delivered a record output power of 14.1 W under 25 V supply voltage with 25% PAE [12]. The first fully integrated, i.e., monolithic microwave integrated circuit (MMIC), GaN PA was presented in 2000 [13], where a nonuniform distributed power amplifier (NDPA), realized using dual-gate

TABLE 1. State-of-the-Art GaN Integrated Circuit Processes

Foundry and Process	V_{DD}	V_{BR}	f_T	Power Density	NF_{min}
Qorvo, 500-nm GaN-on-SiC	65 V	190 V		9 W/mm @3.5 GHz	N/A
Qorvo, 250-nm GaN-on-SiC	40 V	75 V	32 GHz	6 W/mm @10 GHz	N/A
Qorvo, 150-nm GaN-on-SiC	28 V	50 V	90 GHz	4.2 W/mm @30 GHz	N/A
HRL, 150-nm GaN-on-SiC	12 V	50 V		1.8 W/mm	N/A
HRL, 40-nm GaN-on-SiC	12 V	50 V	130 GHz	1.5 W/mm	N/A
WIN, 450-nm GaN-on-SiC	50 V	160 V	15 GHz	7 W/mm @2.7 GHz	N/A
WIN, 250-nm GaN-on-SiC	28 V	120 V	25 GHz	5 W/mm @10 GHz	N/A
WIN, 150-nm GaN-on-SiC	20 V	120 V	35 GHz	3 W/mm @30 GHz	N/A
IAF, 100-nm GaN-on-SiC	15 V	50 V	100 GHz	N/A	N/A
OMMIC, 100-nm GaN-on-Si	12 V	36 V	150 GHz	4.0 W/mm @40 GHz	1.5 dB @40 GHz
OMMIC, 60-nm GaN-on-Si	12 V	36 V	110 GHz	2.9 W/mm @94 GHz	1.0 dB @40 GHz

transistors with 400-nm gate length on sapphire substrate, achieved 1.25 W peak output power and 25% peak PAE at 3 GHz under 15 V supply voltage.

The research and development activities on GaN integrated circuit technologies have been pursued on three main streams: material, device, and circuit. In the *material level*, different substrate materials have been investigated including sapphire [8], native GaN [14], diamond [15], SiC [1], silicon (Si) [16], and silicon-on-insulator (SOI) [17], [18]. The substrate materials are evaluated based on several factors mainly thermal conductivity, fabrication cost, electrical parasitic components, loss, and mechanical robustness. Currently, GaN-on-SiC is the most popular process used in many commercial products. Other than the substrate material, a number of materials have been explored in GaN processes for the fabrication of the gate electrode, drain/source contacts, metal layers, interlayer via, and through-silicon via (TSV) [19].

In the *device level*, a number of GaN HEMT structures capable of operating under higher supply voltages or in higher frequency bands, e.g., T-gate structure, have been presented [1], [2], [3], [4]. Moreover, scaling of the minimum gate length of transistors down to sub-100 nm has enabled the operation of GaN circuits in mm-wave bands [67], [68], [70], [89]. An important challenge in the transistor level has been the development of accurate models for GaN HEMTs which include nonlinearities, high-frequency parasitic components, the charge trapping and memory effects, and the thermal heating impact on performance and reliability [24].

Finally, in the *circuit level*, major developments can be classified to low-loss power combining techniques, harmonic termination networks, integration of bandpass filter (BPF) into the PA circuit, linearization techniques for AM-AM and AM-PM distortions, and broadband uniform and nonuniform distributed PAs. The overall result of these progresses is the development of fully integrated GaN RF PAs with multi-hundred-watt output power, e.g., products by Qorvo [30] and Wolfspeed [31], highly scaled GaN processes, e.g., 40-nm GaN-on-SiC double-heterostructure field-effect transistor (DHFET) [67], [68], 40-nm and 70-nm GaN-on-SiC HEMTs [20], [89], and high-power mm-wave GaN PAs providing 34.8 dBm (3 W) at 84 GHz [83], 37.8 dBm (6 W) at 95 GHz [65], 26 dBm at 120 GHz [70], 15.8 dBm at 180 GHz [70], and 18.5 dBm at 205 GHz [71].

Although the main application of GaN technology is power amplifications, the high power handling capabilities, inherent high linearity, and low noise of the GaN HEMT devices have motivated other applications. GaN low-noise amplifiers (LNAs) can tolerate extremely high input power levels and can provide excellent linearity [88], [89]. Other circuits implemented using GaN technology are control components including switches [92], [93], limiters [94], phase shifters [95], nonreciprocal circulator for full-duplex operation [90], and DC-DC converters [91]. Moreover, single-chip GaN transceiver front-ends have been developed operating at 3 GHz [96], 5.4 GHz [97], 5.9 GHz [98], and 39 GHz [99].

In this article, we present a review on the recent developments in GaN integrated circuit PAs, from transistor to circuit levels, and prospects of GaN technologies. The article is structured as follows. In Section II, progresses in GaN processes and transistors are discussed. In Section III, we present circuit developments on the most popular GaN PA architectures including the reactive matching PAs, Back-off efficiency enhancement PAs, reconfigurable PAs, and distributed PAs. A perspective on future directions is discussed in Section IV. Finally, concluding remarks are presented in Section V.

II. GAN PROCESSES AND TRANSISTORS

A. EARLY DEVELOPMENTS

Successful developments of GaN processes started by the fabrication of 2DEG GaN/AlGaN heterojunctions [5], [6], [7]. Special properties of GaN, wide bandgap of 3.4 eV, high breakdown voltage, and high electron mobility and saturation velocity, have made it a promising material for fabrication of high-power and high-frequency transistors. GaN HEMTs have become commercially available since early 2000, where discrete transistors were provided by different III-V

semiconductor product suppliers, in unmatched and internally matched configurations, delivering up to 1000 W output power and high power densities, ∼ 50 W/mm, operating with high supply voltages, typically ∼ 50–80 V and even >1000 V for some high-power processes, typical PAE of 50–70%, across RF bands below ∼ 10 GHz [1], [3].

The first fully integrated (aka MMIC) GaN PA, implemented using a 400-nm gate length process on sapphire substrate, was a NDPA with 1.25 W peak power and 25% peak PAE operating at 3 GHz under 15 V supply voltage [13]. Subsequently, extensive improvements have been achieved in the reliability and electrical performance of the fully integrated GaN circuits. A summary of the state-of-the-art GaN integrated circuit processes is presented in Table 1. We briefly discuss the most important features of the GaN processes.

B. SUPPLY VOLTAGE

The primary motivation of using GaN HEMTs is their high supply voltage capabilities, resulting from high breakdown voltages of the process. This results in many advantages compared to counterpart processes like GaAs, especially for PA circuits, including the high output power densities, lower supply current, smaller parasitic capacitors, and broadband impedance matching networks. There is therefore a quest to develop transistors capable of sustaining larger supply voltages. The maximum supply voltage however is limited by several factors including the structure and dimensions of the transistor and physical effects, e.g., GaN breakdown electric field (3 MV/cm) [20].

It is experimentally observed that the breakdown voltage increases with the transistor's gate-to-drain separation L_{gd} until it reaches a saturation. The corresponding electric field (V_{BR}/L_{gd}) is about 1–2 MV/cm [20], [23]. The breakdown voltage can be increased using improved HEMT structures, e.g., field plate and multiple field plates [21], [22], [23].

C. SUBSTRATE MATERIAL

Substrate material have significant impacts on thermal, electrical, and cost properties of a GaN process. The substrate performance is conventionally evaluated based on thermal conductivity, fabrication cost, electrical parasitic components, loss, and mechanical robustness. Sapphire was the first substrate used in the early GaN processes, while other materials were subsequently investigated: native GaN [14], diamond [15], SiC [1], Si [16], and SOI [17], [18].

Currently, SiC is the most popular substrate in GaN processes [Fig. 1(a)]. SiC provides an excellent thermal conductivity of 490 W/m·K which allows high power dissipation and prevents self-heating effects. SiC also features a low substrate loss which is especially important for high-frequency and high-speed circuits [1], [9].

Si is another popular substrate material used in GaN processes mainly as a result of the lower cost and the opportunity of heterogeneous integration with CMOS processes [100]. In GaN-on-Si processes, the lateral isolation between multiple transistors is provided through an implant or a mesa etching process, but the coupling through Si substrate degrades the overall isolation [Fig. 1(b)]. Si however suffers from lower thermal conductivity (230 W/m·K) and, more importantly, higher substrate loss compared to SiC. GaN-on-Si processes are maturing rapidly and widely used in high-power switching applications, e.g., boost converters, bridge converter circuits, and power factor correction (PFC) circuits, operating with up to 600 V supply voltages [16].

GaN-on-SOI process has been recently introduced to integrate GaN power systems on a single chip [17], [18]. The process is similar to GaN-on-Si, except for an additional trench or substrate contact to improve the isolation [Fig. 1(c)]. The transistors use a p-type gate (p-GaN) and operate in the enhancement-mode. The fabricated devices have a gate width W_g of 36 mm, a gate length L_g of 0.8 μm, a gate-source spacing L_{gs} of 0.75 μm, and a gate-drain spacing L_{gd} of 6 μm.

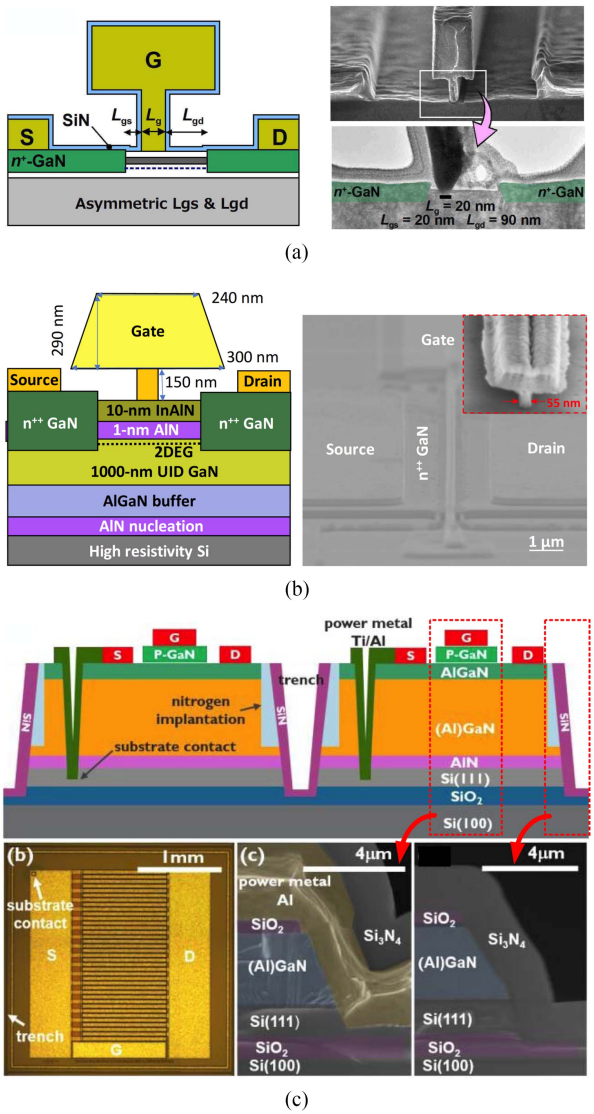

FIGURE 1. (a) GaN-on-SiC HEMT with T-gate and asymmetric gate-drain and gate-source structures [32], (b) GaN-on-Si HEMT structure [34], (c) GaN-on-SOI HEMTs [17].

The p-GaN HEMTs feature a breakdown voltage of around 600 V and can be used for 200 V switching applications [17].

D. TRANSISTOR SCALING

Scaling of GaN HEMTs have been pursued through new device technologies to improve the operational frequency of transistors [20]. The scaling enhances f_T and f_{max} of the transistors but simultaneously degrades their breakdown voltage. This trade-off can be mitigated by using asymmetric HEMT structures with L_{gs} shorter than L_{gd} [see Fig. 1(a)] to prevent the drop of breakdown voltage, e.g., $L_{gd} = 8\,L_{gs}$ in [17].

GaN processes with state-of-the-art operational frequency are 40-nm GaN DH-HEMTs with f_T/f_{max} of 220/400 GHz and breakdown voltage of 42 V [32], GaN-on-Si HEMTs with 40-nm gate length and 300-nm source-drain distance achieving f_T of 250 GHz [33], GaN-on-Si HEMTs with 55-nm gate length and 175-nm source-drain spacing featuring f_T/f_{max} of 250/204 GHz [34], and finally, the highest f_T/f_{max} of 454/444 GHz and 10 V breakdown voltage for a GaN-on-SiC process with 20-nm gate length and $L_{gs} = L_{gd} = 50$ nm [35].

E. MODELING OF TRANSISTORS

Development of accurate models for the transistors is essential to leverage benefits of the GaN process. This is challenging as a result of several physical effects which should be precisely modeled, including the voltage-dependent drain current, $I_{ds} = f(V_{gs}, V_{ds})$, derivatives of the drain current, g_m, g_{m2}, and g_{m3}, voltage- or charge-dependent capacitance models, C_{gs}, C_{gd}, and C_{ds}, temperature-dependent large-signal current model (e.g., through electron mobility and threshold/pinch-off voltage of enhancement/depletion mode devices), models for pulsed and CW operation, and nonlinear models for the load impedance VSWR effects [24].

A number of basic models are conventionally used for GaN HEMTs, e.g., Curtice, EEHEMT, and Angelov [25], which are gradually improved through including important effects [24]. There are some physical behaviors unique to GaN HEMTs which call for new physic-based models. MIT virtual source GaN HEMT high voltage (MVSG-HV) model is a scalable physic-based model capable of capturing static and dynamic behaviors of the transistor through self-consistent charge and current models [28]. Charge trapping is an issue in GaN HEMTs, manifesting as memory nonlinear effects in PA circuits or degraded on-resistance, R_{on}, of the transistor (aka current collapse effect) in switching circuits [26]. Charge trapping effect in MVSG-HV is modeled by including trap transistors as virtual gates in the drain-access region. Moreover, the model includes parameters for the subthreshold operation of the transistor, which is important for accurate modeling of class-C biased devices (e.g., auxiliary amplifier in Doherty PAs). In MVSG-HV, electrothermal model comprises a thermal resistance R_{th} in parallel with a thermal capacitance C_{th}. A nonlinear GaN HEMT equivalent circuit electrothermal model is proposed in [27]. Advanced SPICE model for HEMT (ASM-HEMT), an industry standard model, is a surface potential based physical compact model which can include self-heating, channel length modulation (CLM), drain-induced barrier lowering (DIBL), gate leakage current, surface trapping, and bulk trapping effects [29].

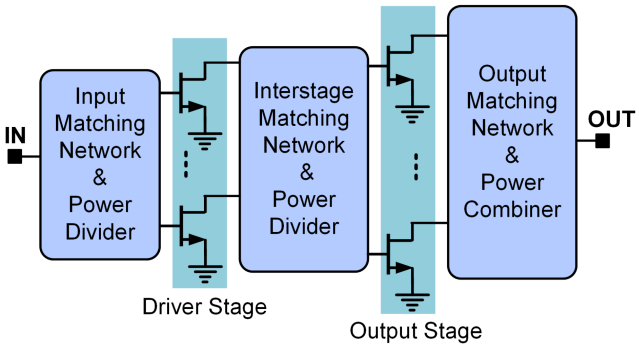

FIGURE 2. Two-stage PA architecture.

III. GAN POWER AMPLIFIERS

A. ADVANTAGES OF GAN FOR PAS

The impressive output power densities of GaN HEMTs is the main, but not the only, advantage for high-frequency PAs. The most important offerings of GaN HEMTs can be summarized as follows.

1) The unparalleled output power densities enable high-power compact PA chips which can be used to reduce electronic systems size and cost in many applications.
2) The high supply voltage translates to lower supply current levels, which improves reliability and reduce thermal cooling requirements.
3) The higher power densities allow smaller transistors to be used for a target output power level. Such transistors feature lower parasitic capacitance, leading to wider bandwidth of the PA circuit.
4) The gate width of GaN HEMTs can be selected to achieve an optimum load resistance R_{opt} close to the load resistance R_L. This results in an impedance transformation ratio close to unity, which helps to realize low-loss and broadband impedance matching networks [38], [39]. This condition cannot be usually satisfied for other processes with lower supply voltages ($R_{opt} \approx 2V_{DD}/I_{max}$).
5) The high breakdown voltage of GaN transistors allows the realization of waveform-shaping PAs to achieve high efficiencies without reliability concerns due to increased drain voltage.

B. REACTIVE MATCHING PAS

In a typical GaN PA, usually multiple transistors are combined to achieve a desired high output power level. The driver stage(s) can also comprise multiple transistors to provide required output power for driving the output stage. A two-stage PA architecture is shown in Fig. 2. The output matching network provides optimum load impedance for the output stage transistors $Z_{L,opt2}$ while combining their output signals and

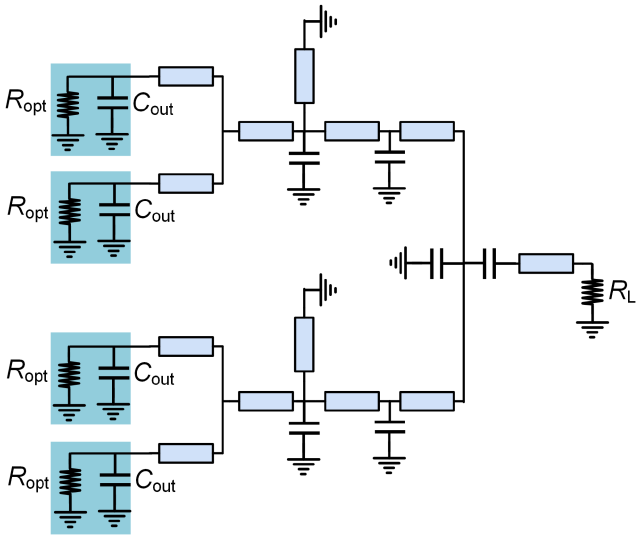

FIGURE 3. Reactive impedance matching and power combining network realized using transmission lines and capacitors. Transistors are modeled by an optimum load resistance in parallel with a parasitic output capacitance which is absorbed into the matching network.

delivering to the load resistance R_L. The interstage matching network transforms the optimum source impedance of the output stage transistors $Z_{S,opt2}$ to the optimum load impedance of the driver stage transistors $Z_{L,opt1}$. The input matching network transforms the source resistance R_S to the optimum source impedance of the driver stage transistors $Z_{L,opt1}$ while dividing the input power between the transistors.

In the reactive matching PAs, the impedance matching networks are realized using lumped LC networks, distributed transmission line based networks, or hybrid of the lumped and distributed elements. The most popular circuit realization is shown in Fig. 3, where the transmissions lines are implemented using meandered microstrip lines or planar waveguides, the capacitors are constructed using the high-quality metal-insulator-metal (MIM) capacitors offered by the GaN process, and the ground connections are realized using back-vias through the substrate. The output impedance of the transistors is modeled by the optimum resistance R_{opt} in parallel with an output capacitance C_{out} which should be absorbed into the output matching network. Resistive components can also be used in the input matching network to ensure stability, extend bandwidth, and improve input impedance matching. The design procedure is similar to the GaAs PAs [36]. In an integrated RF PA, assuming high quality factors for capacitors, efficiency of the output matching network can be derived using quality factors of the inductors as $\eta \approx 1 - \sum_{k=1}^{N_L} \frac{\alpha_k}{Q_{L,k}}$, where N_L is the number of inductors and α_k are coefficients dependent on the impedance transformation ratio and the network circuit architecture [37], [38]. This can provide guidelines to identify critical inductors and maximize their quality factor through layout design techniques.

Several fully integrated GaN PAs using the reactive matching are presented in the literature [40], [41], [42], [43], [44], [47], [65], [69], [70] and developed as commercial products [30], [31]. A performance summary of fully integrated GaN PAs operating in RF bands is presented in Table 2. State-of-the-art RF GaN PAs are shown in Fig. 4. The highest output power levels include 135 W with 47% PAE at 3.1 GHz [40], 40 W with 45% PAE at 5.4 GHz [41], 60 W with 40% PAE at 5.5 GHz [43], 74 W with 40% PAE at 10 GHz [44], 10 W with 45% PAE at 18 GHz [46], and 40 W with 32% PAE at 27 GHz [50].

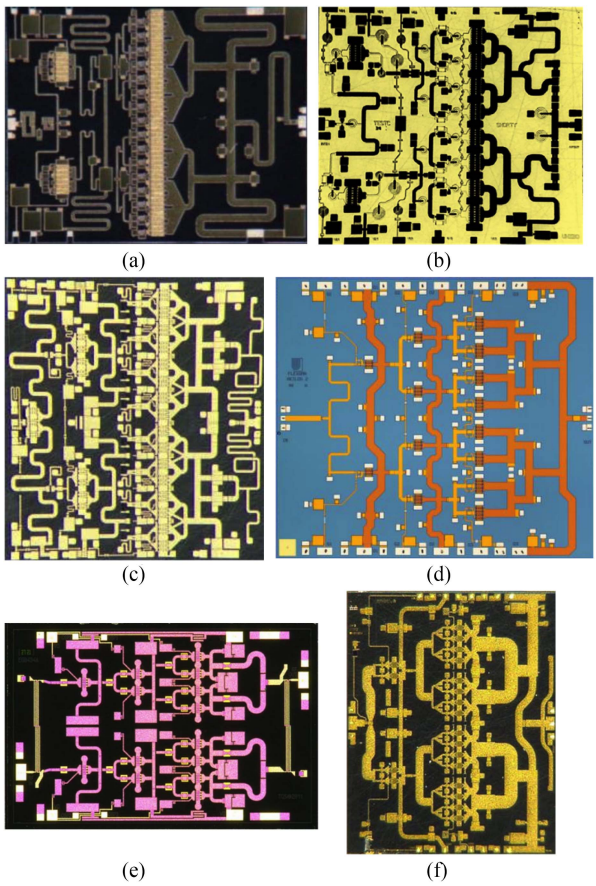

FIGURE 4. State-of-the-art RF GaN PAs. (a) 135 W 3.1 GHz PA [40], (b) 40 W 5.4 GHz PA [41], (c) 74 W 10 GHz PA [44], (d) 10 W 18 GHz PA [46], (e) 9 W 28.5 GHz PA [49], (f) 40 W 27 GHz PA [50].

The output power and efficiency of the GaN HEMTs degrade in mm-wave bands due to the increased loss. The loss of passive elements is also higher in mm-wave bands. This is therefore more challenging to achieve high output power in mm-wave bands. A summary of fully integrated mm-wave GaN PAs is presented in Table 3. State-of-the-art mm-wave GaN PAs are shown in Fig. 5. The highest output power levels achieved in mm-wave bands include 12 W with 30% PAE at 40 GHz [64], 3 W at 84 GHz using a traveling-wave power combining amplifier architecture developed in [83], 6 W with 18% PAE at 95 GHz using a four-path PA with the Wilkinson and Lange coupler power combiners [65], 430 mW with 16% PAE at 120 GHz [70], and 70 mW at 205 GHz implemented using a 70-nm GaN-on-SiC process [71]. Further

TABLE 2. The Reactive Matching RF GaN Integrated Circuit PAs

Ref.	Frequency	V_{DD}	P_{out}	PAE	GaN Process
[40]	2.8–3.5 GHz	40 V	135 W	47%	250-nm GaN-on-SiC
[41]	5.0–5.8 GHz	30 V	40 W	45%	250-nm GaN-on-SiC
[42]	5.6–6.3 GHz	28 V	35 W	61%	250-nm GaN-on-SiC
[43]	5.0–6.0 GHz	28 V	60 W	40%	250-nm GaN-on-SiC
[44]	8.0–12.0 GHz	28 V	74 W	40%	250-nm GaN-on-SiC
[45]	8.5–10.5 GHz	35 V	74 W	54%	150-nm GaN-on-SiC
[46]	17.3–20.2 GHz	9 V	10 W	45%	100-nm GaN-on-Si
[47]	21.5 GHz	20 V	8.9 W	35%	150-nm GaN-on-SiC
[48]	18.5–24.0 GHz	20 V	4 W	40%	150-nm GaN-on-SiC
[49]	27.0–30.0 GHz	20 V	9 W	31%	150-nm GaN-on-SiC
[50]	26.0–30.0 GHz	28 V	40 W	37%	200-nm GaN-on-SiC

TABLE 3. The Reactive Matching mm-Wave GaN Integrated Circuit PAs

Ref.	Frequency	V_{DD}	P_{out}	PAE	GaN Process
[64]	40 GHz	12 V	12 W	30%	100-nm GaN-on-Si
[69]	80 GHz	15 V	720 mW	9%	100-nm GaN-on-SiC
[83]	84 GHz	12 V	3 W	N/A	100-nm GaN-on-SiC
[66]	93 GHz	15 V	2.6 W	21%	100-nm GaN-on-SiC
[65]	95 GHz	15 V	6 W	18%	100-nm GaN-on-SiC
[70]	120 GHz	15 V	430 W	16%	100-nm GaN-on-SiC
[70]	180 GHz	15 V	38 mW	2%	100-nm GaN-on-SiC
[71]	205 GHz	15 V	70 mW	1%	70-nm GaN-on-SiC

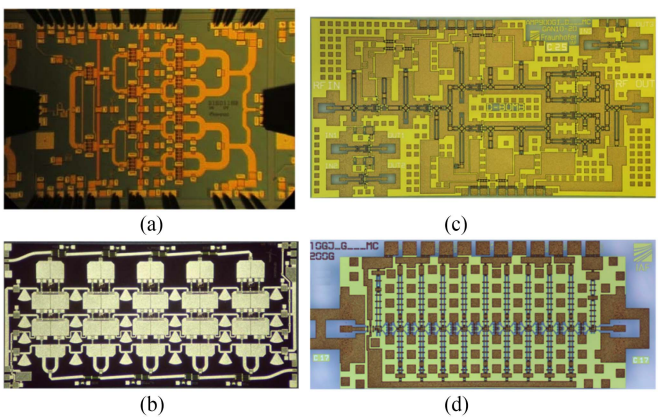

FIGURE 5. State-of-the-art mm-wave GaN PAs. (a) 12 W 40 GHz PA [64], (b) 3 W 84 GHz PA [83], (c) 430 mW 120 GHz PA [70], (d) 70 mW 205 GHz PA [71].

details about mm-wave PAs presented in the literature can be found in [63].

The impedance matching networks of the PA can be used to realize other additional functions, e.g., harmonic termination [37], [39], [42], [51] and filtering [38]. Harmonic termination networks can shape the transistor's drain current and voltage waveforms to realize a specific high-efficiency class of operation (e.g., class E, F). A practical implementation challenge is the narrow bandwidth of the harmonic termination networks [51], which increases their sensitivity to process variations and parasitic components. Broadband harmonic matching networks are introduced to mitigate this issue, but at the cost of lower efficiency [37], [39]. Moreover, a bandpass filter (BPF) can be embedded into the matching networks to suppress harmonics and out-of-band emissions. In [38], a minimum-inductance BPF architecture is introduced which can achieve higher harmonic suppression with a significantly lower total inductance ($\sim 60\%$) compared to a standard BPF. This is used to realize the output matching network of a broadband 2.0–4.0 GHz GaN PA.

C. PA LINEARITY

Linearity of the PA is an important consideration in wireless communications, especially when complex-modulated signals (e.g., QAM and OFDM) are used for efficient high-speed data transmission. These signals are sensitive to the amplitude and phase distortions in the PA characteristics. GaN HEMTs suffer from the soft gain compression where the device exhibits nonlinearity from low power levels (e.g., 10 dB lower than 1-dB compression point). This behavior results in the increased AM-AM and AM-PM distortions of GaN PAs. Also, increasing bandwidth of modulated signals leads to higher

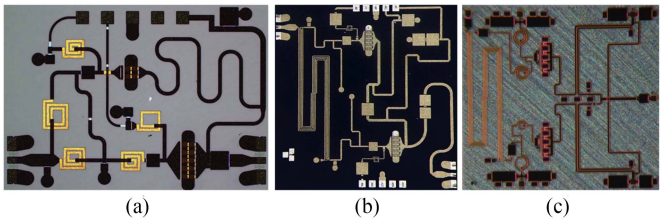

FIGURE 6. GaN integrated circuit Doherty PAs. (a) 3.2 W 6.8–8.5 GHz PA [54], (b) 4 W 5.8–8.8 GHz PA [55], (c) 4 W 4.5–6.0 GHz PA [56]. All PAs are implemented using 250-nm GaN-on-SiC processes.

error vector magnitude (EVM), which is a result of the charge trapping and memory effects in the GaN HEMTs [37], [39].

It is shown that for a fully integrated GaN PA, EVM for QAM signals can be improved (by $>$ 6 dB) through biasing the transistor at the optimum current density [39]. This is a result of the reduced nonlinearity of the transistor's transconductance and gate-source capacitance. Moreover, in [38], a dual-path amplifier architecture is used to combine complimentary compressive and expansive nonlinearity profiles of the two transistors and, as a result, mitigate the AM-AM and AM-PM distortions of the PA. Such circuit-level linearization approaches can provide moderate linearity performance. Nevertheless, digital predistortion (DPD) techniques can be applied to meet the stringent linearity requirements of base stations in the current 5G and emerging generations of wireless communication.

D. BACK-OFF EFFICIENCY ENHANCEMENT

The modulated signals used in wireless communications usually feature a high peak-to-average power ratio (PAPR), typically 6–10 dB, which degrades average efficiency of the PA unless a specific circuit be adopted to improve back-off efficiency of the PA. The most popular PA architecture for back-off efficiency enhancement is the Doherty PA [52], [53]. Doherty PAs implemented as hybrid circuits operating in lower RF bands, typically, $<$ 3 GHz, are extensively investigated in the literature. There are however many practical challenges to leverage the potentials of Doherty PAs implemented as integrated circuits and operating at higher frequencies. The most important issues include the parasitic capacitance and loss of transistors and passive components, large size of transmission lines for on-chip realization, the low gain of the class-C biased auxiliary transistor, and the need for asymmetric transistors for large PAPR signals [53]. A number of circuit architectures are developed for integrated circuit GaN Doherty PAs [54], [55], [56], [57], [58], [59].

In [54], the load modulation network is realized using a T-shape circuit comprising transmission lines (with $l < \lambda/4$) and output parasitic capacitance of the transistors. The PA, shown in Fig. 6(a), achieves 3.2 W peak power and 24–37% PAE at 9-dB back-off across 6.8–8.5 GHz. The Doherty PA presented in [55] comprises a power combining load modulation network, using transmission lines and output parasitic capacitance of the transistors, providing asymmetric drain

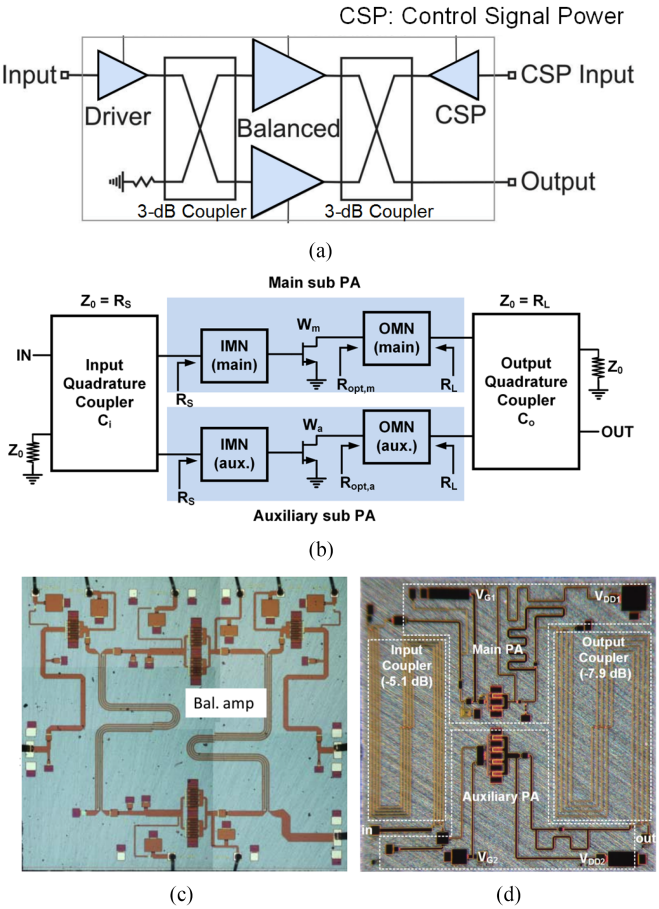

FIGURE 7. Coupler-based PAs: (a) load modulated balanced PA architecture, (b) unbalanced PA architecture, (c) load modulated balanced PA implemented in GaN process [61], (d) unbalanced PA implemented in GaN process [62].

bias for the main and auxiliary transistors, and a Lange coupler operating as the input power splitter and phase shifter. The PA, shown in Fig. 6(b), provides 4 W peak power and 31–39% PAE at 9-dB back-off across 5.8–8.8 GHz. In [56], the load modulation network is realized using coupled transmission lines to extend bandwidth of Doherty PA. The PA chip, shown in Fig. 6(c), achieves 4 W peak power and 22–27% PAE at about 6 dB back-off across 4.5–6.0 GHz.

A number of PA architectures are developed to mitigate limitations of the Doherty PA. Load modulated balanced PA, shown in Fig. 7(a), is a balanced amplifier with an auxiliary amplifier which is used to inject a signal to isolated port of the quadrature coupler. This can modulate the load impedance presented to the two main transistors. The PA efficiency can be improved at back-off over a wide bandwidth through a proper control of the amplitude and phase of the auxiliary signal [60]. A GaN integrated circuit implementation of the load modulated balanced PA, shown in Fig. 7(c), achieves 14 W peak power and $>$ 37% PAE at 9.7 dB back-off across 8.0–9.0 GHz [61]. Another coupler-based PA architecture for back-off efficiency enhancement is unbalanced PA shown in Fig. 7(b) [62]. In this architecture, the class-C biased auxiliary

transistor has a larger size, and hence output power, compared to the class-B biased main transistor. The output quadrature coupler is asymmetric with a coupling coefficient $C_o < -3$ dB. The output power back-off level can be controlled by the transistors' power ratio K_p and coupling coefficient of the output coupler OPBO $= 20\log_{10}[1 + \sqrt{K_p}C_o/\sqrt{1-C_o^2}]$. It is shown that a Doherty-like behavior can be achieved for $C_o \approx -6$ dB. The high isolation between the main and auxiliary amplifiers, provided by the coupler, and the lower impedance transformation ration at back-off result in inherently wider bandwidth performance compared to Doherty PA. The GaN integrated circuit unbalanced PA shown in Fig. 7(d) achieves 2.7 W peak power and 27–40% PAE at about 6 dB back-off across 4.5–6.5 GHz [62].

E. RECONFIGURABLE PAS

Reconfigurable PA architectures which can adapt their circuitry to the input modulated signal can provide remarkable advantages in the average efficiency and linearity. This concept is extensively used in CMOS digital PAs which are mature technology in industry. In GaN technology however the development of reconfigurable PAs is hindered by process limitations, mainly the lack of compact and high-speed switches. We briefly review some preliminary developments in reconfigurable GaN PAs [72], [73], [74].

In [72], a voltage-mode digital GaN PA is presented. The digital PA is implemented in a 250-nm GaN-on-SiC process and is followed by a hybrid BPF circuit which realizes a class-D/S PA. The PA operating at switching frequency of 840 MHz, with a supply voltage varied from 60 to 20 V, achieves the peak output power of 7.8 W and PAE of 47%. A quad-mode reconfigurable harmonic-tuned PA is presented in [73]. The PA comprises one main transistor with the width of W_m and three auxiliary transistors with the width of W_a. The transistors are sized such that $W_m = 3W_a$, which leads to an output power ratio of 2. The PA is implemented in a 250-nm GaN-on-SiC process, operates at 4.8 GHz, provides 2 W maximum power, and through configuring the operation mode can achieve 60% enhancement in the back-off efficiency and 6 dB improvement of the adjacent channel leakage ratio (ACLR). A reconfigurable PA is proposed in [74], which comprises a dual-band output matching network and reconfigurable interstage and input matching networks. The PA can be operated in one of the two modes: 2–3 GHz or 10–12 GHz. The PA is implemented in a 250-nm GaN-on-SiC process and delivers about 1 W output power.

F. DISTRIBUTED PAS

Distributed amplifiers can provide extremely broad bandwidth by absorbing input and output parasitic capacitance of the transistors in the input and output transmission lines [75]. GaN process can provide several advantages for distributed amplifiers mainly simultaneous broad bandwidth and high output power as a result of high power densities which allow small transistors with low parasitic capacitance be used. A

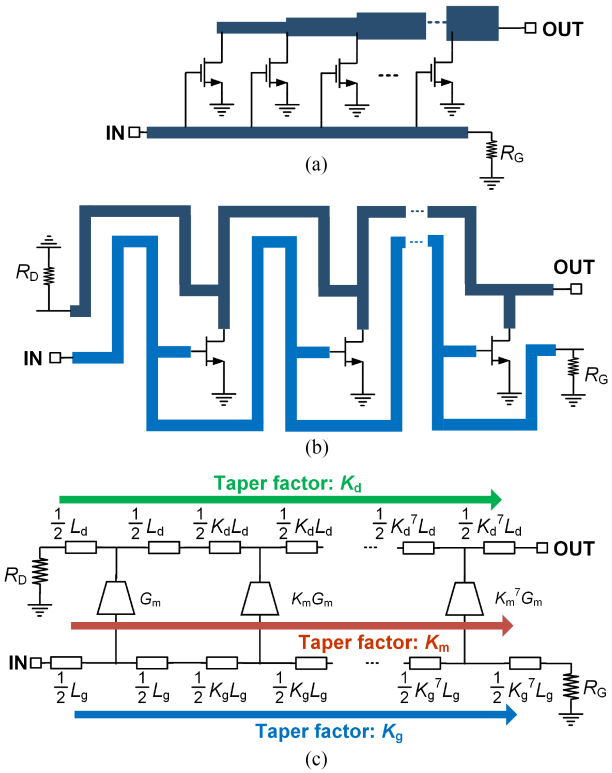

FIGURE 8. (a) Nonuniform distributed amplifier architecture, (b) distributed amplifier with coupled input and output lines, (c) tapered distributed amplifier architecture.

uniform distributed amplifier cannot realize an efficient PA due to the power loss in the output line termination resistor and unequal drain voltage swing of the transistors. These issues are mitigated by using a *nonuniform* distributed amplifier architecture where the characteristic impedance of the output line are scaled down toward the output port and the output line termination resistor is eliminated [Fig. 8(a)]. Sometimes, the width of transistors is also scaled down toward the output port to further enhance the efficiency [76].

A summary of GaN distributed PAs is presented in Table 4. The highest output power of 42–60 W is achieved over 1–6 GHz bandwidth using a 250-nm GaN-on-SiC process with 30 V supply voltage [77]. Moreover, in [80], two nonuniform distributed amplifiers are combined using Lange couplers to construct a balanced amplifier with 12.3–13.5 W output power over 6–18 GHz bandwidth. A bandwidth of 0.1–45 GHz is achieved using a distributed amplifier where the gate lime termination resistor is removed to extend the lower band cut-off frequency [86]. The PA provides 1–2 W output power and is implemented in 150-nm GaN-on-SiC.

Most of the developed GaN distributed PAs use limited circuit architectures, mainly nonuniform distributed amplifier with power combing in the power cell level or as a balanced amplifier. This indicates the need for further circuit level research to achieve higher performance. In [84], a distributed amplifier architecture with coupled input and output lines, as shown in Fig. 8(b), is proposed. It is shown

TABLE 4. Fully Integrated GaN Distributed PAs

Ref.	Frequency	Bandwidth	V_{DD}	P_{out}	PAE	GaN Process
[77]	1.0–6.0 GHz	5.0 GHz | 204%	32 V	42–60 W	30–43%	250-nm GaN-on-SiC
[78]	1.5–17.0 GHz	15.5 GHz | 307%	30 V	9–15 W	20–38%	250-nm GaN-on-SiC
[79]	2.0–18.0 GHz	16.0 GHz | 267%	10 V	0.8–2.0 W	5–15%	200-nm GaN-on-SiC
[80]	6.0–18.0 GHz	12.0 GHz | 115%	40 V	12.3–13.5 W	15–18%	250-nm GaN-on-SiC
[81]	2.0–19.0 GHz	17.0 GHz | 276%	28 V	5.5–12.3 W	22–49%	100-nm GaN-on-Si
[82]	8.0–42.0 GHz	34.0 GHz | 185%	15 V	0.32–0.50 W	4–7%	100-nm GaN-on-SiC
[83]	75–110 GHz	25.0 GHz | 28%	12 V	2–3 W	N/A	100-nm GaN-on-SiC
[85]	2.0–20.0 GHz	18.0 GHz | 285%	N/A	10.0–20.6 W	25–36%	200-nm GaN-on-SiC
[86]	0.1–45.0 GHz	44.9 GHz | 2116%	10 V	1–2 W	N/A	150-nm GaN-on-SiC

that the gate-drain capacitance effects can be canceled by an optimum coupling coefficient between the input and output lines as $k_{opt} = 1/\sqrt{(1 + C_g/C_{gd})(1 + C_d/C_{gd})}$, where C_g and C_d respectively denote the input and output line capacitance in each node and C_{gd} is the transistors' gate-drain capacitance. The original circuit is implemented in a GaAs process which can also be used in GaN processes. Moreover, in [87], a tapered distributed amplifier architecture is proposed in which the length of transmission line segments of the input and output lines as well as the width of transistors are tapered by the factors (K_g, K_d, K_m) [see Fig. 8(c)]. The optimal tapering factors are derived using an analytical model developed for the distributed LNA. This approach can be applied to a distributed PA and derive the optimal tapering factors.

IV. FUTURE PERSPECTIVE

A. TRANSISTOR LEVEL

In the transistor level, one of the major trends pursued has been the scaling of transistors' gate length to enable their operation at higher mm-wave frequencies. The most advanced GaN technology node reported in the literature is the HRL 20-nm GaN-on-SiC HEMT process with f_T/f_{max} of 454/444 GHz [35]. This process can be practically used up to around 200 GHz to realize PA circuits. The process features 50-nm gate-source and gate-drain separation and achieves 10 V breakdown voltage, which limits the supply voltage to about 4 V. The relatively low supply voltage limits the output power density of transistors. In the future therefore two trends can be expected. First, the scaling of transistors will be continued to sub-10-nm nodes to achieve higher operation frequencies and higher performance. Second, to improve the output power densities, the breakdown voltage of transistors should be increased through innovative scaling approaches or transistor structures, e.g., using asymmetric gate-drain and gate-source spacing with $L_{gd} > L_{gs}$.

Another major trend is the development of GaN transistors with extremely high breakdown voltages. Currently, GaN processes with supply voltages of 600 V are available [16]. The quest for higher supply voltages is expected to be continued to push the performance limits of emerging high-power electronic applications. A critical challenge is the trade-off between breakdown voltage and switching speed or maximum operational frequency of the GaN devices. A possible solution can be the development of GaN processes which permit stacking of transistors, i.e., similar to SOI CMOS processes, to apply higher supply voltages without compromising the speed of transistors. This indicates a future trend to address the need for simultaneously high-voltage and high-speed GaN processes.

A limitation of the current GaN processes is their low integration capabilities which hinders to leverage all expected potentials of an integrated circuit process. The most important issues are the large size of transistors, the limited number of metal layers, the low MIM capacitance density in GaN compared to CMOS processes, the availability of only one transistor type for high-power operation, the inaccuracy of the transistor models, e.g., in the subthreshold and non-nominal supply voltages, and the low yield of large GaN chips. These issues should be addressed in future developments to allow the implementation of more complicated GaN circuits and systems with higher levels of functionality.

B. CIRCUIT LEVEL

In the circuit level, there are only a few well-established integrated circuit PA architectures which have been used since the first developments of GaN process. The most popular architectures are the reactive matching PAs, in which output signals of multiple transistors are combined to achieve a target output power over a specific frequency band. The reactive matching networks are tuned over the frequency band. The PA usually comprises one driver stage, and more in mm-wave bands. The main challenge in these PAs is the design of interstage matching networks which should math two complex impedances with large impedance transformation ratio [36]. The next popular GaN PA architecture is the nonuniform distributed amplifier, which can achieve extremely broad bandwidths but their efficiency and output power are usually lower than the reactive matching PAs.

This scarcity of the integrated circuit architectures for GaN PAs can be a result of limited research on circuit design in this process which due to high fabrication costs has been limited to a few specific companies and groups. Moreover, limitations of GaN processes including the transistor models, the large size of transistors, and the low yields of large GaN chips prevent

rapid developments in GaN integrated circuits compared to CMOS processes. Possible improvements in GaN processes in the future can open up opportunities for the realization of novel circuit architectures and functionalities to leverage potentials of this promising process.

V. CONCLUSION

In this article, we presented a review of recent developments in GaN integrated circuits power amplifiers (PAs). The progresses of GaN transistors to reach the current state of performance were discussed. The GaN integrated circuit PA architectures and state-of-the-art in output power in RF and mm-wave frequency bands were investigated. Moreover, we presented future perspectives on the possible improvements in the GaN transistors and circuit architectures to leverage potentials of this process.

REFERENCES

[1] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764–1783, Jun. 2012.

[2] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002, doi: 10.1109/JPROC.2002.1021567.

[3] J. J. Komiak, "GaN HEMT: Dominant force in high-frequency solid-state power amplifiers," *IEEE Microw. Mag.*, vol. 16, no. 3, pp. 97–105, Apr. 2015, doi: 10.1109/MMM.2014.2385303.

[4] C. F. Campbell, A. Balistreri, M.-Y. Kao, D. C. Dumka, and J. Hitt, "GaN takes the lead," *IEEE Microw. Mag.*, vol. 13, no. 6, pp. 44–53, Sep./Oct. 2012, doi: 10.1109/MMM.2012.2205829.

[5] M. Khan, J. van Hove, J. Kuznia, and D. Olson, "High electron mobility GaN/AlGaN heterostructure grown by low-pressure metal organic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 58, pp. 2408–2410, Mar. 1991.

[6] M. Khan, J. Kuznia, J. van Hove, N. Pan, and J. Carter, "Observation of a two-dimensional electron gas in low-pressure metalorganic chemical vapor deposited GaN/AlGaN heterojunctions," *Appl. Phys. Lett.*, vol. 60, no. 24, pp. 3027–3029, 1992.

[7] S. Strite and H. Morkoc, "AlN GaN, and InN: A review," *J. Vac. Sci. Technol.*, vol. 10, pp. 1237–1266, Mar. 1992.

[8] E. R. Dobrovinskaya, L. A. Lytvynov, and V. Pishchik, *Sapphire: Material, Manufacturing, Applications*. Berlin, Germany: Springer-Verlag, 2009.

[9] S. Y. Sheppard et al., "High power microwave GaN/AlGaN HEMT's on semi-insulating silicon carbide substrates," *IEEE Electron Device Lett.*, vol. 20, no. 4, pp. 161–163, Apr. 1999.

[10] J. J. Xu et al., "1–8 GHz GaN-based power amplifier using flip-chip bonding," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 7, pp. 277–279, Jul. 1999.

[11] Y.-F. Wu, R. A. York, S. Keller, B. P. Keller, and U. K. Mishra, "3–9 GHz GaN-based microwave power amplifiers with L-C-R broadband matching," *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 8, pp. 314–316, Aug. 1999.

[12] Y.-F. Wu, D. Wapolnek, J. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "14-W GaN-based microwave power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2000, pp. 963–965.

[13] S. Lee, B. Green, K. Chu, K. Webb, and L. Eastman, "Demonstration of a high efficiency nonuniform monolithic gallium-nitride distributed amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2000, pp. 549–552.

[14] T. Paskova and K. R. Evans, "GaN substrates—Progress, status, and prospects," *IEEE J. Sel. Topics Quantum Electron.*, vol. 15, no. 4, pp. 1041–1052, Jul./Aug. 2009, doi: 10.1109/JSTQE.2009.2015057.

[15] G. H. Jessen et al., "AlGaN/GaN HEMT on diamond technology demonstration," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2006, pp. 271–274, doi: 10.1109/CSICS.2006.319952.

[16] K. J. Chen et al., "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.

[17] X. Li et al., "200 V. enhancement-mode p-GaN HEMTs fabricated on 200 mm GaN-on-SOI with trench isolation for monolithic integration," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 918–921, Jul. 2017, doi: 10.1109/LED.2017.2703304.

[18] X. Li et al., "GaN-on-SOI: Monolithically integrated All-GaN ICs for power conversion," in *Proc. IEEE Int. Electron Devices Meeting*, 2019, pp. 4.4.1–4.4.4, doi: 10.1109/IEDM19573.2019.8993572.

[19] R. Quay, *Gallium Nitride Electronics* (Material Science Series). Berlin, Germany: Springer-Verlag, 2008.

[20] K. Shinohara et al., "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 2982–2996, Oct. 2013.

[21] Y.-F. Wu et al., "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004.

[22] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 161–163, Apr. 2004.

[23] S. L. Selvaraj, A. Watanabe, A. Wakejima, and T. Egawa, "1.4-kV breakdown voltage for AlGaN/GaN high-electron-mobility transistors on silicon substrate," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1375–1377, Oct. 2012, doi: 10.1109/LED.2012.2207367.

[24] L. Dunleavy, C. Baylis, W. Curtice, and R. Connick, "Modeling GaN: Powerful but challenging," *IEEE Microw. Mag.*, vol. 11, no. 6, pp. 83–96, Oct. 2010.

[25] I. Angelov, H. Zirath, and N. Rorsman, "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Trans. Microw. Theory Techn.*, vol. 40, no. 12, pp. 2258–2266, Dec. 1992.

[26] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proc. IEEE*, vol. 90, no. 6, pp. 1048–1058, Jun. 2002.

[27] J. B. King and T. J. Brazil, "Nonlinear electrothermal GaN HEMT model applied to high-efficiency power amplifier design," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 444–454, Jan. 2013, doi: 10.1109/TMTT.2012.2229712.

[28] U. Radhakrishna, D. Piedra, Y. Zhang, T. Palacios, and D. Antoniadis, "High voltage GaN HEMT compact model: Experimental verification, field plate optimization and charge trapping," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, 2013, pp. 1–4, doi: 10.1109/IEDM.2013.6724740.

[29] S. Khandelwal et al., "Robust surface-potential-based compact model for GaN HEMT IC design," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3216–3222, Oct. 2013, doi: 10.1109/TED.2013.2265320.

[30] [Online]. Available: https://www.qorvo.com/products/amplifiers/power-amplifiers

[31] [Online]. Available: https://www.wolfspeed.com/products/rf/

[32] K. Shinohara et al., "220 GHz fT and 400 GHz fmax in 40-nm GaN DH-HEMTs with re-grown ohmic," in *Proc. Int. Electron Devices Meeting*, 2010, pp. 1–4, doi: 10.1109/IEDM.2010.5703448.

[33] W. Xing et al., "InAlN/GaN HEMTs on Si with high f_T of 250 GHz," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 75–78, Jan. 2018, doi: 10.1109/LED.2017.2773054.

[34] L. Li et al., "GaN HEMTs on Si with regrown contacts and cutoff/maximum oscillation frequencies of 250/204 GHz," *IEEE Electron Device Lett.*, vol. 41, no. 5, pp. 689–692, May 2020, doi: 10.1109/LED.2020.2984727.

[35] Y. Tang et al., "Ultrahigh-speed GaN high-electron-mobility transistors with f_T/f_{max} of 454/444 GHz," *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 549–551, Jun. 2015, doi: 10.1109/LED.2015.2421311.

[36] G. Nikandish and A. Medi, "A design procedure for high-efficiency and compact-size 5–10-W MMIC power amplifiers in GaAs pHEMT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2922–2933, Aug. 2013, doi: 10.1109/TMTT.2013.2271997.

[37] G. R. Nikandish, A. Nasri, A. Yousefi, A. Zhu, and R. B. Staszewski, "A broadband fully integrated power amplifier using waveform shaping multi-resonance harmonic matching network," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 1, pp. 2–15, Jan. 2022, doi: 10.1109/TCSI.2021.3095708.

[38] G. R. Nikandish, R. B. Staszewski, and A. Zhu, "Broadband fully integrated GaN power amplifier with minimum-inductance BPF matching and two-transistor AM-PM compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 4211–4223, Dec. 2020, doi: 10.1109/TCSI.2020.3002395.

[39] G. Nikandish, R. B. Staszewski, and A. Zhu, "Design of highly linear broadband continuous mode GaN MMIC power amplifiers for 5G," *IEEE Access*, vol. 7, pp. 57138–57150, 2019, doi: 10.1109/ACCESS.2019.2914563.

[40] A. Alexander and J. Leckey, "A 120 watt GaN power amplifier MMIC utilizing harmonic tuning circuits for S-band applications," in *Proc. IEEE MTT-S Int. Microw. Symp.*, 2015, pp. 1–3, doi: 10.1109/MWSYM.2015.7167045.

[41] C. Florian, R. Cignani, A. Santarelli, and F. Filicori, "Design of 40-W AlGaN/GaN MMIC high power amplifiers for C-band SAR applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4492–4504, Dec. 2013, doi: 10.1109/TMTT.2013.2286109.

[42] H. Xie, Y. J. Cheng, Y. R. Ding, L. Wang, and Y. Fan, "A C-band high-efficiency power amplifier MMIC with second-harmonic control in 0.25 μm GaN HEMT technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 12, pp. 1303–1306, Dec. 2021, doi: 10.1109/LMWC.2021.3106196.

[43] Y. Xu et al., "A scalable large-signal multiharmonic model of AlGaN/GaN HEMTs and its application in C-band high power amplifier MMIC," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 8, pp. 2836–2846, Aug. 2017, doi: 10.1109/TMTT.2017.2669984.

[44] H.-Q. Tao, W. Hong, B. Zhang, and X.-M. Yu, "A compact 60 W X-band GaN HEMT power amplifier MMIC," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 1, pp. 73–75, Jan. 2017, doi: 10.1109/LMWC.2016.2630926.

[45] J. Kamioka, Y. Tarui, Y. Kamo, and S. Shinjo, "54% PAE, 70-W X-band GaN MMIC power amplifier with individual source via structure," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 12, pp. 1149–1152, Dec. 2020, doi: 10.1109/LMWC.2020.3031273.

[46] P. Colantonio, M. Lopez, L. Cabria, F. Vitobello, and R. Giofrè, "10 W high efficiency GaN-Si MMIC power amplifier for 17.3-20.2 GHz onboard satellite use," in *Proc. IEEE/MTT-S Int. Microw. Symp.*, 2022, pp. 775–777, 10.1109/IMS37962.2022.9865599.

[47] Y. S. Noh and I. B. Yom, "A linear GaN high power amplifier MMIC for Ka-band satellite communications," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 8, pp. 619–621, Aug. 2016, doi: 10.1109/LMWC.2016.2585553.

[48] M. R. Duffy, G. Lasser, G. Nevett, M. Roberg, and Z. Popovic, "A three-stage 18.5–24-GHz GaN-on-SiC 4 W. 40% efficient MMIC PA," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2402–2410, Sep. 2019.

[49] C. F. Campbell, M.-Y. Kao, and S. Nayak, "High efficiency Ka-band power amplifier MMICs fabricated with a 0.15 μm GaN on SiC HEMT process," in *IEEE MTT-S Int. Microw. Symp. Dig*., 2012, pp. 1–3.

[50] S. Din, M. Wojtowicz, and M. Siddiqui, "High power and high efficiency Ka band power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig*., 2015, pp. 1–4.

[51] G. Nikandish, E. Babakrpur, and A. Medi, "A harmonic termination technique for single- and multi-band high-efficiency class-f MMIC power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 5, pp. 1212–1220, May 2014, doi: 10.1109/TMTT.2014.2315591.

[52] A. Grebennikov and S. Bulja, "High-efficiency Doherty power amplifiers: Historical aspect and modern trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.

[53] G. Nikandish, R. B. Staszewski, and A. Zhu, "Breaking the bandwidth limit: A review of broadband Doherty power amplifier design for 5G," *IEEE Microw. Mag.*, vol. 21, no. 4, pp. 57–75, Apr. 2020, doi: 10.1109/MMM.2019.2963607.

[54] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and N. Rorsman, "A wideband and compact GaN MMIC Doherty amplifier for microwave link applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922–930, Feb. 2013.

[55] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and C. Fager, "A GaN MMIC modified Doherty PA with large bandwidth and reconfigurable efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3006–3016, Dec. 2014.

[56] G. Nikandish, R. B. Staszewski, and A. Zhu, "Bandwidth enhancement of GaN MMIC Doherty power amplifiers using broadband transformer-based load modulation network," *IEEE Access*, vol. 7, pp. 119844–119855, 2019, doi: 10.1109/ACCESS.2019.2937388.

[57] V. Camarchia, J. Fang, J. J. Moreno Rubio, M. Pirola, and R. Quaglia, "7 GHz MMIC GaN Doherty power amplifier with 47% efficiency at 7 dB output back-off," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 1, pp. 34–36, Jan. 2013.

[58] R.-J. Liu et al., "A 24–28-GHz GaN MMIC synchronous Doherty power amplifier with enhanced load modulation for 5G mm-wave applications," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 8, pp. 3910–3922, Aug. 2022, doi: 10.1109/TMTT.2022.3176818.

[59] M. Bao, D. Gustafsson, R. Hou, Z. Ouarch, C. Chang, and K. Andersson, "A 24–28-GHz Doherty power amplifier with 4-W output power and 32% PAE at 6-dB OPBO in 150-nm GaN technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 752–755, Jun. 2021, doi: 10.1109/LMWC.2021.3063868.

[60] D. J. Shepphard, J. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 6, pp. 443–445, Jun. 2016, doi: 10.1109/LMWC.2016.2559503.

[61] J. R. Powell, D. J. Shepphard, R. Quaglia, and S. C. Cripps, "A power reconfigurable high-efficiency x. -band power amplifier MMIC using the load modulated balanced amplifier technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 6, pp. 527–529, Jun. 2018, doi: 10.1109/LMWC.2018.2824560.

[62] G. R. Nikandish, R. B. Staszewski, and A. Zhu, "Unbalanced power amplifier: An architecture for broadband back-off efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 367–381, Feb. 2021.

[63] V. Camarchia, R. Quaglia, A. Piacibello, D. P. Nguyen, H. Wang, and A.-V. Pham, "A review of technologies and design techniques of millimeter-wave power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2957–2983, Jul. 2020, doi: 10.1109/TMTT.2020.2989792.

[64] J. Moron, R. Leblanc, F. Lecourt, and P. Frijlink, "12 W, 30% PAE, 40 GHz power amplifier MMIC using a commercially available GaN/Si process," in *Proc. IEEE/MTT-S Int. Microw. Symp.*, 2018, pp. 1457–1460, doi: 10.1109/MWSYM.2018.8439689.

[65] W. Wang, F. Guo, T. Chen, and K. Wang, "24.8 A. W-band power amplifier with distributed common-source GaN HEMT and 4-Way Wilkinson-Lange combiner achieving 6 W output power and 18% PAE at 95 GHz," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2020, pp. 376–378, doi: 10.1109/ISSCC19947.2020.9063161.

[66] W. Shaobing, G. Jianfeng, W. Weibo, and Z. Junyun, "W-band MMIC PA with ultrahigh power density in 100-nm AlGaN/GaN technology," *IEEE Trans. Electron Devices*, vol. 63, no. 10, pp. 3882–3886, Oct. 2016, doi: 10.1109/TED.2016.2597244.

[67] A. Margomenos et al., "GaN technology for E., W and G-band applications," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, La Jolla, CA, USA, 2014, pp. 1–4.

[68] A. Kurdoghlian et al., "First demonstration of broadband W-band and D-band GaN MMICs for next generation communication systems," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Honolulu, HI, USA, 2017, pp. 1126–1128.

[69] M. Cwiklinskiy et al., "Full W-band GaN power amplifier MMICs using a novel type of broadband radial stub," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5664–5675, Dec. 2018.

[70] M. Cwiklinski et al., "D-band and G-band high-performance GaN power amplifier MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 12, pp. 5080–5089, Dec. 2019, doi: 10.1109/TMTT.2019.2936558.

[71] M. Cwiklinski et al., "First demonstration of G-band broadband GaN power amplifier MMICs operating beyond 200 GHz," in *Proc. IEEE/MTT-S Int. Microw. Symp.*, 2020, pp. 1117–1120, doi: 10.1109/IMS30576.2020.9224041.

[72] A. Wentzel, S. Chevtchenko, P. Kurpas, and W. Heinrich, "A flexible GaN MMIC enabling digital power amplifiers for the future wireless infrastructure," in *Proc. IEEE MTT-S Int. Microw. Symp.*, 2015, pp. 1–4, doi: 10.1109/MWSYM.2015.7166795.00.

[73] G. R. Nikandish, R. B. Staszewski, and A. Zhu, "A fully integrated reconfigurable multimode Class-$F_{2,3}$ GaN power amplifier," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 270–273, 2020, doi: 10.1109/LSSC.2020.3013430.

[74] L. Kang, W. Chen, and A. Wu, "A reconfigurable S-/X-band GaN MMIC power amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 6, pp. 547–550, Jun. 2022, doi: 10.1109/LMWC.2022.3141230.

[75] G. Nikandish, R. B. Staszewski, and A. Zhu, "The (R)evolution of distributed amplifiers: From vacuum tubes to modern CMOS and GaN ICs," *IEEE Microw. Mag.*, vol. 19, no. 4, pp. 66–83, Jun. 2018, doi: 10.1109/MMM.2018.2813838.

[76] J. Chen and A. M. Niknejad, "Design and analysis of a stage-scaled distributed power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 5, pp. 1274–1283, May 2011.

[77] M. Roberg, J. Zhang, R. Flynt, and M. Irvine, "A 50 W CW 1–6 GHz GaN MMIC power amplifier module with greater than 30% power added efficiency," in *Proc. IEEE/MTT-S Int. Microw. Symp.*, 2022, pp. 426–428, doi: 10.1109/IMS37962.2022.9865433.

[78] C. Campbell et al., "A wideband power amplifier MMIC utilizing GaN on SiC HEMT technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2640–2647, Oct. 2009.

[79] R. Santhakumar et al., "Two-stage high-gain high-power distributed amplifier using dual-gate GaN HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 8, pp. 2059–2063, Aug. 2011.

[80] S. Masuda et al., "Over 10 W. C-Ku band GaN MMIC non-uniform distributed power amplifier with broadband couplers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2010, pp. 1388–1391.

[81] H.-F. Wu et al., "A compact ultrabroadband stacked traveling-wave GaN on Si power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 7, pp. 3306–3314, Jul. 2018, doi: 10.1109/TMTT.2018.2828434.

[82] P. Dennler, D. Schwantuschke, R. Quay, and O. Ambacher, "8–42 GHz GaN non-uniform distributed power amplifier MMICs in microstrip technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2012, pp. 1–4.

[83] J. M. Schellenberg, "A 2-W W-band GaN traveling-wave amplifier with 25-GHz bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2833–2840, Sep. 2015.

[84] G. Nikandish and A. Medi, "Unilateralization of MMIC distributed amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3041–3052, Dec. 2014.

[85] J. Komiak, K. Chu, and P. C. Chao, "Decade bandwidth 2 to 20 GHz GaN HEMT power amplifier MMICs in DFP and No FP technology," in *IEEE MTT-S Int. Microw. Symp. Dig*., 2011, pp. 1–4.

[86] K. W. Kobayashi, D. Denninghoff, and D. Miller, "A novel 100 MHz-45 GHz input-termination-less distributed amplifier design with low-frequency low-noise and high linearity implemented with a 6 inch 0.15 μm GaN-SiC wafer process technology," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2017–2026, Sep. 2016.

[87] G. Nikandish and A. Medi, "A 40-GHz bandwidth tapered distributed LNA," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 11, pp. 1614–1618, Nov. 2018, doi: 10.1109/TCSII.2017.2758861.

[88] S. Colangeli, A. Bentini, W. Ciccognani, E. Limiti, and A. Nanni, "GaN-based robust low-noise amplifiers," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3238–3248, Oct. 2013, doi: 10.1109/TED.2013.2265718.

[89] F. Thome, P. Brückner, S. Leone, and R. Quay, "A wideband E/W-band low-noise amplifier MMIC in a 70-nm gate-length GaN HEMT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 2, pp. 1367–1376, Feb. 2022, doi: 10.1109/TMTT.2021.3134645.

[90] A. M. Darwish et al., "Multi-octave GaN MMIC circulator for simultaneous transmit receive applications," in *Proc. IEEE/MTT-S Int. Microw. Symp.*, 2018, pp. 417–419, doi: 10.1109/MWSYM.2018.8439451.

[91] D. Yan and D. B. Ma, "A monolithic GaN power IC with on-chip gate driving, level shifting, and temperature sensing, achieving direct 48-V/1-V DC–DC conversion," *IEEE J. Solid-State Circuits*, early access, Sep. 13, 2022, doi: 10.1109/JSSC.2022.3201781.

[92] T. Kim, H. Im, S.-H. Lee, K.-J. Kim, and C. Park, "Highly linear K-/Ka-band SPDT switch based on traveling-wave concept in a 150-nm GaN pHEMT process," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 8, pp. 987–990, Aug. 2022, doi: 10.1109/LMWC.2022.3161498.

[93] F. Thome, P. Brückner, R. Quay, and O. Ambacher, "Millimeter-wave single-pole double-throw switches based on a 100-nm gate-length AlGaN/GaN-HEMT technology," in *Proc. IEEE MTT-S Int. Microw. Symp.*, 2019, pp. 1403–1406, doi: 10.1109/MWSYM.2019.8700955.

[94] C. F. Campbell, J. C. Hitt, and K. Wills, "Wideband GaN FET based limiter MMICs," in *Proc. 7th Eur. Microw. Integr. Circuit Conf.*, 2012, pp. 417–420.

[95] T. N. Ross, K. Hettak, G. Cormier, and J. S. Wight, "Design of X-band GaN phase shifters," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 1, pp. 244–255, Jan. 2015, doi: 10.1109/TMTT.2014.2366149.

[96] R. Giofrè et al., "S-band GaN single-chip front end for active electronically scanned array with 40-W output power and 1.75-dB noise figure," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5696–5707, Dec. 2018, doi: 10.1109/TMTT.2018.2861716.

[97] M. van Heijningen et al., "C-band single-chip radar front-end in AlGaN/GaN technology," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4428–4437, Nov. 2017, doi: 10.1109/TMTT.2017.2688438.

[98] P. Choi et al., "A 5.9-GHz fully integrated GaN frontend design with physics-based RF compact model," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1163–1173, Apr. 2015, doi: 10.1109/TMTT.2015.2405913.

[99] B. Kim and V. Z.-Q. Li, "39 GHz GaN front end MMIC for 5G applications," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2017, pp. 1–4, doi: 10.1109/CSICS.2017.8240473.

[100] D. S. Green, C. L. Dohrman, J. Demmin, Y. Zheng, and T.-H. Chang, "A revolution on the horizon from DARPA: Heterogeneous integration for revolutionary microwave/millimeter-wave circuits at DARPA: Progress and future directions," *IEEE Microw. Mag.*, vol. 18, no. 2, pp. 44–59, Mar./Apr. 2017, doi: 10.1109/MMM.2016.2635811.

REZA NIKANDISH (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2014. He is currently an Assistant Professor with University College Dublin, Dublin, Ireland. His research interests include integrated circuits for communication and sensing, intelligent sensors for human-computer interaction and health monitoring, and quantum computing. He was a recipient of the Marie Curie Post-Doctoral Fellowship from the European Union's Horizon 2020 Research and Innovation Program in 2017, the National Elites Foundation Ph.D. Fellowship in 2010, and the Silver Medal of the National Electrical Engineering Olympiad in 2004. He is a member of scientific communities IEEE Solid-State Circuits, Signal Processing, Microwave Theory and Technology, and Sensors Council.