26th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2019)

2 July – 5 July 2019
Grand Hyatt Hotel, Hangzhou, China

Technically Co-sponsored by

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Content

Welcoming Address **1**

IPFA Board **2**

Committee Members **2**

Technical Program Committee **3**

Special speakers **7**

General Information **8**

Map of the Conference Zone **10**

Sponsor **11**

Map of the Exhibition Zone — Exhibition Hall **13**

List of Exhibitors & Booth **14**

Exhibitors' Information **15**

Keynote speakers **31**

Tutorials speakers **33**

Invited speakers **41**

Technical Program **60**

Poster Paper Information **71**

Welcoming Address

Dear IPFA2019 participants,

On behalf of the organizing committees from both China and Singapore, you are cordially invited to attend the 26th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits - IPFA. IPFA is an international conference which has been one of the major conferences in the reliability and failure analysis of devices and integrated circuits. This has been the 26th in its series and organized by the IEEE EDS Hangzhou Chapter and the IEEE Singapore Reliability/CPMT/ED Chapter. The Symposium is technically co-sponsored by the IEEE Electron Devices Society. This year the symposium will be held in Hangzhou, China.

In this symposium we have received more than 201 submissions from 15 countries, in which 54 papers were selected for oral presentations, and 101 for poster presentations. We have also 19 invited talks, along with two outstanding exchange papers contributed from ISTFA and ESREF 2018, respectively. We are also delighted to have two distinguished keynote speakers for the plenary session. Dr. Prasad Chaparala, Amazon Lab126, will speak on "Building Reliable Products Guided by Customer Obsession" and Dr. Shimeng Yu, Georgia Institute of Technology, will address on "Emerging Non-Volatile Memory's Applications in Neuro-Inspired Computing and Hardware Security". The events of IPFA 2019 include a one-day tutorial, 3 days technical paper presentation, and concurrently with exhibition from worldwide vendors. A one-day tutorial, scheduled for Tuesday, July 2, will cover seven topics in two parallel sessions. This brings up an excellent opportunity for experienced as well as engineers, scholars, professors, and students, to broaden their technical knowledge in both reliability and failure analysis techniques. Vendor exhibits presenting state-of-the-art advanced techniques and equipments on the failure analysis, testing and measurement equipments etc., which are held throughout the whole conference.

This year's symposium will not be possible without continuing support from the IPFA board in Singapore, the exhibit vendors, paper review from our program committee members, and the contributed papers from our authors. Especially, we would like to express our sincere gratitude to everyone who contributed numerous efforts of the local arrangements, especially thanks to the Program Chair, Dr. Zhiwei Liu and co-chairs, Dr. Wardhana A. Sasangka and Dr. Youlin Wu, for their dedication of hard-work in paper selections, as well as those more than 60 world experts technical committee members, in the field of reliability. Finally, special thank goes to Jasmine Leong for her help in the transformation and sharing the information from the Singapore team in their past years' experience.

We expect a truly international forum for this exciting conference. Enjoy the conference, enjoy the friendship, and enjoy your stay in Hangzhou!

2nd July, 2019

Dr. Juin J.Liou
General Chair

Dr. Nagarajan Raghavan
General Co-Chair

IPFA Board

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	John Thong (NUS, Singapore)

Track 2: Case Studies on Fault Isolation

Chair	**Christian Boit** (Technical University Berlin, Germany)
Co-Chair	**Alfred Quah** (GlobalFoundries, Singapore)
Member	**Hirotoshi Terada** (Hamamatsu, Japan)
	Szu Huat Goh (GlobalFoundries, Singapore)
	Zhongling Qian (Infineon, USA)
	Amit Jakati (GlobalFoundries, Singapore)
	Joshua Kevek (Intel, USA)

Track 3: Case Studies on Physical Failure Analysis

Chair	**Alan Street** (On Semiconductor, China)
Co-Chair	**Ingrid De Wolf** (IMEC, Belgium)
Member	**James Lee** (TSMC, Taiwan)
	Olivier Latry (University of Rouen Normandy, France)
	Eckhard Langer (GlobalFoundries, Germany)
	Ruby Vollrath (Qualcomm, USA)

Track 4: Package-Level Failure Analysis

Chair	**Susan Li** (Cypress, USA)
Co-Chair	**Jiann Min Chin** (AMD, Singapore)
Member	**Bernice Zee** (AMD, Singapore)
	Wentao Qin (On Semiconductor, USA)
	Peter Jacob (EMPA, Switzerland)
	Yan Li (Intel, USA)
	Em Julius Dela Cruz (Maxim Integrated, Philippines)
	Liyi Li (Intel, USA)

Technical Program Committee

Track 5: Advanced Electrical Fault Isolation Techniques

Chair	**Venkat Krishnan Ravikumar** (AMD, Singapore)
Member	**Phillippe Perdu** (CNES, France)
	Kris Dickson (NXP, USA)
	Mike Bruce (Consultant, USA)
	Christopher Nemirow (Thermofisher, USA)

Track 6: Advanced Physical Failure Analysis Techniques

Chair	**Christian Hobert** (GlobalFoundries, Germany)
Member	**Umberto Celano** (IMEC, Belgium)
	Chen Changqing (GlobalFoundries, Singapore)
	Michael DiBattista (VarioScale, USA)
	Hongwen He (Hisilicon Technologies, China)
	Jayhoon Chung (Texas Instruments, USA)

Track 7: Emerging Topics in Failure Analysis

Chair	**Zhigang Ji** (Liverpool John Moores University, UK)
Co-Chair	**Samuel Chef** (NTU, Singapore)
Member	**Cheryl Hartfield** (ZEISS, USA)
	Wen Qiu (AMD, Singapore)
	Chee Lip Gan (NTU, Singapore)
	Hong Yang (IMECAS, China)
	Bin Gao (Tsinghua University, China)
	Sun Litao (Southeast University, China)
	Du Anyan (IMECAS, China)
	Changze Liu (Huawei Technologies, China)

Track 8: Transistor and NVM Device Reliability

Chair	**Runsheng Wang** (Peking University, China)
Co-Chair	**Mario Lanza** (Soochow University, China)
Member	**Jim Stathis** (IBM, USA)
	Jianfu Zhang (Liverpool John Moores University, UK)
	Shubhakar Kalya (SUTD, Singapore)
	Kaikai Xu (UESTC, China)
	Felix Palumbo (National Tech. University (UTN), Argentina)
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Ming Liu (IMECAS, China)
Mingxiang Wang (Soochow University, China)
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Subhali Subhechha (IMEC, Belgium)
Marco Villena (Soochow University, China)
You-Lin Wu (National Chi Nan University, Taiwan)
Wei Zhang (Liverpool John Moores University, UK)
Wei Liang (GlobalFoundries, USA)

Track 9: Interconnect and Packaging Reliability

Chair	**Jeffrey Gambino** (ON Semiconductor, USA)
Co-Chair	**Rongxiang Wu** (UESTC, China)
Member	**Lim Yeow Kheng** (STATSChipPAC, Singapore)
	Kristof Croes (IMEC, Belgium)
	Tam Lyn Tan (GlobalFoundries, Singapore)
	Kuan-Neng Chen (NCTU, Taiwan)
	Wenqi Zhang (NCAP, China)
	Hajdin Ceric (TU Wien, Austria)
	Valeriy Sukharev (Mentor Graphics, USA)
	Wardhana A. Sasangka (Singapore-MIT Alliance for Research and Technology, Singapore)
	Christine Hau-Riege (Qualcomm, USA)

Technical Program Committee

Track 10: Photovoltaic Device Reliability and Failure Analysis

Member	**Zhang Li** (Singapore-MIT Alliance for Research and Technology, Singapore)
	Kunal Mukherjee (University of California, Santa Barbara, USA)
	Arief Suriadi Budiman (SUTD, Singapore)
	Ariya Sangwongwanich (Aalborg University, Denmark)
	Rongshan Wei (Fuzhou University, China)
	Yang Xu (Zhejiang University, China)
	Andrew Tay (SUTD, Singapore)
	Kristof Croes (IMEC, Belgium)

Track 11: High Power Electronics/Wide Bandgap Device Reliability and Failure Analysis

Chair	**Min Ren** (UESTC, China)
Co-Chair	**Wardhana A. Sasangka** (Singapore-MIT Alliance for Research and Technology, Singapore)
Member	**Francesco Iannuzo** (Aalborg University, Denmark)
	Tian-Li Wu (National Chiao Tung University, Taiwan)
	Martin Kuball (University of Bristol, UK)
	Siyang Liu (Southeast University, China)
	Wangran Wu (Southeast University, China)
	Jinping Zhang (UESTC, China)
	Bhawani Shankar (Indian Institute of Science, India)
	Zhongling Qian (Infineon, Germany)
	Matteo Meneghini (University of Padova, Italy)
	Guoqiao Tao (Ampleon, Netherlands)

Track 12: 2D Materials and Devices: Reliability and Failure Analysis

Chair	**Yang Xu** (Zhejiang University, China)
Co-Chair	**Wu Xing** (ECNU, China)
Member	**Kah Wee Ang** (National University of Singapore (NUS), Singapore)
	Alok Ranjan (SUTD, Singapore)
	Fei Hui (Technion-Israel Institute of Technology, Israel)
	Yuanyuan Shi (Technion-Israel Institute of Technology, Israel)

Special speakers

Keynote speakers:

Prasad Chaparala (Amazon Lab126, USA)
Shimeng Yu (Georgia Institute of Technology, USA)

Tutorials:

Dimitris P. Ioannou (GlobalFoundries, USA)
David Su (Taiwan Semiconductor Manufacturing Company, Taiwan)
Jianfu Zhang (Liverpool John Moores University, UK)
Lihong Cao (ASE Group, TX, USA)
Francesco Iannuzzo (Aalborg University, Denmark)
Venkat Krishnan Ravikumar (AMD, Singapore)
Baozhen Li (IBM System and Technology Group, Essex Vermont, USA)
Szu Huat Goh (GlobalFoundries, Singapore)

Invited speakers:

Jianfu Zhang (Liverpool John Moores University, UK)
Lihong Cao (ASE Group, Austin, TX, USA)
Mu-Chun Wang (Minghsin University of Science and Technology, Taiwan)
Baozhen Li (IBM System and Technology Group, Essex Vermont, USA)
Venkat Krishnan Ravikumar (AMD, Singapore)
You Li (GlobalFoundries, USA)
Christian Boit (TU Berlin, Germany)
You Wang (Beihang University, China)
Ching-Chun Lin (Integrated Service Technology, Taiwan)
Francesco Iannuzzo (Aalborg University, Denmark)
David Su (Taiwan Semiconductor Manufacturing Company, Taiwan)
Xing Zhou (Nanyang Technological University, Singapore)
Sun Litao (South East University, China)
Dimitris P. Ioannou (GlobalFoundries, USA)
Yury Illarionov (TU Wien, Austria)
Wu Xing (East China Normal University, China)
Bin Gao (Tsinghua University, China)
Mario Lanza (Soochow University, China)
Kosuke Nagashio (University of Tokyo, Japan)

General Information

Venue of Conference

Grand Hyatt Hangzhou
28 Hubin Rd, HuBin ShangQuan, Shangcheng Qu, Hangzhou Shi, Zhejiang Sheng, China.

Registration and Information Desk and Conference Secretariat

The registration and information desk will be arranged at the Reception Desk. The conference secretariat will be set in the Secretary Room from July 2nd to July 5th during the conference.

Poster Presentations

Poster sessions will be arranged at the Poster Zone. Please refer to the Technical Program for your poster number.
Poster are supposed to put up in advance and taken off after the session. Tape is available on request from the Information Desk. Please understand that any poster remaining over the removal time will be disposed after the conference.

Name Badge

For identification purpose, badges are expected to be worn at all times during the conference.

Internet

Wireless connection will be available in the conference theatres. The account for log-in will be provided during the conference.

Meal

From July 2nd to July 5th, lunches will be provided at West Lake Room which is located at the 2nd Floor in Grand Hyatt Hangzhou Hotel. Please bring your lunch coupon with you for lunch. You must show your ticket to the waitress.

Emergency Contact

Please ask the help from the conference information desk.

General Information

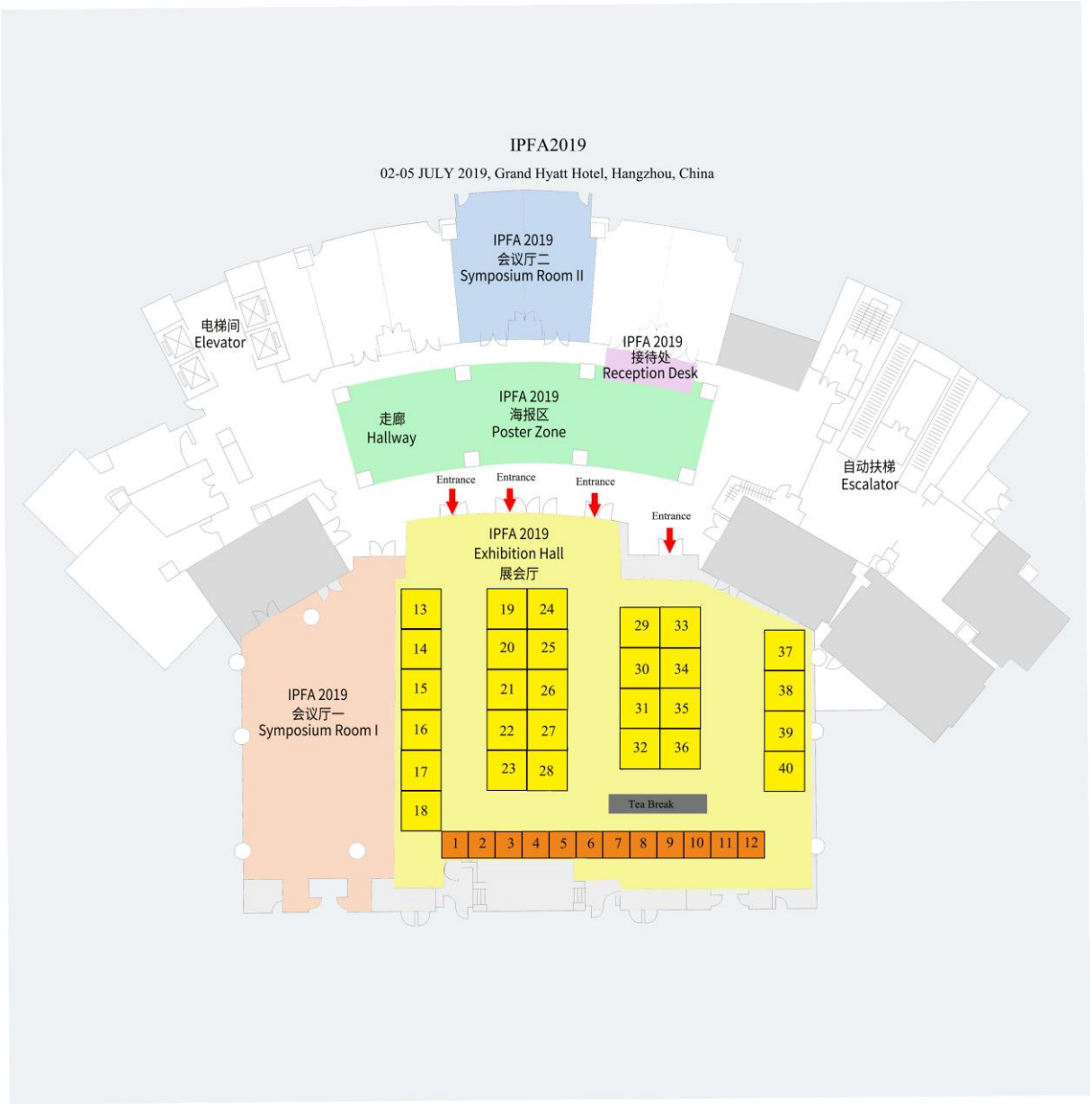
Banquet

The banquet will be held at **Huazhongcheng Banquet Hall**, No.630 Fengqi road, Hangzhou (Southern door of The Zhejiang People's Greathall) and starts from 6:00 PM, July 4th. Please gather at the hotel lobby at 5:40, and we will take you from the Grand Hyatt Hangzhou to the Huazhongcheng Banquet Hall.

The banquet is opened to all of the IPFA2019 attendees. Please get the tickets for banquet upon registration. Please bring the ticket and show it for the events.

Map of the Conference Zone

Please check the Room information by the different color.



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Contact: Paige Tan, Event Manager
Email: paige.tan@thermofisher.com

Thermo Fisher Scientific supplies innovative solutions for electron microscopy and microanalysis. We provide SEMs, TEMs and DualBeam™ FIB/SEMs combined with electrical test solutions and advanced software suites to take customers from electrical localization to physical root cause. Our industry-leading workflows deliver fast, accurate answers for accelerating IC design and production decisions. Our fault isolation and analysis products provide superior images, rich feature sets, cross-sectional metrology and automation to speed process defect identification, enable root-cause analysis, reduce yield loss and accelerate time-to market for new products. Our experts engage with applications, engineering, and manufacturing teams to address today's challenges, while our leadership and significant R&D commitment are paving the way to sub-7–nanometer technologies and beyond.

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Tel: 800-988-0501
Website: www.istgroup.com
E-mail: marketing_cn@istgroup.com

Founded in 2002 in China, iST began its business from IC circuit debugging and modification and gradually expanded its scope of operations. In 2016, iST established a fully integrated circuit supply chain verification and analysis engineering service platform in Shanghai to provide comprehensive services for failure analysis, reliability verification, wafer microstructure material analysis, board level reliability test and wafer grinding so on.
iST's customers cover the whole spectrum of the electronics industry from IC design, wafer manufacturing, IC packaging and testing to end products. In response to rising Cloud Intelligence (AI), Internet of Things (IoT) and Internet of Vehicles (IoV), iST not only focuses on core services but also establishes a unique and integrated automotive chip (Single Chip/Multi Chip/System-in-Package), Board Level Reliability Test and Failure Analysis verification platform in mainland China to face the diversified national and international growing trend.

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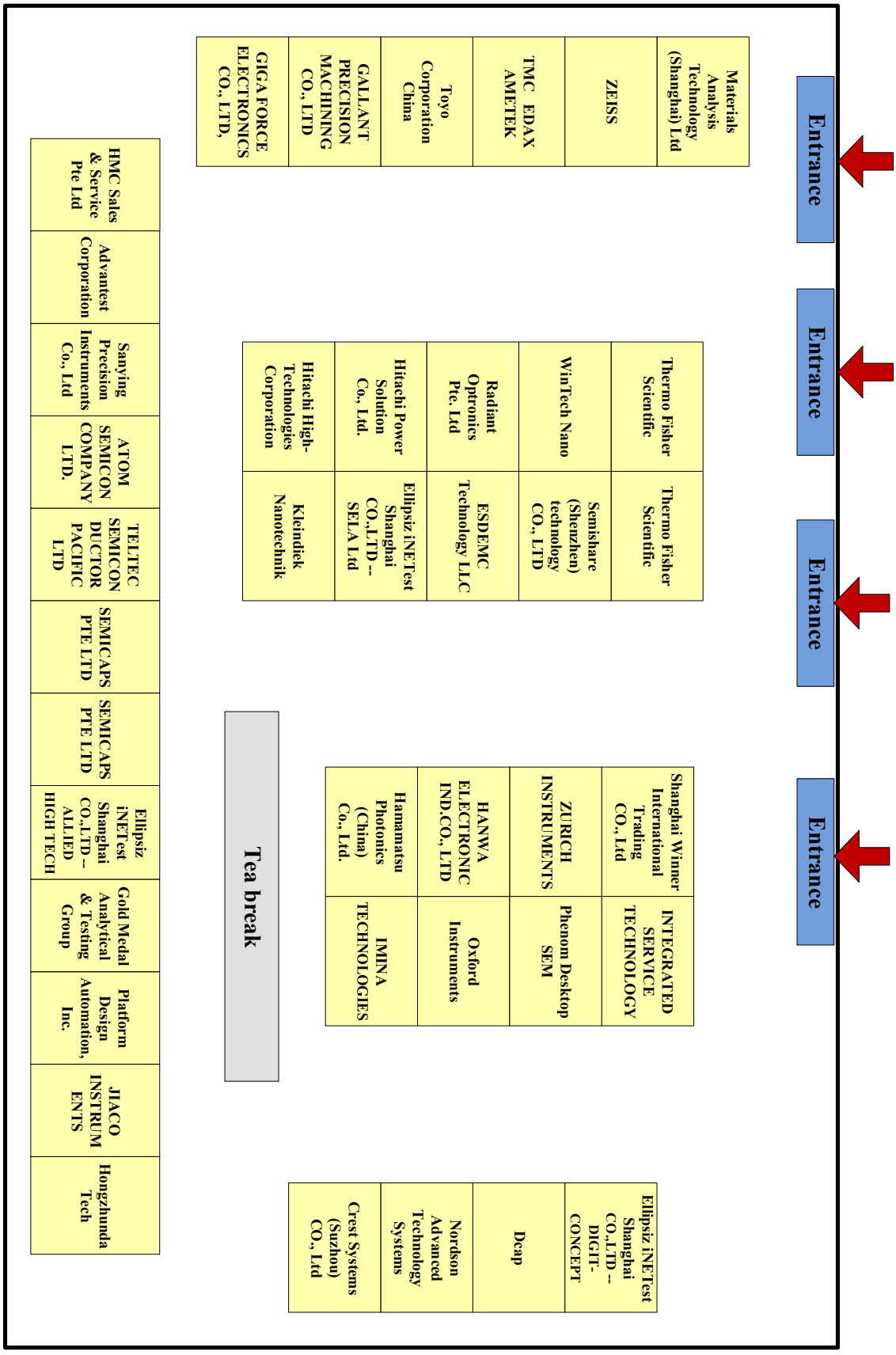
ZEISS has the most comprehensive portfolio of light, x-ray, electron beam and ion beam imaging technologies in the industry and is a leading solution provider to the global semiconductor community. Solutions span semiconductor manufacturing from wafer fab through packaging and assembly. For mask making and lithography, ZEISS provides unique solutions in the areas of zero defect, in-die metrology, critical dimension/registration and overlay control. ZEISS innovative process control and failure analysis solutions deliver actionable information to both wafer fab and packaging/assembly processes to meet the semiconductor industry's challenges for next-generation devices.
ZEISS is represented in over 40 countries around the globe with more than 40 manufacturing sites, around 50 sales and service locations, and over 20 research and development centers. Founded in 1846 in Jena, the company now has its headquarters in Oberkochen in southwest Germany. Carl Zeiss AG is wholly owned by the Carl Zeiss Stiftung (Carl Zeiss Foundation).

Map of the Exhibition Zone — Exhibition Hall

The Exhibitor Presentation Session will be arranged in the Symposium Room I.



List of Exhibitors & Booth

B01	HMC Sales & Service Pte Ltd
B02	Advantest Corporation
B03	Sanying Precision Instruments Co.,Ltd
B04	ATOM SEMICON COMPANY LTD.
B05	TELTEC SEMICONDUCTOR PACIFIC LTD
B06-B07	SEMICAPS PTE LTD
B08	Ellipsiz iNETest Shanghai CO.,LTD -- ALLIED HIGH TECH
B09	Gold Medal Analytical & Testing Group
B10	Platform Design Automation, Inc.
B11	JIACO INSTRUMENTS
B12	Hongzhunda Tech
B13	Materials Analysis Technology (Shanghai) Ltd
B14	ZEISS
B15	AMETEK TMC
B16	Toyo Corporation China
B17	GALLANT PRECISION MACHINING CO.,LTD
B18	GIGA FORCE ELECTRONICS CO.,LTD,
B19,B24	Thermo Fisher Scientific
B20	WinTech Nano
B21	Radiant Optronics Pte. Ltd
B22	Hitachi Power Solutions Co., Ltd
B23	Hitachi High-Technologies Corporation
B25	Semishare (shenzhen) technology CO., LTD
B26	ESDEMC Technology LLC
B27	Ellipsiz iNETest Shanghai CO.,LTD -- SELA Ltd
B28	Kleindiek Nanotechnik
B29	Shanghai Winner International Trading CO., Ltd
B30	ZURICH INSTRUMENTS
B31	HANWA ELECTRONIC IND.CO., LTD
B32	Hamamatsu Photonics (China) Co.,Ltd.
B33	INTEGRATED SERVICE TECHNOLOGY
B34	Phenom Desktop SEM
B35	Oxford Instruments
B36	IMINA TECHNOLOGIES
B37	Ellipsiz iNETest Shanghai CO.,LTD -- DIGIT- CONCEPT
B38	DCap
B39	Nordson Advanced Technology Systems
B40	Crest Systems (Suzhou) CO., Ltd

Exhibitors' Information

HMC Sales & Service China office — Booth No: B01

Room 23005, Blk 8, Manhattan Square No.3, Weihua Road, Suzhou Industrial Park, Suzhou, Jiangsu, China 215021
Tel/Fax: (86) 512-6500-1006
Email: alanhu@hmcasia.com

HMC Sales & Service was established in 1990 and incorporated into a Private Limited company in January 1997 with the aim of providing reliable products and quality services of the highest standard to the regional semiconductor and electronics industry. In June 1997, HMC Sales & Service Philippines was established follow by HMC Sales & Service Suzhou in October 2004.
Both Philippines and Suzhou offices was to provide a closer link with customers in that region and to meet the growing demand and expectation of the semiconductor and electronics market. HMC provide HITACHI Environmental Testing Chambers TC, TS, THB and HIRAYAMA HAST Chamber, Pressure Cooker, Pressurized LCD Liquid Processing Autoclaves. Pressurized Steam Tester, HAST board design/fabrication.

Advantest Corporation — Booth No: B02

A world-class technology company, Advantest is the leading producer of automatic test equipment (ATE) for the semiconductor industry and a premier manufacturer of measuring instruments used in the design and production of electronic instruments and systems. Its leading-edge systems and products are integrated into the most advanced semiconductor production lines in the world. The company also focuses on R&D for emerging markets that benefit from advancements in nanotech and terahertz technologies, and has introduced multi-vision metrology scanning electron microscopes essential to photomask manufacturing, as well as groundbreaking 3D imaging and analysis tools. With the industry's No. 1 test technology capabilities and an internationally-renowned global support system, we pledge to redouble our efforts to grow with our customers around the world, enhance our corporate value, and contribute to a sustainable future for all.

Sanying Precision Instruments Co.,Ltd — Booth No: B03

Building 7, Didadonggu International, 22 Erwei Road, Dongli Economic Development Zone, Tianjin, P.R. China
Tel:0086-15802222209
Contact person: Jian. Wu
Email: jwu_1@sypi.com.cn

Sanying Precision Instruments Co., Ltd. (stock code: 839222) is the first professional manufacturer and supplier of high-resolution intelligent X-ray 3D fluoroscopic imaging testing equipments that has its own intellectual property in China. The Company is mainly engaged in developing and manufacturing of high-resolution X-ray 3D fluoroscopic imaging testing equipment, including X-ray 3D microscope, high-precision X-ray industrial CT scanner, X-ray online testing equipment, lithium battery 3D CT scanner, full core CT scanner, plate CT scanner, 3D digital mobile testing center, and so on. In addition, the Company also provides

nondestructive imaging testing services.
As a national high-tech enterprise, Sanying has passed ISO9001:2008 quality management system certification, has a postdoctoral working station, and has strict quality control and strong R&D capability.
With the concept of "technique innovation, precision manufacture and quality first", the Company is dedicated to build a high-tech industrial platform centered by micro-nano nondestructive testing technology and provide professional solutions for national defense industry, new energy, new material, petroleum geology, aerospace, health and medicine, life science and agricultural technology and so on. Sanying expects to go forward hand in hand with you.

ATOM SEMICON COMPANY LTD. Booth No: B04

B35 1A2, No.1, Lising 1st Rd., East Dist., Hsinchu City 300, Taiwan (R.O.C.)
Tel: +886 3 5788474
Fax: +886 3 5788879
Website: www.atom-semi.com
E-mail: bob.lin@atom-semi.com
Contact person at the exhibition: GM Bob.Lin

ATOM provides professional services for agent products.
ATOM SEMICON was founded by GM Bob.Lin in August 2013. It is the agent for the distribution of Taiwan business of equipment Vendor, and Mr. Wang Wende is the chairman of the company. Focusing on the development of novel application fields, and cooperating with Taiwan's excellent university (NCTU, NCKU...), it has become an equipment vendor novel application field development and professional technology solution provider.
ATOM led equipment vendor products into Taiwan's semiconductor field successfully, equipment vendor product portfolio ranges from fully automated, SEMI compliant batch and cluster systems for high volume manufacturing to smaller scale R&D and pre-pilot production tools. Production-proven solutions for IC, MEMS, LED, Sensor, Biomedical materials and 3D component processing are mastered with world-class process quality, the leading equipment design, the most comprehensive process support, and the best customer care.
In the future, ATOM will continue to agent other leading application technology related products, and keep the professional technical services and industry-university cooperation to provide the best professional development experience and solutions for all future customers.

Teltec Semiconductor Pacific Limited Booth No: B05

Tel: +852 2521 4213
Website: www.teltec.asia

Teltec Semiconductor Pacific Ltd is a leading Sales & Service Organization serving the Semiconductor Industry (Front & Backend) & Emerging Hi-technology Industry (MEMS, Nanotechnology, Opto-electronics & PV Solar) for over 34 years.

Applications of our represented products:
1) Substrate Cleaning: Plasma Cleaning Systems, UVO Cleaners
2) Failure Analysis: SAM, X-ray Inspection Machines, Bond Testers, Decapsulation Systems, IV Curve Tracers, EMMI, IREM
3) Reliability: Burn-in Ovens, Centrifuges, Reflow Ovens, Advanced Reliability Testers
4) IC Testing: IC Testers & Handlers, Harddockings, Interfaces, Manipulators, Automated Wafer Probe Stations
5) Photolithography: Mask Aligners, Photoresists, Maskless Exposure Systems, Spin Coaters & Hotplates
6) Metrology: AFM, Thin Film/Wafer Stress and Thickness Measurement Systems, Optical Profilers, Nanoindentors, Thermal Warpage and Strain Measurement Systems, AOI Machines
7) Deposition & Etching: Plasma Deposition & Etching Systems, ALD Systems, Sputtering & Evaporation Systems
8) Others: Solar Simulators, Nanoimprint Stamps, In-situ Aligned Wafer Bonders, Solderability Testers

SEMICAPS Pte Ltd. Booth No: B06-B07

SEMICAPS is a developer and manufacturer of world-leading fault localization and defect characterization equipment for the semiconductor industry. We provide solutions and services for design debug, product engineering, yield enhancement and customer returns. With the semiconductor technology node progressing towards 22nm and 14nm, more demand is anticipated for our leading edge machine to help customers analyze their advance node products.
Our products include:
a. Laser Timing Probe (LTP) - An instrument which allows the waveform at a particular node inside a semiconductor device or IC to be measured using a laser as a probe;
b. Scanning Optical Microscope (SOM) System - A multi-laser scanning optical microscope system for the active localization of integrated circuit defects using static power alteration and dynamic tester-based techniques;
c. Photon Emission Microscope (PEM) System - A highly sensitive passive fault localization system for the localization of integrated circuit defects using panchromatic imaging and spectroscopy.

ELLIPSIZ DSS PTE LTD Booth No: B08, B27, B37, B38

Building 2, Room 1406, No. 289, ZheQiao Road, Shanghai, China
Website: http://www.ellipsiz.com/

Ellipsiz is pleased to be collaborating with both our principals Allied High Tech Products, Inc, SELA & DIGIT CONCEPT to showcase their products during this IPFA 2019.
Allied High Tech Products, Inc, a US-based manufacturer with a specialized product offering of precision grinding and polishing equipment in support of electrical and physical failure analysis of electronic devices. As the leader in this field, Allied offers a complete solution for sample preparation of electronic components from sectioning, mounting, milling/grinding and polishing to measurement. Allied will

its Precision Milling/Polishing System (X-PREP®), Polishing System (MULTIPREPTM) & Substrate Measurement Instrument (X-PREP® VISIONTM).

SELA is a leading innovator in advanced solutions for the sample preparation for physical failure analysis and characterization in the semiconductor industry. Over the past 25 years, SELA has been developing technologies and offering solutions that help our customers create the best of the kind electronic devices that have become an integral part of everyday life for each of us. SELA will have a live demo for its latest Smart IR Micro Cleaving Solution MC20

DIGIT CONCEPT (DC) was founded in 1992 and is one of the leading suppliers of commercial IC Decapsulation, Cross Sectioning, Bonding and PCB Cut.

We design and manufacture state of the art equipment and this year we will show the newest ones

For SELA equipment:

China: Mr. Jacky Zhang - zhang.jacky@ellipsiz-cn.com

SEA: Mr. LeeChoon Liang - lee.cl@ellipsiz.com

For ALLIED equipment:

China: Mr. ChaoLiu –liu.chao@ellipsiz-cn.com

SEA: Ms. Susan Lim - lim.susan@ellipsiz.com

For DC equipment:

China: Mr ChaoLiu –liu.chao@ellipsiz-cn.com

SEA: Mr LeeChoon Liang - lee.cl@ellipsiz.com

Badge Sponsorship Introduction: DC Booth 37-38

DIGIT CONCEPT (DC) was founded in 1992 and is one of the leading suppliers of commercial IC Decapsulation, Cross Sectioning, Bonding and PCB Cut.

We design and manufacture state of the art equipment and this year we will show the newest ones:

- SesamePLASMA: new iCE_MIP™ XL release

We will be happy to present you on our booth the last release of:

- SesameLASER
- SesameACID
- SesameMECHANICAL

UP-GRADE or TRADE-IN your old equipment with iPanel™

Have a fruitful IPFA 2019 with DC and ELLIPSIZ Teams

Company Name:	DIGIT CONCEPT SAS
Address:	SECQUEVILLE EN BESSIN – FRANCE
Website:	www.digit-concept.com
Contact Person:	Michael OBEIN
Phone:	+33 231 354 354
Email:	m.obein@digit-concept.com

Exhibitors' Information

Gold Medal Analytical & Testing Group — Booth No：B09

No. 2 Xiangshan Avenue
Zengcheng District, Guangzhou
Tel: +020 32199187
Fax: +020 26225379
Website: www.gmatg.com
Contact: Yu hui Luo --Sales Director; Sheng wei Zhou--Sales Director
Email: sales@gmatg.com
Wechat Public Number: ledqalab

Gold Medal Analytical & Testing Group is a new type of scientific research and testing institution, which is founded by Dr. Fang Fang, an expert of the National "Thousand People Program" and focuses on failure analysis of the third generation semiconductor GaN and SiC chips and devices. Gold Medal Analytical & Testing Group has set up instrument research and development centers in China and Britain. The main equipments independently developed include Microscopic Light Distribution Testing System, Microscopic Thermal Distribution Testing System and Laser Opening System. The product has been widely used by scientific research institutes and listed companies in universities, and widely praised by teachers and researchers. Excellent performance, trustworthy.

Platform Design Automation, Inc. — Booth No: B10

Platform Design Automation, Inc.（PDA） provides EDA tools and a comprehensive set of services to facilitate designs using highly scaled technologies. Our years of experiences in device modeling, PDK and cell library as well as our unique EDA platform technology enable us to ensure accurate and robust design inputs including device models, PDK and cell libraries. Our EDA tools in device modeling, PDK and device characterization solutions are based on the latest technology and grow rapidly in recent years. PDA HQ is in Beijing, and has branch offices in Shanghai and Taiwan Hsinchu.

JIACO Instruments — Booth No: B11

Feldmannweg 17
2628 CT, Delft
The Netherlands
Tel: (31) 62526 1648
Fax: (31) 15 -278 7369
Website: www.jiaco-instruments.com
Contact: Mr. Mark McKinnon – Sales Director
Email: mark@jiaco-instruments.com

JIACO Instruments Microwave-Induced-Plasma (MIP) decapsulation system is a breakthrough innovation: Automated atmospheric pressure MIP decapsulation utilizing O2-only recipes. The system has been proven

for Cu, PdCu, Au, Ag bond wires and for advanced package types like 3D, SiP, WLCSP, High Tg, Chip on Board, BOAC; all without process induced damage for reliable failure analysis and quality control.

The JIACO Instruments MIP system has been in the market since mid-2016 and is now in use by many renown global companies for reliable failure analysis and quality control. We look forward to discussing your decapsulation challenges & requirements at IPFA 2019!

Hongzhunda Tech — Booth No: B12

CHANG ZHOU: Building 1C,Jintong Industrial Park,No.8 Xihu Road, Wujin National High Tech Industrial Development Zone
Tel: 0519-86228809
SHANG HAI: RoomC-D,2nd Floor, Building 3#,133 Curie Road,433Guoshoujing Road, Pudong New Area, Shanghai
Tel: 021-50905218
XIA MEN: Room 101'No34 GuanRi, Software Park Phase II, Siming District.
Tel: 0592-5936290

Founded in 2014, specializing in the semiconductor industry chain customers to provide inspection and testing services, failure analysis consulting, science and technology consulting and other related technical services, committed to providing customers with efficient, fast and accurate problem solutions.
The company's service strongholds are located in Shanghai, Xiamen, Changzhou, with industry professional and technical personnel team, with strong technical and resource integration ability.
The product service object covers the university, the research institute, the semiconductor industry upstream and downstream.
Under the trend of industry differentiation becoming more and more mature, the company is the first comprehensive platform for virtual IDM, to integrate industrial resources and provide value services.
Quality policy: to provide customers with satisfactory service.
Management policy: imaginative, creative, executive, binding.

MA-tek — Booth No: B13

MA-tek is an independent lab with ISO-9001 and IECQ 17025 international accreditations, and filed for an IPO in August 2009. Shortly, in 2016,it is also certified by ISO-27001 on information security.

Materials Analysis (MA-eek) is world-class laboratory providing service in material analysis (MA). In line with the growth of the business's development, Ma-tek has successfully expanded to be equipped with additional Failure Analysis (FA), Reliability testing (RT), and Surface Analysis (SA) and Chemical Analysis (CA) services.

These integrations allow MA-Tek to provide superior service for its clients in various industries.

Exhibitors' Information

ZEISS — Booth No: B14

No. 60, Meiyue Road, Pudong new district, Shanghai, China
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Fax: +86-21-5048-1193
Website: www.ZEISS.com/PCS
Contact: Sales Support Specialist
Email: spring.wang@zeiss.com

ZEISS has the most comprehensive portfolio of light, x-ray, electron beam and ion beam imaging technologies in the industry and is a leading solution provider to the global semiconductor community. Solutions span semiconductor manufacturing from wafer fab through packaging and assembly. For mask making and lithography, ZEISS provides unique solutions in the areas of zero defect, in-die metrology, critical dimension/registration and overlay control. ZEISS innovative process control and failure analysis solutions deliver actionable information to both wafer fab and packaging/assembly processes to meet the semiconductor industry's challenges for next-generation devices.

ZEISS is represented in over 40 countries around the globe with more than 40 manufacturing sites, around 50 sales and service locations, and over 20 research and development centers. Founded in 1846 in Jena, the company now has its headquarters in Oberkochen in southwest Germany. Carl Zeiss AG is wholly owned by the Carl Zeiss Stiftung (Carl Zeiss Foundation).

AMETEK TMC and EDAX — Booth No: B15

Part A1, A4, 2nd Floor Building No.1, No.526 Fute 3rd Road East, Pilot Free Trade Zone (Shanghai), China.
Tel: +86 21 58685111
Fax: +86 21 58660969
Website: www.techmfg.com
www.edax.com.cn

TMC designs and manufactures advanced building floor vibration isolation systems for nanotechnology. TMC isolators support ultra precision measurements, instruments, and manufacturing. TMC products enable ultra-precision research, measurements, and manufacturing in the fields of photonics, semiconductor manufacturing, life sciences, drug discovery, and nanotechnology.

EDAX is a leading provider of innovative materials characterization systems, which are essential and commonly used for failure analysis. EDAX products include stand alone tools, integrated tools for EDS-EBSD, EDS-WDS, and EDS-EBSD-WDS, and a free-standing Micro-XRF bench-top elemental analyzer providing small and micro-spot X-ray analysis and mapping.

Exhibitors' Information

TOYO CORPORATION CHINA — Booth No: B16

ROOM 310, #228 Meiyuan Road, Jing'An District, Shanghai, China.
Tel: +86-21-63809633
Website: www.toyochina.com.cn
Contact: Jerhyn Chen
Email: chencongyu@toyochina.com.cn

Magnetic Fault Isolation for static failure. TOYO introduces a new use of a scanning super conducting quantum interference device SQUID microscope to image magnetic fields generated by currents in an integrated circuit at room temperature. SQUIDs are the most sensitive magnetic sensor known and they can be designed to measure fields as small as 1fT, which is 40 billion times smaller than the Earth's magnetic field. With the strong penetration of magnetic field and the high sensitivity of the detector, SQUID became a new method to be used in various applications.

GALLANT PRECISION MACHINING CO., LTD. — Booth No: B17

No.5-1 Innovation 1'st Rd., Science Based Industrial Park, Hsinchu, 30076 Taiwan
TEL: +886-3-563-9999
Website: www.gpmcorp.com.tw
Email: andrewchen@gpmcorp.com.tw
Contact Person: Andrew Chen

The headquarter of GMP group is located at Hsinchu Science Park, with additional research facilities and manufacturing centers located in Central Taiwan Science Park. Taichung Industrial Park, and Suzhou, China.

GPM provides services throughout Taiwan, China, and South-East Asia with a 24 hour full after-sales service and support to assist customers solving any production related issues.
GPM devotes to develop leading technologies for making equipment with new process, especially integrates IBM's Picosecond Imaging Circuit Analysis (PICA) on advanced IC Characterization and Failure Analysis, which has made GPM fully grasp technical advantages and market opportunities.

Giga Force Electronics Co.,Ltd — Booth No: B18

GIGA FORCE ELECTRONICS CO.,LTD, was founded in 2008 and had kept moving forward to integration services for semiconductor back-end field. We provide one stop turnkey solution from PCB Design/Fabrication/SMT, Reliability Qualification, Failure-Analysis, Material-Analysis, Assembly& Testing and Equipment& Component sales. GIGA FORCE had achieved the high-tech enterprise and the specialized new-tech enterprises certification, also we had obtained ISO9001 and CNAS certification, Giga Force had established close relationship with many Enterprises, University and Research Institutes. Our service has been widely recognized by many Tier-1 world-wide customers. GIFA FORCE IPOed in Y2016, the stock code is 870641.

Exhibitors' Information

Thermo Fisher Scientific — Booth No: B19, B24

1 Jalan Kilang Timor
#04-02 Pacific Tech Centre
Singapore 159303
Tel: +65 6272 0050
Fax: +65 6272 0034
Website: www.thermofisher.com/EM-sales
Contact: Paige Tan, Event Manager
Email: paige.tan@thermofisher.com

Thermo Fisher Scientific supplies innovative solutions for electron microscopy and microanalysis. We provide SEMs, TEMs and DualBeam™ FIB/SEMs combined with electrical test solutions and advanced software suites to take customers from electrical localization to physical root cause. Our industry-leading workflows deliver fast, accurate answers for accelerating IC design and production decisions. Our fault isolation and analysis products provide superior images, rich feature sets, cross-sectional metrology and automation to speed process defect identification, enable root-cause analysis, reduce yield loss and accelerate time-to market for new products. Our experts engage with applications, engineering, and manufacturing teams to address today's challenges, while our leadership and significant R&D commitment are paving the way to sub-7–nanometer technologies and beyond.

WinTech Nano — Booth No: B20

WinTech Nano is a leading 24 hour running service laboratory providing one-stop analytical services. Our professional services cover Structure Analysis, Material Characterization and Electrical Failure Analysis. WinTech Nano has world-class analytical instruments including: 3D X-Ray, OBIRCH, EMMI, FIB, TEM, TOF-SIMS, D-SIMS, XPS, etc. Our fast and reliable analysis result gives the best support to R&D and production customers.

RADIANT OPTRONICS PTE LTD — Booth No: B21

621 Aljunied Road
#03-03 Lipo Building
Singapore 389834
Tel: (65) 6288 5252
Fax: (65) 6858 5822
Website: www.radiantoptronics.com
Contact: Mr Christopher Cheong, Director
Email: chris@radiantoptronics.com

Radiant Optronics Pte Ltd specializes in sample Preparations equipment for Failure Analysis applications. Our equipment consists of: Radiant Laser Decapsulators, Ultratec Mechanical Decapsulators, Muegge Plasma Decapsulators. Infrared Microscopes. Please visit our website - www.radiantoptronics.com

Exhibitors' Information

Hitachi Power Solutions Co., Ltd — Booth No: B22

Hitachi Power Solutions develops and provides our original Scanning Acoustic Tomographs and their transducers used for non-destructive testing of semiconductor and electronic devices. We have very abundant experiences in this field for more than 30 years.
We have very wide products' lineup consisting of FineSAT series, FSLine series, WaferLine and ES-5100. The FineSAT series can be utilized to inspect wide variety of electronic devices and materials not only in laboratories but also in mass-production lines. FSLine series are optimum for large scale mechanical parts and materials such as sputtering targets. The WaferLine is an automated system for bonded Si wafers, MEMS wafers and other applications. ES-5100 can realize extremely high-speed testing on combination with phased array transducers. These tools achieves many kinds of inspection in conjunction with wide variety of optional parts and software.
We can also offer appropriate transducers selected from the wide variety of lineup or customize transducers to customers' samples.
Please feel free to consult us.

Hitachi High-Technologies Corporation — Booth No: B23

Room 1405,Beijing Fortune Bldg.No.5Dong San Huan Bei-Lu, Chao Yang District, Beijing 100004,P.R.C.
Tel:(86)10-6590-8705 Fax:(86)10-6590-8710
Homepage:www.hitachi-hightech.com
Contact: jinrong.liu
Mail: jinrong.liu.ue@hitachi-hightech.com

Hitachi High-Technologies Corporation aims to be a successful enterprise trusted by all our stakeholders and contributing to social progress through business activities that emphasize value creation through high-tech solutions. We are committed to open, transparent, and reliable business practices. As we continue to grow, we will value environmental responsibility and strive to build a prosperous community, contributing as a corporate citizen with passion and pride in our work.
Business Policy：
To place the customer first, growing with our customers by providing the best solutions, consistently a step ahead of market needs.
To contribute to value creation in the global community through synergies between our strengths in cutting-edge technologies and our capabilities as an established trading company.
To aim for reliability and excellence based on our core assets of talent and technical resources, and to maximize our corporate value.

Semishare (Shenzhen) technology CO., LTD — Booth No: B25

Semishare Instruments Shenzhen Office
Web site：www.semishare.com
Leo Mobile：+86-18124555912

Exhibitors' Information

SEMISHARE committed to the sharing business of advanced semicon technology, focusing on promoting China's fast growth in the semiconductor industry. Our target is be a leading total solution partner to our clients. Currently, we have our semiconductor equipment agent business group and semicon equipment manufacturing plant which makes probe station and laser repairing machine in Shenzhen, China.
SEMISHARE equipment agent business group provide the world famous semiconductor testing equipment and processing equipment. Testing equipment including probe station, laser repair system, IV / CV tracer and source meter
SEMISHARE's products and solutions have been successfully used in most IC/LED/LCD foundries and R&D centers in China.

ESDEMC Technology LLC — Booth No: B26

4000 Enterprise Drive, Suite 103, Rolla, MO, 65409, USA
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Fax: +1 877-641-9358
Website: www.esdemc.com
E-mail: info@esdemc.com; rachel@esdemc.com

ESDEMC Technology develops, manufactures, and markets ESD and EMC related products. We are devoted to delivering creative, flexible, and cost effective ESD and EMC solutions and top-level consulting services. We also offer customized design services to satisfy all of our customers' needs.

We provide:

- Pulsed IV-Curve Solutions;
- Probe Station Solutions System Level ESD Solutions
- cable discharge solutions;
- EMC&RF solutions and Hight voltage measurement
- High voltage supply system

ESDEMC Technology LLC offers top specification Transmission Line Pulse (TLP) Solutions. Our design team has over 20-years' experience with tough high voltage and high frequency designs. ESDEMC has been providing great System Level ESD Consulting for the industry. We offer ESD failure analysis, test solutions and ESD design consulting. We have been the OEM for other ESD/EMC companies.

KLEINDIEK NANOTECHNIK — Booth No: B28

Aspenhaustr. 25
72770 Reutlingen
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Tel: +49 7121 345 395 0
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Website: www.kleindiek.com
Contact: info@kleindiek.com

Kleindiek Nanotechnik is a customer oriented, innovative high-tech company specialized on manufacturing micro- and nano-positioning systems for a wide range of applications - including electrical fault isolation at the nano-scale.
Our customer-driven approach is focused on providing complete and innovative solutions for each of our market segments: researchers, industrial customers and enterprises.
Our product development philosophy is the direct solution of the specific underlying problem. The simplicity, homogeneity and harmony of our designs guarantee maximum manoeuvrability and highest resolution while maintaining the smallest outer dimensions.

Shanghai Winner International Trading CO., LTD **Booth No: B29**

RM708, Building 2, NO. 268,
Taihong Road, Hongqiao CBD,
Shanghai, China
Tel: 021-31037266 Fax: 021-64200918
Website: www.ghitcsh.com
Contact: Mr. Heng
Email: michael@ghitcsh.com

As a professional supplier of nanotechnology solutions, Shanghai Winner International Trading Co., Ltd. is committed to the sales and production of semiconductor equipment, laboratory physical and chemical analysis equipment, electron microscopy and supporting equipment. At present, it is the agent of Lattice Gear Precision Fixed-point Slicing System, IBSS plasma cleaning system, Tousimis critical point dryer, Swiss IMINA nanomanipulator in China. The sales and after-sales service of the district, as well as the solution of localized in-situ electron microscopy and sample preparation equipment, meet the application needs of scientific research and industrial users.

Zurich Instruments **Booth No: B30**

Room 2015-2016, Block A, Gateway International Plaza,
No.325 Tianyaoqiao Road., Xuhui District, Shanghai 200030, China.
Tel: +86 21-64870285/87
Website: www.zhinst.cn
E-mail: info.cn@zhinst.com
Contact person at the exhibition: Dr. Luo Lu, luo.lu@zhinst.com
Social media channels:
https://twitter.com/Zhinst
https://www.linkedin.com/company/zurich-instruments-ag

https://www.youtube.com/zhinst

Zurich Instruments is a technology leader developing and selling advanced test & measurement instruments for dynamic signal analysis. These devices are used in many fields of application by high-technology research laboratories and industrial development sites.

Zurich Instruments' vision is to revolutionize instrumentation in the high-frequency (HF) and ultra-high-frequency (UHF) range by incorporating the latest analog and digital technology into powerful measurement systems for unprecedented functionality. Best-in-class performance, differentiating features, new measurement solutions, and premium customer support complete the unique offering.

The product philosophy is derived from observing the complexity of many laboratory setups: devices are stacked upon each other and numerous interconnects introduce an unnecessary potential for errors. We help users to reduce the complexity of their setups by combining the required functions into fewer boxes. Further we use our application know-how to help customers to choose the right instrument, to quickly get started and obtain first results.

HANWA ELECTRONIC IND. CO., LTD. Booth No: B31

689-3 OGAITO, WAKAYAMA, JAPAN, 649-6272
TEL：+81-73-477-4435
FAX：+81-73-477-3445
Website：http://www.hanwa-ei.co.jp/
Contact：Mr. Keiichi Hasegawa
Email：info@hanwa-ei.co.jp

We are the worldwide ESD/CDM/TLP tester maker in providing customers with good quality and service of ESD testers over 30 years throughout the world. We have acquired the largest market share of ESD industry in Japan and have developed various new ESD testers over many years. Also, we are one of committee member of EOS/ESD Association, Inc.
Here is our products: - High pin count automatic ESD tester, HED-G5000 / HED-N5000 - Full Automatic ESD tester, HED-S5000R - CDM Tester, HED-C5000R - Wafer Level HBM tester, HED-W5300D – TLP Tester, HED-T5000 HED-G5000 is an automatic ESD tester with ultra low parasitic capacitance and allows you to have ESD test with Max.2048 pins. Perfectly it corresponds with the worldwide standards: ESDA, JEDEC, AEC and JEITA.
If you are interested in these products and other ESD Testers, please contact us anytime. E-mail: info@hanwa-ei.co.jp TEL: +81-73-477-4435 FAX: +81-73-477-3445

Hamamatsu Photonics Booth No: B32

Hamamatsu has been working with the Photon for more than 60 years since 1953. Our products applied widely in medical biology, HEP, universal detection technology, rigorous analysis etc. We have established ourselves as the top company of photoelectron conversion technologies in the world. Members of Hamamatsu

consider ourselves a research and development company, and we believe that the only way to achieve sustainable growth is to maintain our technological advantages. It is our job and passion to advance photonic technologies. In order to make more contribution to Chinese photonics industries, Hamamatsu Photonics (China) Co., Ltd. was established in Oct 2011 and to be responsible for sales, marketing, technology support and after-sales service in China.
What's more, we realize that pursuing the knowledge of photonics technologies alone, by ourselves, is like reaching for the stars with a ladder. Thus we will work together with colleagues around the world, who share our passion and the belief that understanding photonic technologies will lead to broader applications and also generate new industries for the advancement of humankind.

Integrated Service Technology — Booth No: B33

2,Bldg., No.455 Jinfeng Road, Pudong New Area,
Shanghai, China 201201
Tel:800-988-0501
Website:www.istgroup.com
E-mail: marketing_cn@istgroup.com

Founded in 2002 in China, iST began its business from IC circuit debugging and modification and gradually expanded its scope of operations. In 2016, iST established a fully integrated circuit supply chain verification and analysis engineering service platform in Shanghai to provide comprehensive services for failure analysis, reliability verification、wafer microstructure material analysis、board level reliability test and wafer grinding so on.
iST's customers cover the whole spectrum of the electronics industry from IC design, wafer manufacturing, IC packaging and testing to end products. In response to rising Cloud Intelligence (AI), Internet of Things (IoT) and Internet of Vehicles (IoV), iST not only focuses on core services but also establishes an unique and integrated automotive chip (Single Chip/Multi Chip/System-in-Package)、Board Level Reliability Test and Failure Analysis verification platform in mainland China to face the diversified national and international growing trend.

Phenom Desktop SEM — Booth No: B34

Room 501-503, Tower E, German Centre, No.88 Keyuan Road, Pudong, Shanghai
Tel: 400 857 8882
Fax: 021-28986858
Web: www.phenom-china.com
Email: info@phenom-china.com
Contact person: Di Zha, Marketing Manager

Phenom-World is a global leading supplier of Desktop Scanning Electronic Microscopes, and the company focuses on imaging solutions for submicron scale and nanoscale applications. Our SEM-based systems are

used in a wide range of markets and applications, such as material science, electronics, nano-particle, biomedical sciences, textile fiber and geological sciences, etc.
Phenom Scientific Instrument (Shanghai) Co., Ltd., the Chinese exclusive agency of Phenom-World is responsible for marketing and sales of Phenom Desktop SEM in China to provide the professional technical support and testing services.
Phenom Scientific Instrument (Shanghai) Co., Ltd. has a high-qualified application supporting team, it has built test center and service center in Shanghai, Beijing, Guangzhou and Chengdu. Nowadays the users of Phenom Desktop SEM in China are more than 1000.

Oxford Instruments — Booth No: B35

Shanghai, China
Tel: 400-678-0609
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Oxford Instruments plc is a leading provider of high technology products, systems and tools to the world's leading industrial companies and scientific research communities.
We use innovation to turn smart science into world-class products that support research and industry to address the great challenges of the 21st Century.
We are proud to be recognised as the leaders in what we do and for the difference we make in the world.

Imina Technologies SA — Booth No: B36

Tel: +31 630666760
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Contact: Mr. Rob Claassen
Email: claassen@imina.ch

Imina Technologies' Nanoprobing Turnkey Solutions have up to 8 nanoprobers based on a unique accurate and stable motion technology to position probe tips with precision and establish steady contacts with the device under test. Various configurations and solutions are offered to adapt with your specific SEM-FIB or Optical Microscope equipment and FA test routines. The Nanoprobing module of Precisio™ software suite provides a step by step assistance to guide the operator from setting up measurement campaigns, to landing probes and acquire data, ensuring a smooth and intuitive workflow." to get to quantitative data easy and fast.

Suzhou Nordson Electronics Equipment Co., Ltd — Booth No: B39

Building 7, No.666, Jianlin Rd,
Suzhou, China 215129
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Fax: +86 512 6665 3218

Exhibitors' Information

Website: www.nordson.com
Contact: Mr. Cotton Yang (Sales Manager)
Email: Cotton.Yang@nordson.com

Nordson Advanced Technology Electronics Systems is the industry leader in several fields of Semiconductor and Electronics assembly. Through our group of leading edge technology companies ASYMTEK Precision Dispensing, DAGE Bond Test and Materials Testing, DAGE MXI Stand Alone X-Ray, DIMA Hot Bar Soldering, MARCH Plasma Cleaning, MATRIX AXI In-line X-Ray, SELECT Selective Soldering, SONOSCAN Acoustic Micro Imaging and YESTECH AOI Inspection, we deliver standard and customized solutions to customers worldwide for the most challenging Manufacturing and Test & Inspection Issues.
Nordson is involved in all of the leading edge manufacturing challenges in today's complicated electronics and semiconductor supply chain. From component manufacturing to MEMS and module assembly, through board assembly, test, inspection, failure analysis and final assembly, Nordson works with our customers to optimize the process through process and application expertise. Delivering complete solutions to the issues and problems of our customers through hardware, software and first class customer support. For more information, please visit www.nordson.com.

Crest Systems (Suzhou) Co., Ltd **Booth No: B40**

03-04, 3F, B Building, Ascendas-Xinsu
Industrial Square, No.5 Xinghan Street, Suzhou, Jiangsu, China
Tel: (86)512-6741 2701
Fax: (86)512-6741 0973
Website: www.crest-systems.com
Contact: Mr.Brad-Business Manager
Email: Brad.liu@crest-group.net

Crest Systems (Suzhou) Co.,Ltd, Crest is committed to the world famous brand of high-tech testing equipment and related products to the majority of customers in China and South of Asia.
We are located in China, Malaysia, Thailand, Singapore and other regions, for customer to provide first-class detection equipment and solutions, industries covering semiconductors, aerospace, universities, automotive electronics, research institutions and other fields.
Our equipment includes: Imina-Nanoprobe, Nordson Dage Bond-tester, Nordson Dage X-ray Inspection System, Nordson MatriX, Nordson MARCH, Nordson Yestech, Nordson Sonoscan C-SAM Tester, Olympus microscope, NSC-decap system, etc.
We uphold the principle of first-class products, service first. Believe us, choose us, will bring you more surprises!

Keynote speakers

Prasad Chaparala
Amazon Lab126, USA

Prasad Chaparala is the Director of Reliability Engineering at Amazon Lab126 in Sunnyvale, California. He is responsible for reliability engineering of a broad range of consumer electronic devices such as Echo smart speakers, Kindle e-readers, Fire tablets, and Fire TV products. Prior to this, he was the Vice President of Product and Reliability Engineering at Alta Devices from 2010 to 2014. Before joining Alta Devices, he was with National Semiconductor for 14 years in various process and reliability engineering roles. He received a Ph.D in Reliability Engineering from the University of Maryland, College Park. He has contributed to more than 50 publications in international journals and conference proceedings and holds 18 US patents. He is a recipient of three Best Paper awards at IEEE International Reliability Physics Symposium (IRPS). Additionally, he was served as the General Chair for the 2014 IRPS and was a member of the Board of Directors for IRPS.

Building Reliable Products Guided by Customer Obsession

With the rapid proliferation of consumer IoT devices that are embedded into everyday life, building both affordable and reliable hardware that continues to meet the highest customer expectations is of paramount importance. This is particularly challenging for new applications where customer-use conditions can vary broadly and can be unpredictable. Unlike other established industries such as semiconductor, automotive or aerospace where widely accepted reliability standards exists, there are no industry reliability standards for consumer electronics devices. In-depth understanding of customer usage environments, patterns, and expectations is critical in deriving appropriate system-level reliability specifications and test methods in order to build reliable devices that surpass customer expectations. This talk will provide an overview of how system-level reliability requirements for devices such as the Amazon Echo and Fire TV products are defined by working backwards from customer needs. The talk will cover various advanced engineering approaches in defining reliability specifications and test methods through user surveys, statistical analysis and machine learning techniques and customer feedback.

Keynote speakers

Shimeng Yu
Georgia Institute of Technology, USA

Shimeng Yu is an associate professor of electrical and computer engineering at the Georgia Institute of Technology in Atlanta, Georgia. He received the B.S. degree in microelectronics from Peking University, Beijing, China in 2009, and the M.S. degree and Ph.D. degree in electrical engineering from Stanford University, Stanford, California, in 2011 and in 2013, respectively. From 2013 to 2018, he was an assistant professor of electrical and computer engineering at Arizona State University, Tempe, Arizona.

Emerging Non-Volatile Memory's Applications in Neuro-Inspired Computing and Hardware Security

Emerging non-volatile memory (eNVMs) technologies have made significant advances in the past decade as storage class memory and embedded memory with extensive industrial research and development. This presentation will survey the recent progresses of using eNVMs for new applications beyond data storage in the era of artificial intelligence (AI) and Internet of Things (IoT), in particular for 1) neuro-inspired computing and 2) hardware security. Firstly, I will introduce the individual components of the deep neural network hardware – the eNVM based synaptic devices and neuronal devices. Secondly, I will discuss the crossbar array architecture that embeds the computation into memory array, namely compute-in-memory approach, and show the array-level and chip-level demonstration results. Then, I will introduce the "NeuroSim" framework, a device-circuit-algorithm co-design simulator that benchmarks the non-ideal effects of eNVMs on the machine learning accelerator performance. Lastly, I will introduce how to leverage the eNVM's variability as physical unclonable function (PUF), a hardware security primitive for device authentication and cryptographic key generation. Through the presentation, the potential reliability issues and failure mechanisms of these new applications will be discussed.

Tutorials speakers

Dimitris P. Ioannou
GlobalFoundries, Hopewell Junction, NY 12533, USA

Dimitris Ioannou is a Senior Member of Technical Staff at GlobalFoundries. He received his B.S degree in Physics from the University of Thessaloniki, Greece, and the M.S. and Ph.D. degrees in Electrical Engineering from George Mason University, Fairfax, VA. In 2006, he joined IBM where he played a critical role in the characterization and modeling of reliability mechanisms in advanced Silicon On Insulator (SOI) High-k/Metal Gate CMOS technologies including IBM's 3D TSV technology. As of 2015 he is with GlobalFoundries where he leads the RF reliability of advanced SOI CMOS and SiGe BiCMOS devices. He has published over 40 papers in the field of CMOS reliability.

Reliability of 3D Through-Silicon-Via (TSV) Technologies

3D integration has emerged as viable solution for meeting the growing demands and requirements of advanced CMOS systems such as higher performance, increased functionality, lower power consumption, all, at a smaller footprint. This tutorial will provide an overview of the key features of 3D TSV technologies and the challenges associated with them. It will discuss the impact of 3D TSV integration on FEOL, BEOL and package reliability highlighting the unique aspects of the TSV structure such as differential thermal expansion mismatch and the high aspect ratio structure. It will also discuss potential processing related reliability issues such as contamination effects, wafer thinning, dicing and packaging. Finally, it will provide with an overview of available mitigation strategies for these reliability challenges.

Tutorials speakers

David Su
Taiwan Semiconductor Manufacturing Company, Inc., Taiwan (Retired)

David Su was Director of the Failure Analysis Division of TSMC in charge of reliability-related failure analysis, materials and surface analysis including TEM, and chemical analysis from 2000 until 2018. Prior to joining TSMC, he was Director of TEM and FIB Technology Development at Accurel Systems in Sunnyvale, California (1998-2000). From 1991 to 1998 he was TEM Specialist at the Materials Analysis Group of Philips Semiconductors in Sunnyvale, California. He was an adjunct professor at the Department of Materials Engineering at San Jose State University in San Jose, California from 1989 to 1991. David Su received his B.S. degree in Chemical Engineering from the University of Sao Paulo, Brazil and his M.S. and Ph. D. degrees in Chemical Engineering from Stanford University. He has been a board member of the Taiwan Microscopy Society since 2004. He was a board member of the Electronic Device and Failure Analysis Society of the U. S. (2014-2016) and Chair of the Sematech Integrated-Circuit Failure Analysis Council (2013). He was chairman of the 2010 IRPS Failure Analysis Technical Program and was International Chair for ISTFA 2010, 2011 and International Co-Chair in 2013.

Principles and Applications of TEM and FIB in the Semiconductor Industry

The demands of failure and materials analysis for advanced technology nodes of the integrated circuit industry have pushed Transmission Electron Microscopy (TEM) and Focused Ion Beam (FIB) systems to their limits, especially the need to obtain 3D information both visually and compositionally in the nanometer size range. In this tutorial, the principles and applications of these techniques will be discussed. In addition to conventional imaging and elemental analysis, techniques such as strain measurement, tomography will be presented. The important area of sample preparation will be addressed as well as efforts to automate both data acquisition and sample preparation. Finally, advances in FIB circuit editing will also be discussed.

Tutorials speakers

Jianfu Zhang
Liverpool John Moores University, UK

Jianfu Zhang received B.Eng. degree in electrical engineering from Xi'an Jiao Tong University in 1982 and Ph.D. degree from University of Liverpool in 1987. He joined Liverpool John Moores University (LJMU) as a Senior Lecturer in 1992, became a Reader in 1996, and a Professor in 2001.

Dr. Zhang has worked on the qualification of devices and processes for over 30 years, specializing in defects, ageing, modeling, and lifetime prediction of CMOS technologies. He is the author or coauthor of over 200 journal/conference papers, including 55 papers in IEEE Transactions and Electron Device Letters, 19 papers at IEDM/Symposium of VLSI Technology, and 35 invited papers/book chapters. He is/was a member of the technical program committee of several international conferences, including IEDM. His research has been supported by IMEC, ARM, Synopsys, Qualcomm, and the Engineering and Physical Sciences Research Council of UK.

BTI: Testing and Predictive Modelling

Bias temperature instabilities (BTI) of MOSFETs are well known ageing processes and their qualification is essential for CMOS technologies. To modelling BTI and qualify device lifetime, the common practice is to extract BTI model based on accelerated ageing tests. Several models were proposed by early works and their ability to fit the test data is often demonstrated. This tutorial will show that some models cannot accurately predict the BTI under use-conditions, where ageing is slow. The As-grown-Generation (AG) model is introduced and its predictive capability is demonstrated. The key for the success of AG model is an accurate separation of defects into as-grown defects and generated defects. After presenting a defect framework and the evidences for it, this tutorial will describe the detailed techniques for the defect separation and a step-by-step guide for their implementation. It will be shown that different defects have different ageing kinetics and how the correct time exponent can be extracted independent of test conditions. AC modelling and defect discharging also will be addressed. The connection and difference between AG model and the JEDEC procedure will be clarified.

Tutorials speakers

Lihong Cao
ASE Group, Austin, TX, USA

Lihong Cao is a Director in ASE Group responsible for new packaging technology development (2.5D/3D, FOWLP, FOCoS, PoP, SIP, SESUB), technology promotion, new product introduction, technical program management, strategic planning, and business engagement. Her focusing spans from design, process qualification, root cause analysis and production enablement in HPC (High Performance Computing), AI/MI (Artificial & Machine Intelligence) and 5G/mmWave.

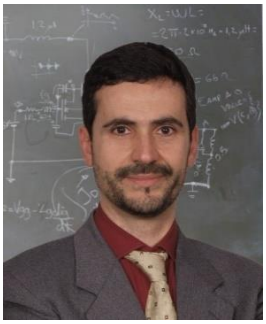
Prior to joining ASE, as a Sr. Manager in AMD, she led global package analysis operations to support product development, qualification, production and customer issues for 28/16/14/7nm technology. She was also in charge of failure analysis technique development and roadmap for advanced package analysis. She not only has semiconductor industries experience, but also had academic and professional experience in National Research Institute and Universities.

Lihong received her Doctoral degree in Material Science & Engineering in Wuhan University of Technology and Research Associate Professor in Nanyang Technology University in Singapore. She has published more than 80 technical papers and held several US patents. She has been a Technical Chair and Tutor in ISTFA since 2011. She was invited as panel member in ISTFA 2018.

Advanced 2.5D/3D Package Level Failure Analysis

IC packages are becoming increasingly complex due to the large body size, small form factor and application of integrated packages such as MCM (multi-chip modules), POP (package on package), FOWLP (fanout wafer level package), Chiplets MCP (multi chip package), SIP (system in package) and 2.5D & 3D stacked die package. Package level failure analysis has become very challenging. Efficiently detecting and localizing the failure in order to drive root cause has become very critical. This tutorial will provide a brief overview of the package level failure analysis techniques including electrical verification and advanced fault isolation for 2.5D/3D stacked packages. Given an “alphabet soup” of isolation techniques available, the choice of the optimal technique for a particular fail can be very challenging. The tutorial will also focus on how to make a decision on which techniques are best suited for the defect types commonly occurred in package level, followed by FA examples.

Tutorials speakers



Francesco Iannuzzo

Ph.D. Center of Reliable Power Electronics (CORPE), Aalborg University, Denmark

Francesco Iannuzzo received the M.Sc. degree in Electronic Engineering and the Ph.D. degree in Electronic and Information Engineering from the University of Naples, Italy, in 1997 and 2002, respectively. He is primarily specialized in power device modelling.

He is currently a professor in reliable power electronics at the Aalborg University, Denmark, where he is also part of CORPE, the Center of Reliable Power Electronics. His research interests are in the field of reliability of power devices, including mission-profile based life estimation, condition monitoring, failure modelling and testing up to MW-scale modules under extreme conditions. He is author or co-author of more than 190 publications on journals and international conferences, three book chapters and four patents. Besides publication activity, over the past years he has been invited for several technical seminars about reliability at first conferences as ISPSD, EPE, ECCE, PCIM and APEC.

Prof. Iannuzzo is a senior member of the IEEE (Reliability Society, Power Electronic Society, Industrial Electronic Society and Industry Application Society). He currently serves as Associate Editor for Transactions on Industry Applications, and is secretary elect of IAS Power Electronic Devices and Components Committee. He was the general chair of ESREF 2018, the 29th European Symposium on Reliability of Electron devices, Failure physics and analysis, which scored +400 participants from 43 countries.

Testing for Reliability of Power Electronic Components

The tutorial introduces the modern principles of testing for reliability of power electronic components. After a short introduction about CORPE – the center of Reliable Power Electronics at Aalborg University, where expectations from power electronics industries will be presented as well, some reliability theory fundamentals will be given, along with practical details about common testing protocols. Wear/life testing types will be then presented and classified, each with its specific aim. The last part will be about the original test approach at Aalborg University, both for Silicon IGBTs and Silicon Carbide MOSFETs, which are by far the most used components in medium-voltage power electronics. Some prospects about failure analysis will conclude the tutorial.

The expected audience includes students and industry engineers who want to get basic-intermediate information about reliability theory and modern challenges.

Tutorials speakers

Venkat Krishnan Ravikumar
Advanced Micro Devices Singapore & Singapore University of Technology and Design, Singapore

Venkat Krishnan Ravikumar received his Master of Science (Microelectronics) from National University of Singapore in 2007 and has been employed as a Senior member of Technical Staff at Advanced Micro Devices Singapore where he has spent the last 13 years performing Electrical Fault Isolation and Failure Analysis on processors built with the cutting-edge technology node. He is additionally a final year candidate for the Doctorate in Philosophy at the Singapore University of Technology and Design researching on electro-optic effects in transistors.

Advanced Fault Isolation Technologies: Design House and Foundry Perspectives

Fault isolation plays a critical role in the overall failure analysis process. Although the eventual objective as one of the initial steps to narrow the failure search area is similar, in fact, there are significant differences in the conduct of fault isolation between design houses and foundries, especially, in advanced applications. Instead of an over-emphasis on the generic descriptions of tools and techniques, this tutorial approaches the topic from different perspectives to present a holistic view on fault isolation. Challenges, future roadmaps and emerging applications will also be discussed.

Scope:

1. Introduction to the role of fault isolation
   a. Failure analysis workflow
   b. Failure debug and yield engineering
   c. Overview of fault isolation techniques (software, hardware, static, dynamic, global, local)
2. Equipment Setup and Workflows
   a. Software-based techniques setup workflow and challenges
   b. Motivation for dynamic fault isolation approaches
   c. Hardware-based techniques setup workflow and challenges
      i. Hard-dock, soft-dock
      ii. Wafer, package
      iii. Challenges: cooling, optical resolution, vibration etc.
   d. Introduction to test fundamentals
      i. Typical test flow, terminologies, common debug tools
3. Global Dynamic Fault Isolation techniques: Concepts/ Principles and Applications
   a. Emission-based (PEM, Thermal, Spectroscopy)
   b. Laser-based (SDL, LADA, TRLADA, FM/LVI, 2nd harmonic, phase mapping, 2pLADA, EeLADA)
4. Local Dynamic Fault Isolation techniques: Concepts/ principles and Applications
   a. Laser-based (LVP)
   b. Nanoprobing
5. Other Emerging Techniques

Tutorials speakers

Baozhen Li
IBM System and Technology Group, Essex Vermont, USA

Baozhen Li is a Senior Technical Staff Member (STSM) at IBM Systems. He has been working on technology reliability for more than 20 years. His experiences cover a wide range of reliability aspects, including electromingttion (EM), stress migration (SM), dielectric breakdown (TDDB), thermal mechanical stability and chip-package interactions (CPI). In addition to reliability studies for leading edge semiconductor technology development, he also works on reliability design optimization and chip level reliability for high end computing systems. He publishes and patents extensively in the semiconductor technology and reliability area. He has given multiple tutorials and invited talks at international conferences and wrote multiple invited introductory papers in journals. He received a bachelor's degree from Northeastern University in China and Ph. D degree from the University of Notre Dame in USA.

MOL & BEOL Reliability Challenges for Advanced Technology Nodes

Aggressive technology scaling places severe challenges on patterning, process integration, material selection and reliability. In this tutorial, the interactions among these challenges will be highlighted. The focus will be on middle of line (MOL) and back end of line (BEOL) reliability challenges including electromigration (EM), dielectric integrity (TDDB), and Stress Migration (SM). After a review of the fundamentals of each reliability mechanisms, details will be given on how the new patterning, integration schemes and material sets impact each of the reliability failure mechanisms. To meet these challenges, demands and progress on new understanding, innovation and reliability models will also be reviewed.

Tutorials speakers

Szu Huat Goh
GlobalFoundries, Singapore

Szu Huat received his BEng and PhD in electrical and computer engineering from the National University of Singapore. He is currently with GLOBALFOUNDRIES, where he leads a team responsible for product failure diagnostics and advanced methodologies to accelerate yield ramp. He focuses on the development of wafer-level dynamic fault isolation techniques combining with cross-functional domain knowledge of software, design and test to enhance yield learning. His current exploration centers on machine learning to enhance FA and yield prediction. He is the technical program chair, general co-chair and general chair for the International Physical and Failure Analysis (IPFA) in 2016, 2017 and 2018

Advanced Fault Isolation Technologies: Design House and Foundry Perspectives

Fault isolation plays a critical role in the overall failure analysis process. Although the eventual objective as one of the initial steps to narrow the failure search area is similar, in fact, there are significant differences in the conduct of fault isolation between design houses and foundries, especially, in advanced applications. Instead of an over-emphasis on the generic descriptions of tools and techniques, this tutorial approaches the topic from different perspectives to present a holistic view on fault isolation. Challenges, future roadmaps and emerging applications will also be discussed.

Scope:

1. Introduction to the role of fault isolation
   a. Failure analysis workflow
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4. Local Dynamic Fault Isolation techniques: Concepts/ principles and Applications
   a. Laser-based (LVP)
   b. Nanoprobing
5. Other Emerging Techniques

Invited speakers

Jianfu Zhang
Liverpool John Moores University, UK

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Challenge and solution for characterizing NBTI-generated defects in nanoscale devices

Negative bias temperature instability (NBTI) is a well-known ageing process for CMOS technologies. Many early works were focused on large devices where device-to-device variations (DDV) are negligible. As device sizes downscale to nanometers, DDV becomes substantial. NBTI is a stochastic process and causes a time-dependent DDV. Characterizing the NBTI-generated defects in nanoscale devices has two main challenges. First, current fluctuates with time and this introduces uncertainties in measurements. Second, the test time is long and costly: to characterize the NBTI-induced DDV, it is essential to repeat the same test on multiple devices. This work reviews recent progresses in addressing these issues. Based on the As-grown-Generation (AG) model, it will be shown that the measurement uncertainties are dominated by As-grown hole traps and can be removed by subtracting the average value. To reduce the test time, the voltage step stress (VSS) technique is combined with the Stress-Discharge-Recharge (SDR) method. This VSS-SDR technique reduces test time to within one hour per device. The model extracted by VSS-SDR is verified by comparing its prediction with the test data obtained under conventional constant voltage stress.

Invited speakers

Lihong Cao
ASE Group, Austin, TX, USA

Lihong Cao is a Director in ASE Group responsible for new packaging technology development (2.5D/3D, FOWLP, FOCoS, PoP, SIP, SESUB), technology promotion, new product introduction, technical program management, strategic planning, and business engagement. Her focusing spans from design, process qualification, root cause analysis and production enablement in HPC (High Performance Computing), AI/MI (Artificial & Machine Intelligence) and 5G/mmWave.

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Lihong received her Doctoral degree in Material Science & Engineering in Wuhan University of Technology and Research Associate Professor in Nanyang Technology University in Singapore. She has published more than 80 technical papers and held several US patents. She has been a Technical Chair and Tutor in ISTFA since 2011. She was invited as panel member in ISTFA 2018.

Challenge for Advanced Package Level Fault Isolation

Complex package application in semiconductor process development requires early feedback on systematic and package level defect-driven detractors. The capabilities of current commonly used for non-destructive analysis tools, such as RTX, SAM, TDR and Thermal Imaging, on advanced packaging for 2.5D/3D, FOWLP, PoP have already been exceeded. It is critical to identify current gaps and forecast expected gaps in the package failure analysis in order to provide solutions. New development for the non-destructive fault isolation techniques are discussed on 3D RTX, EOTPR and Thermal Lock-In. The challenge and future development for these techniques are also addressed.

Invited speakers

Mu-Chun Wang
Minghsin University of Science and Technology, Hsinchu, Taiwan

Mu-Chun Wang got his Ph.D. in Electrical Engineering from Texas A&M University in 1995. He has ever been a senior device manager at UMC/ Taiwan from 1997 to 2001. He is a full professor of Electronic Engineering at Minghsin University of Science and Technology. He has already published over 436 journal and conference peer-reviewed papers, awarded over 52 USA or Taiwan patents in semiconductor and sensor fields and edited two professional textbooks related to TFT display and nano-node CMOS process in Chinese. He served as 41 journal reviewers including 32 SCI journals and 20 TPC in international conferences as well as being the guest editors in 3 SCI journals plus one technical journal. He was invited as a member of Reviewer Board of Sensors in 2018 and nominated as the Best Reviewers of MEAMT in 2017, 2018 and 2019. More than 160 have been with a professional course lecturer, containing in TSMC, UMC, PowerChip, Winbond, VIS, and JHICC, etc.

Punch-through and DIBL Effects Exposing Nano-node SOI FinFETs under Heat Stress

Through the electrical measurement plus the heat stress to enhance the existed or latent defects of FinFETs in the nano-node process flow is a useful metrology. This method not only effectively and timely provides the mapping analysis in a whole wafer, but the sensed data may be correlated to the process variation and optimization in statistical analysis. Besides the common electrical characteristics in ON/OFF current, the punch-through and drain-induced barrier lowering (DIBL) effects are good tools to probe the channel integrity. More process parameters related to these two effects are announced.

Invited speakers

Baozhen Li
IBM System and Technology Group, Essex Vermont, USA

Baozhen Li is a Senior Technical Staff Member (STSM) at IBM Systems. He has been working on technology reliability for more than 20 years. His experiences cover a wide range of reliability aspects, including electromingttion (EM), stress migration (SM), dielectric breakdown (TDDB), thermal mechanical stability and chip-package interactions (CPI). In addition to reliability studies for leading edge semiconductor technology development, he also works on reliability design optimization and chip level reliability for high end computing systems. He publishes and patents extensively in the semiconductor technology and reliability area. He has given multiple tutorials and invited talks at international conferences and wrote multiple invited introductory papers in journals. He received a bachelor's degree from Northeastern University in China and Ph. D degree from the University of Notre Dame in USA.

Advanced On-Chip Interconnect Reliability

For high performance computing applications, the on-chip interconnect not only needs to carry high electrical current and support high Vmax devices, but also must sustain extremely low reliability failure during long product lifetime. To meet these challenges, a good understanding of translating element reliability to system level reliability is essential. In this talk, discussions will be made on reliability failure characteristics and statistics from simple elements to more complicated systems. Examples will be given on electromigration (EM) failure probability from a simple via/line structure to on chip power grid, including how the redundancy and current redistribution impacts EM lifetime and failure statistics. Details will also be discussed on thermal interactions among the neighboring elements and their impact on reliability failure and scaling.

Invited speakers

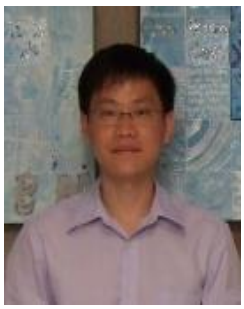
Venkat Krishnan Ravikumar
Advanced Micro Devices Singapore & Singapore University of Technology and Design, Singapore

Venkat Krishnan Ravikumar received his Master of Science (Microelectronics) from National University of Singapore in 2007 and has been employed as a Senior member of Technical Staff at Advanced Micro Devices Singapore where he has spent the last 13 years performing Electrical Fault Isolation and Failure Analysis on processors built with the cutting-edge technology node. He mentors research and development efforts for Fault isolation and is responsible for tool, technique enhancements and technology readiness. He is additionally a final year candidate for the Doctorate in Philosophy at the Singapore University of Technology and Design researching on electro-optic effects in transistors. He has received several best paper awards at failure analysis conferences including the most recent best student paper award at ISTFA 2018.

Challenges in laser probing at spatial resolution compromised technology nodes

Laser probing using NIR lasers at sub-20nm technology has become increasingly difficult due to interaction of the optic probe with multiple transistors. Laser probing waveform is the cumulation of modulations from every active transistor within the optic probe. When multiple transistors are active, they result in “crosstalk” or waveform convolution, resulting in misleading results. In this work, we address some of the typical manifestations of crosstalk and corresponding mitigation strategies for successful probing at resolution compromised technology nodes.

Invited speakers



You Li

Senior Member of Technical Staff, GlobalFoundries, USA

You Li received his B.S. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2003 and M.S. and Ph.D. degrees from the University of Central Florida, Orlando, FL in 2007 and 2010, respectively; all in the electrical engineering. His Ph.D. research work focused on the design of low-capacitance and high-speed Electrostatic Discharge (ESD) devices for low-voltage protection applications. From 2010 to 2012, he worked at Infineon Technologies North America as an application engineer responsible for the system-level ESD protection products. In 2012, he joined IBM as an advisory engineer in the semiconductor research and development center (SRDC), where he worked on the ESD device and model development in 22nm and 14nm Silicon-on-Insulator (SOI) technologies. He has joined GlobalFoundries since 2015 and currently he is leading on ESD devices development in several leading-edge CMOS Bulk and SOI technologies. He is the technical program committee member of EOS/ESD symposium and ESD working group chair of Si2 Compact Model Coalition. He has published over 20 journal and conference papers and granted ~20 patents in ESD area.

ESD Design and Optimization in Advanced SOI and Bulk FinFET Technologies

As advanced CMOS technologies progress from 2-D planar devices to vertical structures such as the three-dimensional FinFET transistors, the achievement of robust on-chip ESD protection design is challenged by the shrinking of ESD design window since the I/O devices fail at lower breakdown voltage and the reduced ESD performance per footprint due to the significant loss of silicon volume. Similar sized ESD elements employed in SOI technology have even lower ESD performance than Bulk counterparts due to the use of thin silicon film and the presence of buried oxide isolation. In this talk, the design and optimization of several ESD devices including ESD diode, Silicon-controlled Rectifier (SCR) and lateral bipolar will be presented in various SOI and bulk FinFET technologies. The key design parameters and engineering approaches are investigated for ESD performance improvement. The efforts of device design and optimization assure the achievement to ESD design target in the advanced FinFET technologies.

Invited speakers

Christian Boit
Technical University of Berlin, Germany (retired)

Christian Boit was Chair of Semiconductor Devices at Technische Universität Berlin from 2002 to 2018, prior to that Director of Failure Analysis at Infineon Technologies AG, Munich, Germany. He was involved in infrared based contactless characterization of electronic devices from 1983, a pioneer of photon emission for Siemens AG 1988 and protagonist of chip backside access techniques from 1996 on. He published more than 150 papers and supported the major conferences of this topic. He was a founding member of EDFAS, served as General Chair of ISTFA 2002 and ESREF 2014 and is member of Acatech, the German Academy of Science and Engineering. In recent years, he also investigated CFI techniques as IC hardware security risk.

Quantitative MIS Characterization Through Electro-Optical Signals

Metal-Insulator-Semiconductor (MIS) systems are the gate structures of FET devices. The characterization uses capacitance-voltages (C-V) curves for identification of flatband and threshold voltages. This presentation discusses how the MIS properties can be transferred into a charge model. The characterization curves of charge over voltage can be contactlessly detected by electro-optical techniques (EOFM, EOP, LVI, LVP). The expected curves will be derived and compared to initial EOFM measurements of FEOL and BEOL test structures.

Invited speakers

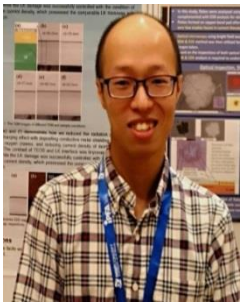
You Wang
Beihang University, Beijing, China

You Wang is a research scientist at the School of Microelectronics, Beihang University. He received B.S. degree in optoelectronics from Huazhong University of Science and Technology, Wuhan, China, in 2011, the engineer diploma and M.S. degree in electrical engineering from University of Paris-Sud, France, in 2013, and the PhD degree in electrical engineering from Institut Mines-Télécom, Télécom Paristech, France, in 2017. He is currently working with the research project of design and development of novel circuits based on fault tolerance analysis of spintronic devices. His research interests include spintronic devices modeling, circuit reliability-aware design and novel circuit designs for low power computing methods and security applications. He has authored/coauthored more than 30 scientific papers and was the recipient of ESREF 2014 best poster award.

Reliability Issues of STT-MRAM and Their Impact on the Performance

Spin transfer torque magnetic random-access memory (STT-MRAM) is considered as a promising candidate for the next generation of memory and computing applications, which may possibly replace SRAM in the future CPU. However, limited to the technology imperfections, STT-MRAM with nanoscale size suffers from considerable reliability issues. This talk will classify the possible reliability issues of STT-MRAM and the current research including theory, experiments and simulations will be presented. Meanwhile, the effects on the performance in terms of access speed, power consumption, area occupancy, PVT robustness, endurance and data retention will be analyzed. Moreover, some possible applications profiting from the intrinsic properties of STT-MRAM will be explored.

Invited speakers



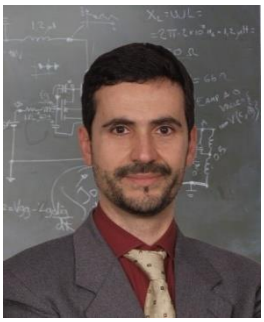
Ching-Chun Lin
integrated Service Technology Inc., Hsinchu, Taiwan

Ching-Chun Lin is a deputy manager at the TEM sample preparation section at the integrated Service Technology Inc (iST). His daily job includes management and development of TEM related activity, such as dual-beam FIB, TEM/STEM, NBD, EDX and EELS analysis. Prior to joining iST, he was a principal engineer at Taiwan Semiconductor Manufacturing Company Limited (TSMC), Hsinchu, Taiwan from 2013 to 2014. His work in TSMC mainly focused on the 16nm Backend of line (BEOL) process integration. He received B.S. degree in chemical engineering in 2006, and Ph.D. in material science in 2012 from Tsinghua University, Hsinchu, Taiwan.

Failure Analysis for Advanced Package Technology

In this talk, the methodology of failure analysis for advanced package technology, such as 3D IC, InFO and CoWos structures is provided. Different failure modes are reported using variety of fault isolation tools. We try to establish the successful pattern to improve the fault isolation based on our experience, which will be discussed in this presentation as well.

Invited speakers



Francesco. Iannuzzo
Ph.D. Center of Reliable Power Electronics (CORPE), Aalborg University, Denmark

Francesco Iannuzzo received the M.Sc. degree in Electronic Engineering and the Ph.D. degree in Electronic and Information Engineering from the University of Naples, Italy, in 1997 and 2002, respectively. He is primarily specialized in power device modelling.

He is currently a professor in reliable power electronics at the Aalborg University, Denmark, where he is also part of CORPE, the Center of Reliable Power Electronics. His research interests are in the field of reliability of power devices, including mission-profile based life estimation, condition monitoring, failure modelling and testing up to MW-scale modules under extreme conditions. He is author or co-author of more than 190 publications on journals and international conferences, three book chapters and four patents. Besides publication activity, over the past years he has been invited for several technical seminars about reliability at first conferences as ISPSD, EPE, ECCE, PCIM and APEC.

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Wear- and Short-Circuit Testing of Silicon Carbide Power MOSFETs

The speech will introduce the present testing techniques for Silicon-Carbide Power Electronic MOSFET, both for wear and short circuit robustness assessment, which are highly demanded for qualification of industrial components. As a major finding, the temperature plays a major role in limiting reliability performance of current-generation devices, and efforts must be devoted in that direction. Modern failure analysis techniques must be used to help in such a process and speed up the learning curve.

Invited speakers

David Su
Taiwan Semiconductor Manufacturing Company, Inc., Taiwan (Retired)

David Su was Director of the Failure Analysis Division of TSMC in charge of reliability-related failure analysis, materials and surface analysis including TEM, and chemical analysis from 2000 until 2018. Prior to joining TSMC, he was Director of TEM and FIB Technology Development at Accurel Systems in Sunnyvale, California (1998-2000). From 1991 to 1998 he was TEM Specialist at the Materials Analysis Group of Philips Semiconductors in Sunnyvale, California. He was an adjunct professor at the Department of Materials Engineering at San Jose State University in San Jose, California from 1989 to 1991. David Su received his B.S. degree in Chemical Engineering from the University of Sao Paulo, Brazil and his M.S. and Ph. D. degrees in Chemical Engineering from Stanford University. He has been a board member of the Taiwan Microscopy Society since 2004. He was a board member of the Electronic Device and Failure Analysis Society of the U. S. (2014-2016) and Chair of the Sematech Integrated-Circuit Failure Analysis Council (2013). He was chairman of the 2010 IRPS Failure Analysis Technical Program and was International Chair for ISTFA 2010, 2011 and International Co-Chair in 2013.

Failure and Materials Analysis in the Logic Integrated Circuit Industry: Status and Challenges in Advanced Nodes

The demands of advanced technology nodes of integrated circuits have pushed failure and materials analysis to their limits. In dynamic fault isolation, improved optical resolution is being constrained by sample preparation. In the materials analysis front, while TEM has very high spatial resolution for imaging, obtaining visual and compositional information, with sub-nanometer resolution, for 3D structures such as fins in FinFET is very challenging. Techniques currently being developed or deployed to address these problems will be discussed including optical and electron beam-based fault isolation, atom probe tomography, He/Ne focused ion beam systems, improvements in FIB and SEM optics and techniques to bring synchrotron-like capabilities to the lab.

Invited speakers

Xing Zhou
Nanyang Technological University, Singapore

Xing Zhou obtained his B.E. degree in electrical engineering from Tsinghua University in 1983, M.S. and Ph.D. degrees in electrical engineering from the University of Rochester in 1987 and 1990, respectively. He has been with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore since 1992. His past research interests include Monte Carlo simulation of photocarrier transport and ultrafast phenomena as well as mixed-mode circuit simulation and CAD tool development. His recent research mainly focuses on nanoscale CMOS compact model development. His research group has been developing a unified core model for nanoscale bulk, SOI, double-gate, nanowire CMOS, as well as III-V HEMTs. He has given more than 140 IEEE EDS distinguished lectures and invited talks at various universities as well as industry and research institutions. He is the founding chair for the Workshop on Compact Modeling (WCM) in association with the NSTI Nanotechnology Conference since 2002. Dr. Zhou was an editor for the IEEE Electron Device Letters (2007–2016), a guest Editor-in-Chief for the special issue of the IEEE Transactions on Electron Devices (Feb. 2014) on compact modeling of emerging devices, and a member of the Modeling & Simulation subcommittee for IEDM (2016, 2017). He was an Elected Member-at-Large of EDS Board of Governors (2004–2009; 2011–2016) and served as Vice-President for Regions/Chapters (2013–2015). He has been an EDS distinguished lecturer since 2000.

Reduction of Current Collapse in GaN (MIS)-HEMTs Using Dual Material Gate

GaN high electron-mobility transistors suffer from various defects or trap states present either in AlGaN barrier or GaN buffer layer. This work presents a different approach to reducing the current-collapse effects in GaN-based transistors by using a dual material gate technology, whereby two different materials having different work functions are merged together to form a single gate, resulting in an improvement of current collapse of around 50%. The current transport efficiency also improves, thus offering improved transconductance. The presence of two gate materials of different work-function modifies the peak electric-field at the drain end, reducing current-collapse and dynamic-$R_{ds,ON}$ degradation.

Invited speakers

Sun Litao
Southeast University, China

Litao Sun is Changjiang Distinguished Professor and serves as the head of School of Electronic Science and Engineering, Southeast University (SEU). He received his PhD from the Shanghai Institute of Applied Physics, Chinese Academy of Sciences in 2005. He worked as a research fellow at the University of Mainz, Germany from 2005 to 2008, and a visiting professor at the University of Strasbourg, France from 2009 to 2010. Since 2008, he joined SEU and honored as a Distinguished Professor. Currently, his research interests focus on: (1) in-situ device microscopy; (2) novel behaviors/properties from sub-10nm materials; (3) applications of nanomaterials in environment, renewable energy and micro/nanosystems. He has published more than 200 peer-reviewed papers including 2 in Science, 13 in Nature and Nature series journals, etc. He holds around 90 patents and has given more than 160 invited presentations. He is the founding chairman of IEEE Nanotechnology Council Nanjing Chapter, the Review Panel member of Graphene Flagship (EU). He has obtained the National Science Fund for Distinguished Young Scholars, Young Leading Talent in Science and Technology Innovation, etc.

In-situ Device Microscopy

With the development of in situ techniques inside transmission electron microscope (TEM), external fields and probes can be applied to individual nanostrucutures, which extends the capability of TEM and may give new insights into the relationship between atomic structure and unique properties of the materials and related devices. Here we review our recent progress in atomic resolution nanofabrication and dynamic characterization of individual nanostructures and nanodevices based on the idea of "setting up a nanolab inside a TEM". Additional probes from a special-designed holder provide the possibility to further manipulate and measure the electrical/mechanical/photoelectric properties of the nanostructures in a TEM.

Invited speakers

Dimitris P. Ioannou
GlobalFoundries, Hopewell Junction, NY 12533, USA

Dimitris Ioannou is a Senior Member of Technical Staff at GlobalFoundries. He received his B.S degree in Physics from the University of Thessaloniki, Greece, and the M.S. and Ph.D. degrees in Electrical Engineering from George Mason University, Fairfax, VA. In 2006, he joined IBM where he played a critical role in the characterization and modeling of reliability mechanisms in advanced Silicon On Insulator (SOI) High-k/Metal Gate CMOS technologies including IBM's 3D TSV technology. As of 2015 he is with GlobalFoundries where he leads the RF reliability of advanced SOI CMOS and SiGe BiCMOS devices. He has published over 40 papers in the field of CMOS reliability.

Hot Carrier reliability assessment strategies in advanced RF SOI technologies for 5G applications

Innovations in reliability characterization and modeling of advanced RF Front-End-Modules (FEMs) are critical for maximizing the reliability margins. Emerging reliability issues and the unique challenges associated with components like Low Noise Amplifiers, Switches and Power Amplifiers are highlighted. Possible strategies and techniques are discussed in view of device mission profile and key Figure-of-Merits for each of the FEM's building blocks.

Invited speakers

Yury Illarionov[1,2]

[1]Institute for Microelectronics (TU Wien), Vienna, Austria

[2]Ioffe Physical-Technical Institute, St-Petersburg, Russia

Yury Illarionov was born in Leningrad (now St.-Petersburg, Russia) in 1988. He received the B.Sc. and M.Sc. degrees from St.-Petersburg State Polytechnical University in 2009 and 2011, respectively. In 2010 he was awarded with Erasmus Mundus scholarship and in 2012 received the double M.Sc. degree from Grenoble INP and the University of Augsburg within the FAME Master program. In 2015 he received the Ph.D. degree from Ioffe Physical-Technical Institute and Dr.techn. degree from TU Wien. Currently Dr. Yury Illarionov is a postdoc at the TU Wien. He is also a research staff member of Ioffe Physical-Technical Institute. The research interests of Dr. Yury Illarionov are centered around FETs with 2D materials and their reliability and scalability. His most recent achievement is demonstration of MoS2 FETs with record-thin 2 nm crystalline CaF2 insulators. Dr. Yury Illarionov has contributed to more than 60 research works, including papers in Nature Electronics, ACS Nano, Advanced Functional Materials, Nano Energy and 2D Materials among others. He is also a member of Mediterranean Institute of Fundamental Physics (MIFP).

Reliability of 2D Field-Effect Transistors: from First Prototypes to Scalable Devices

The rich and fascinating properties of two-dimensional (2D) materials have recently inspired various intriguing ideas for post-silicon nanoelectronics. One of the most far reaching of them is the possible substitution of Si with 2D materials in modern field-effect transistors (FETs). Ideally, this should suppress short-channel effects and thus extend Moore's law below 5 nm channel lengths, while maintaining and possibly even overcoming the high performance of commercial Si devices. However, despite recent progress at fabricating 2D FETs, there is still no commercially competitive transistor technology. One of the main reasons for this is the relatively poor reliability of typical 2D FET prototypes, which suffer from hysteresis and bias-temperature instabilities (BTI) of the transistor characteristics. Despite this, the attention paid to this serious problem is impermissibly low. In my talk I will discuss the main achievements at understanding the reliability of various 2D FETs, from the first prototypes to recently reported scalable devices.

Invited speakers

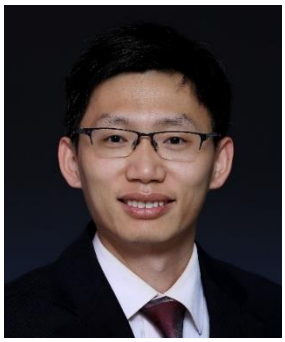
Wu Xing
East China Normal University, China

Dr. Xing Wu received her bachelor's degree in Electronic Engineering from Xi'an Jiaotong University (XJTU) China in 2008 and her PhD degree from Nanyang Technological University (NTU) Singapore in 2012 (supervisor: Prof. Kinleong Pey). Then, she worked at the Singapore University of Design and Technology (SUTD) and Southeast University (SEU). She is currently a professor at East China Normal University (ECNU) China. She has published more than 90 SCI journal papers including Nature Communications, Advanced Materials, Small, and Applied Physics Letters with more than 2000 citations. She holds more than 20 patents.

In situ TEM study on Flexible Electronics Reliability and Failure Analysis

Transmission electron microscopy (TEM), with its high spatial resolution and versatile external fields, is undoubtedly a powerful tool for the static characterization and dynamic manipulation of nanomaterials and nanodevices at the atomic scale. The rapid development of thin-film and precision microelectromechanical systems (MEMS) techniques allows flexile electronics to be probed and engineered inside TEM under external stimuli such as electrical and mechanical, fields at the nanoscale. Here, taking advantage of advanced in situ transmission electron microscopy, we manipulated interfaces of nanomaterials-based flexible pressure sensors. The progress of the in situ TEM paves the way to future wearable devices.

Invited speakers



Bin Gao
Tsinghua University, Beijing, China

Bin Gao is an associate professor with the Institute of Microelectronics, Tsinghua University, Beijing, China. He received the B.S. degree in physics in 2008 from Peking University, Beijing, China, and received the Ph.D. degree in microelectronics from Peking University in 2013. He joint Tsinghua University in 2015. His research interests focus on optimization, characterization and modelling on oxide based RRAM.

Reliability Assessment for Oxide based Neuromorphic Devices and Systems

A perspective is provided to compare the reliability requirements of metal oxide based Resistive Random Access Memory (RRAM) for digital memory application and neuromorphic computing application. Retention and endurance are considered as the two key device metrics to evaluate the impact on neuromorphic system. Statistical measurements and system simulation demonstrate that the retention and endurance degradation behaviors of oxide based RRAM are quite unique when implementing on a neuromorphic system. New evaluation method is therefore needed for reliability assessment.

Invited speakers

Mario Lanza
Soochow University, China

Mario Lanza is a Full Professor at Soochow University since September 2013. Dr. Lanza got his PhD in Electronics in 2010 at Universitat Autonoma de Barcelona. During the PhD he was a visiting scholar at The University of Manchester (UK) and Infineon Technologies (Germany). In 2010-2011 he did a postdoc at Peking University, and in 2012-2013 he was a Marie Curie fellow at Stanford University. Dr. Lanza has published over 100 research papers, including Science, Nature Electronics and IEDM, edited an entire book for Wiley-VCH, and registered four patents (one of them granted with 5.6 Million CNY). He is member of the advisory board of several journals, including Advanced Electronic Materials (Wiley-VCH, Germany), Scientific Reports (Nature Publishing Group, UK), and Nanotechnology (Institute of Physics, UK), and guest editor of a special issue in Advanced Functional Materials (Wiley-VCH, Germany). He is an active member of the technical committee of several world-class international conferences (including IEEE-IEDM, IEEE-IRPS and IEEE-IPFA). Prof. Lanza has received the 2017 Young Investigator Award from Microelectronic Engineering (Elsevier), and the 2015 Young 1000 Talent award (among others), and in 2019 he was appointed as Distinguished Lecturer of the Electron Devices Society (IEEE-EDS). Currently he is leading a research group formed by 15-20 PhD students and postdocs, and together they investigate on the improvement of electronic devices using 2D materials, with special emphasis on two-dimensional (layered) dielectrics and memristors for non-volatile digital information storage and artificial intelligence computing systems.

Erroneous fabrication and reliability characterization of memristors: how to detect it?

Resistive switching (RS) is an interesting property shown by some materials systems that, especially during the last decade, has gained a lot of interest for the fabrication of electronic devices, with electronic nonvolatile memories being those that have received the most attention. The presence and quality of the RS phenomenon in a materials system can be studied using different prototype cells, performing different experiments, displaying different figures of merit, and developing different types of computational analyses. Therefore, the real usefulness and impact of the findings presented in each study for the RS technology will be also different. In this presentation we describe the most recommendable methodologies for the fabrication, characterization, and simulation of RS devices, as well as the proper methods to display the data obtained. The idea is to help the scientific community to evaluate the real usefulness and impact of an RS study for the development of RS technology, and to help researchers to detect those works that (intentionally or unintentionally) show the data in a tricky manner to exaggerate performances and hide weaknesses.

Invited speakers

Kosuke Nagashio
The University of Tokyo, Tokyo, Japan

Kosuke Nagashio received the B.E. degree in Materials Science & Engineering from Kyoto University in 1997 and the M.E. and Ph.D. degrees in Materials Engineering from The University of Tokyo in 1999 and 2002, respectively. From 2002 to 2003, he was a postdoctoral research fellow at Stanford University, California. He is currently an Associate Professor with the Department of Materials Engineering, The University of Tokyo. His research interests presently focus on the synthesis, characterization and electron device application of 2D materials. Dr. Nagashio is a member of the Japan Society of Applied Physics (JSAP), the Materials Research Society (MRS), the IEEE Electron Device Society (EDS) and the American Physics Society (APS).

Reliability of *h*-BN and its application to 2D heterostructure FET

h-BN has been widely utilized as the substrate and gate insulator to achieve high carrier mobility in graphene and 2D layered channel materials. However, the reliability issue of *h*-BN itself had not been focused on, since the 2D heterostructure FET had been investigated mainly by the physics researchers. Therefore, we started to study the reliability of *h*-BN as well as 2D heterostructure FET from the viewpoint of device performance to reveal whether the dielectric breakdowns of 2D layered insulators follow the general breakdown phenomena for 3D amorphous oxides. In this talk, the anisotropic dielectric breakdown of *h*-BN, heterostructure fabrication by dry transfer technique and performance of 2D heterostructure FET are presented. The perspective on the 2D FET application will be discussed.

Technical Program

Time	2 July (Day 0) - Tutorials			
	Symposium Room II		**Symposium Room I**	
	Session TUT A: Tutorials (Reliability) Session Chair: Wardhana A. Sasangka *Singapore-MIT Alliance for Research and Technology, Singapore*		**Session TUT B: Tutorials (Failure Analysis)** Session Chair: Sun Litao *Southeast University, China*	
08:30-10:30	TUT A1	**Reliability of 3D Through-Silicon Via (TSV) Technologies** Dr. Dimitris P. Ioannou *Globalfoundries, USA*	TUT B1	**Principles and Applications of TEM and FIB in the Semiconductor Industry** Dr. David Su *TSMC, Taiwan (Retired)*
10:30-10:45	**Tea Break**			
10:45-12:45	TUT A2	**BTI: Testing and Predictive Modeling** Prof. Jianfu Zhang *Liverpool John Moores University, UK*	TUT B2	**Advanced 2.5D/3D Package Level Failure Analysis** Dr. Lihong Cao *ASE Group, TX, USA*
12:45-13:45	**Lunch**			
13:45-15:45	TUT A3	**Testing for Reliability of Power Electronic Components** Prof. Francesco Iannuzzo *Aalborg University, Denmark*	TUT B3	**Advanced Fault Isolation Technologies: Design House and Foundry Perspectives: PART I** Mr. Venkat Krishnan Ravikumar *AMD, Singapore*
15:45-16:00	**Tea Break**			
16:00-18:00	TUT A4	**MOL & BEOL Reliability Challenges for Advanced Technology Nodes** Dr. Baozhen Li *IBM System and Technology Group, Essex Vermont, USA*	TUT B4	**Advanced Fault Isolation Technologies: Design House and Foundry Perspectives: PART II** Dr. Szu Huat Goh *GlobalFoundries, Singapore*
End of Day 0				

Time	3 July (Day 1)			
09:00-09:10	**Opening Address by General Chair - Prof. Juin J. Liou** ***Zhengzhou University, China***			
09:10-09:15	**Technical Program Briefing by TPC Chair - Zhiwei Liu** ***UESTC, China***			
09:15-09:20	**IPFA 2018 Best Papers Award Presentation**			
09:20-10:20	**KN.1** Session Chair: Juin J. Liou	**Building Reliable Products Guided by Customer Obsession** Prasad Chaparala *Amazon Lab126, USA*		
10:20-10:40	**Tea Break**			
	Symposium Room II		**Symposium Room I**	
	Session 1A: Logic / NVM Device Reliability Session Chair: Jiezhi Chen *Shandong University, China*		**Session 1B: Package Level Failure Analysis** Session Chair: Hong Yang *IME, CAS, China*	
10:40-11:10	Paper ID: 331 Invited (1A.1)	**Challenge and solution for characterizing NBTI-generated defects in nanoscale devices** Jianfu Zhang Liverpool John *Moores University, UK*	Invited (1B.1)	**Challenge for Advanced Package Level Fault Isolation** Lihong Cao *ASE Group, Austin, TX, USA*
11:10-11:30	Paper ID: 289 (1A.2)	**Experiment Characterization of Front and Back Interfaces Impact on Back Gate Modulation in UTBB-FDSOI MOSFETs** Wangyong Chen et al. *Institute of Microelectronics, Peking University, China*	Paper ID: 261 (1B.2)	**Improvement of sensitivity of ultrasonic beam induced resistance change (SOBIRCH) method with ultrasound resonance in the mold resin** Takuto Matsui et al. *Toyohashi University of Technology, Japan*
11:30-11:50	Paper ID: 301 (1A.3)	**Resistive switching in atomic layer deposited and sputtered TiO2 films: electroforming observed by constant voltage stress** Tao Wang et al. *Soochow University, China*	Paper ID: 298 (1B.3)	**Enhancement of localization capability of lock-in thermography for power semiconductor devices by searching high-emissivity films** Norimichi Chinone, Toru Matsumoto and Kazushige Koshikawa *Hamamatsu Photonics K. K, Japan*
11:50-12:10	Paper ID: 283 (1A.4)	**Output Breakdown Characteristics and the Related Degradation Behaviors in Metal Oxide Thin Film Transistors** Xiaotong Ma et al. *Shenzhen University, China*	Paper ID: 128 (1B.4)	**The probe marker discoloration on Al pad and wafer storage** Wen-Fei Hsieh, Henry Lin, Vincent Chen, Irene Ou and YS Lou *Ardentec Cooperation, Taiwan, ROC*

^12:10-12:40 *12:10-12:30	^Paper ID: 330 Invited (1A.5)	**Advanced FinFET Device Reliability** Mu-Chun Wang *MUST, Taiwan*	*Paper ID: 226 (1B.5)	**Signal Processing Method for Scanning Acoustic Tomography Defect Detection based on a Correlation between Ultrasound Waveforms** Masayuki Kobayashi, Kaoru Sakai, Kenta Sumikawa and Osamu Kikuchi *Hitachi, Japan*
12:40-13:40	**Lunch**			
	Session 2A: Interconnect and Packaging Reliability Session Chair: Wardhana A. Sasangka *Singapore-MIT Alliance for Research and Technology, Singapore*		**Session 2B: Case Studies on Fault Isolation** Session Chair: Christian Boit *TU Berlin, Germany*	
13:40-14:10	Paper ID: 337 Invited (2A.1)	**Advanced On-Chip Interconnect Reliability** Baozhen Li *IBM System and Technology Group, Essex Vermont, USA*	Invited (2B.1)	**Challenges in laser probing at spatial resolution compromised technology nodes** Venkat Krishnan Ravikumar *AMD Singapore*
14:10-14:30	Paper ID: 162 (2A.2)	**Self-heating aware EM Reliability Prediction of Advanced CMOS Technology by Kinetic Monte Carlo Method** Linlin Cai et al. *Peking University, China*	Paper ID: 200 (2B.2)	**Using Microprobe to enhance Die Level Static Fault Isolation in Complex IC** Dayanand Nagalingam et al. *Globalfoundries, Singapore*
14:30-14:50	Paper ID: 275 (2A.3)	**CPB fcCSP BGA Package Reliability assessment via the study of Bump Cross Section Morphology after Product Realiability stress testing** Haitham Hamed and Vicky Wang *SK Hynix Memory Solutions, USA*	Paper ID: 114 (2B.3)	**Integrating NI LabVIEW in Soft Defect Localization of Temperature Dependent Voltage Failure** Paul Hubert Llamera, Camille Joyce Garcia-Awitan, Febus Reidj Cruz and Glenn Magwili *Maxim Integrated, Philippines*
14:50-15:10	Paper ID: 156 (2A.4)	**Comparison of Cl effects on Au-Al and Cu-Al HTS and bHAST reliability** Lois Jinzhi Liao et al. *Huawei Technologies, China*	Paper ID: 185 (2B.4)	**Increase Fault Isolation Efficiency by Using Scan Cell Visualizer for Scan Chain Failure** Thin Wei Chua, Loke Sheng Foo, Kim Choo Ng and Keith Serrels *NXP Semiconductors, Malaysia*
15:10-15:30	**Tea Break**			

	Session 3: Exhibitor Session
15:30-18:00	**Thermo Fisher Scientific** (8min) **ZEISS** (6min) **INTEGRATED SERVICE TECHNOLOGY** (6min) **SEMICAPS PTE LTD** (8min) **Kleindiek Nanotechnik** (4min) **TELTEC SEMICONDUCTOR PACIFIC LTD** (4min) **Hamamatsu Photonics (China) Co.,Ltd.** (4min) **Shanghai Winner International Trading CO., Ltd** (4min) **Crest Systems (Suzhou) CO., Ltd** (4min) **Nordson Advanced Technology Systems** (4min) **IMINA TECHNOLOGIES** (4min) **Materials Analysis Technology (Shanghai) Ltd** (4min) **Hitachi High-Technologies Corporation** (4min) **Ellipsiz iNETEST Co., Ltd** (4min) **Ellipsiz iNETest Shanghai CO.,LTD -- SELA Ltd** (4min) **Ellipsiz iNETest Shanghai CO.,LTD -- DIGIT- CONCEPT** (4min) **DIGIT CONCEPT SAS** (4min) **HMC Sales & Service Pte Ltd** (4min) **GALLANT PRECISION MACHINING CO., LTD** (4min) **ZURICH INSTRUMENTS** (4min) **Semishare（shenzhen）technology CO., LTD** (4min) **ESDEMC Technology LLC** (4min) **Platform Design Automation, Inc.** (4min) **WinTech Nano** (4min) **Oxford Instruments** (4min) **Hitachi Power Solution Co. ,Ltd.** (4min) **AMETEK TMC** (4min) **Advantest Corporation** (4min) **Gold Medal Analytical & Testing Group** (4min) **Sanying Precision Instruments Co.,Ltd** (4min) **ATOM SEMICON COMPANY LTD.** (4min) **GIGA FORCE ELECTRONICS CO.,LTD,** (4min) **Toyo Corporation China** (4min) **HANWA ELECTRONIC IND.CO., LTD** (4min) **Radiant Optronics Pte. Ltd** (4min) **JIACO INSTRUMENTS** (4min) **Phenom Desktop SEM** (4min) **Hongzhunda Tech** (4min)
End of Day 1	

Time	4 July (Day 2)			
08:30-09:30	**KN.2** Session Chair: Juin J. Liou	**Emerging Non-Volatile Memory's Applications in Neuro-Inspired Computing and Hardware Security** Shimeng Yu *Georgia Institute of Technology, USA*		
Session 4: Best Paper Exchange Session Chair : Nagarajan Raghavan, *SUTD, Singapore*				
09:30-10:00	ISTFA 2018 Exchange Paper (4.1)	**Scan Chain Fault Isolation using Single Event Upsets Induced by a Picosecond 1064 nm Laser** Keith Serrels *NXP Semiconductors, USA*		
10:00-10:30	ESREF 2018 Exchange Paper (4.2)	**Further Improvements of an Extended Hakki-Paoli Method** Massimo Vanzi *University of Cagliari, Italy*		
10:30-10:50	**Tea Break**			
	Symposium Room II		**Symposium Room I**	
	Session 5A: Transistor Reliability (ESD) Session Chair: Zhiwei Liu, *UESTC, China* and You Li, *Globalfoundries, USA*		**Session 5B: Advanced Electrical Fault Isolation Techniques** Session Chair: Venkat Krishnan Ravikumar *AMD, Singapore*	
10:50-11:20	Invited (5A.1)	**ESD / advanced FinFET device reliability** You Li *Globalfoundries, USA*	Invited (5B.1)	**Quantitative MIS Characterization Through Electro-Optical Signals** Christian Boit *TU Berlin, Germany*
11:20-11:40	Paper ID: 251 (5A.2)	**Modeling and Simulation of Diode Triggered Silicon Controlled Rectifier Behavior Under ESD Stresses** Meng Miao, You Li and Robert Gauthier *Globalfoundries, USA*	Paper ID: 308 (5B.2)	**EOFM measurements of lateral and vertical Bipolar Transistors in Silicon and SiGe:C Technologies** Anne Beyreuther, Tomonori Nakamura, Stefan Keil and Christian Boit *TU Berlin, Germany*
11:40-12:00	Paper ID: 203 (5A.3)	**Investigation of Electrical Parameters Degradations for 600V SOI-LIGBT under Repetitive ESD Stresses** Li Lu, Ran Ye, Siyang Liu and Weifeng Sun *Southeast University, China*	Paper ID: 307 (5B.3)	**EOFM for contactless parameter extraction of low k dielectric MIS structures** Norbert Herfurth, Stefan Keil, Tomonori Nakamura and Christian Boit *TU Berlin, Germany*
12:00-14:00	**Lunch** **Poster Session**			

14:00-14:20	Paper ID: 237 (5A.4)	**A Systematic Failure Analysis Approach to Determine True Electrical Overstress Failures on Integrated Circuits** Em Julius Dela Cruz *Maxim Integrated, Philippines*	Paper ID: 326 (5B.4)	**Fault Localization Using Dynamic Optical-beam Induced Current Variation Mapping** Man Hon Thor et al. *Globalfoundries, Singapore*
14:20-14:40	Paper ID: 150 (5A.5)	**New Approaches in ESD Risk Measurement of PCB Assembling Machines and ESD Countermeasures** Peter Jacob *Empa Duebendorf, Switzerland*	Paper ID: 325 (5B.5)	**Accurate Memory Bitmapping based on Built-in Self-Test: Challenges and Solutions** Lin Zhao, Szu Huat Goh, Ngow Yee Ta and Patrick Chan *Globalfoundries, Singapore*
14:40-15:00	Paper ID: 285 (5A.6)	**Failure Analysis of Microwave Module by ESD Effect** Zhimin Ding et al. *China Academy of Space Technology, China*	Paper ID: 256 (5B.6)	**Characterization of 1122nm Laser for Laser Based Fault Isolation Applications** Vasanth Somasundaram, Yi Xuan Seah, Venkat Krishnan Ravikumar, Angeline Phoa and Choon Meng Chua *AMD, Singapore*
15:00-15:20	Paper ID: 204 (5A.7)	**Capacitor Modeling Methodology for System-level ESD Simulation** Li Xiang, Xie Xiaofei, Xia Nan and Gu Zhengdong *Huawei Technologies, China*	Paper ID: 121 (5B.7)	**Cycle-Shift Scan Chain Failure Analysis Using Single Pulse Test Pattern** Eric Paulraj, Chwee-Lin Choong and Yiang Won Chai *Intel Technologies, Malaysia*
15:20-15:40	**Tea Break**			
	Session 6A: Transistor Reliability Session Chair: Xinnan Lin *Peking University Shenzhen Graduate School*		**Session 6B: Case Studies on Fault Isolation** Session Chair: Szu Huat Goh *Globalfoundries, Singapore*	
15:40-16:10	Invited (6A.1)	**Reliability of STTRAM Devices** You Wang *Beihang University, China*	Paper ID: 334 Invited (6B.1)	**Failure Analysis for Advanced Package Technology** Ching-Chun Lin and Kim Hsu *Integrated Service Technology, Taiwan*
16:10-16:30	Paper ID: 210 (6A.2)	**Understanding lifetime prediction methodology for In0.53Ga0.47As nFETs under Positive Bias Temperature Instability (PBTI) condition** Zhigang Ji, Xiong Zhang and Jianfu Zhang *Liverpool John Moores University, China*	Paper ID: 191 (6B.2)	**Root cause analysis on analog circuit using TR-LADA** Winson Lua, Venkat Krishnan Ravikumar, Angeline Phoa, Gopinath Ranganathan and Girish AS *AMD, Singapore*

16:30-16:50	Paper ID: 262 (6A.3)	**Comparison of NBTI kinetics in RMG Si p-FinFETs featuring ALD W Filling Metal Using B2H6 and SiH4 Precursors** Longda Zhou et al. *University of Chinese Academy of Sciences, China*	Paper ID: 178 (6B.3)	**Optical Failure Analysis on Pulsed Signals Embedded in Logic Cloud – A Case Study of Laser Voltage Tracing** Yuzhu Sun et al. *Thermo Fisher Scientific, USA*
16:50-17:10	Paper ID: 279 (6A.4)	**Impact of Channel Doping on NBTI Reliability and Variability in Nanoscale FinFETs** Zhe Zhang, Runsheng Wang, Yangyuan Wang and Ru Huang *Peking University, China*	Paper ID: 305 (6B.4)	**Methodology to Investigate the Root Cause of Threshold Voltage Drift of Transistor Devices using Capacitance Voltage Measurements** Chung Keow Ang et al. *Infineon Technologies, Malaysia*
17:10-17:30	Paper ID: 264 (6A.5)	**Study of Internal Latchup Behaviors in Advanced Bulk FinFET Technology** Wei Liang, Robert Gaunthier Jr, Souvick Mitra, You Li *Globalfoundries, USA*		
End of Day 2				
18:00-21:30	**IPFA 2019 BANQUET**			

Time	5 July (Day 3)			
	Symposium Room II		**Symposium Room I**	
	Session 7A: Reliability and Failure Analysis of Power Devices Session Chair: Min Ren *UESTC, China*		**Session 7B: Case Studies on Physical Faiure Analysis** Session Chair: Changze Liu *HiSilicon, China*	
08:30-09:00	Invited (7A.1)	**Wear- and Short-Circuit Testing of Silicon Carbide Power MOSFETs** Francesco Iannuzzo *Aalborg University, Denmark*	Invited (7B.1)	**Failure and Materials Analysis in the Logic Integrated Circuit Industry: Status and Challenges in Advanced Nodes** David Su *TSMC (Retired), Taiwan, R.O.C*
09:00-09:20	Paper ID: 132 (7A.2)	**High Resolution Mapping of Defects at SiO2/SiC Interfaces by Local-DLTS Based on Time-Resolved Scanning Nonlinear Dielectric Microscopy** Yuji Yamagishi and Yasuo Cho *Tohoku University, Japan*	Paper ID: 219 (7B.2)	**An Effective Monitored and Improved Method to Control Moisture for Outgoing FOSB** Yi-Ying Chen, Chiu-E Tseng, Hsin-Wen Fan and Chih-Chao Pai *Powerchip Corporation, Taiwan, R.O.C*
09:20-09:40	Paper ID: 288 (7A.3)	**Failure Analysis on TiAl Metallization Process for Ohmic Contact on 4H-SiC pMOSFET** Chia Lung Hung, Jung-Chien Cheng and Bing-Yue Tsui *National Chiao Tung University, Taiwan, R.O.C*	Paper ID: 222 (7B.3)	**The Application of Thermal Sensor to Locate IC Defects in Failure Analysis** Authors: Kuan-Chieh Huang and Yi-Chen Lin, *Powerchip Corporation, Taiwan, R.O.C*
09:40-10:00	Paper ID: 228 (7A.4)	**Repetitive-avalanche-induced Electrical Degradation and Optimization for 1.2kV 4H-SiC MOSFETs** Hao Fu, Jiaxing Wei, Siyang Liu, Wangran Wu and Weifeng Sun *Southeast University, China*	Paper ID: 165 (7B.4)	**The Case of Failure Analysis of the PCBA Wire Corrosion under High Reliability Requirements** Zheng Jie et al. *CEPREI, China*
10:00-10:20			Paper ID: 247 (7B.5)	**Metallic Trace Contaminant Detection Using SEM/EDX** Aaron Lee, Bernice Zee and Fang Jie Foo *AMD, Singapore*
10:20-10:40	**Tea Break**			

	Session 8A: Reliability and Failure Analysis of RF and Power Devices Session Chair: Liu Siyang, *Southeast University, China*		**Session 8B: Advanced Phyisical Failure Analysis Techniques** Session Chair: Wu Xing, *ECNU, China*	
10:40-11:10	Paper ID: 233 Invited (8A.1)	**Reduction of current collapse in GaN (MIS)-HEMTs using dual material gate** Binit Syamal and Xing Zhou *Nanyang Technological University, Singapore*	Invited (8B.1)	**In-situ device microscopy** Sun Litao *South East University, China*
11:10-11:30	Paper ID: 212 (8A.2)	**100V Integrated Bootstrap Diode with Dynamic Field Limiting Rings for Solving Reverse Recovery Failure in GaN Gate Driver ICs** Ajiang Li et al. *Southeast University, China*	Paper ID: 318 (8B.2)	**Probing SRAM Signals for Yield Management** Greg Johnson et al. *Carl Zeiss, USA*
^11:30-12:00 *11:30-11:50	^Invited (8A.3)	**Hot Carrier reliability assessment strategies in advanced RF SOI technologies for 5G applications** Dimitris P. Ioannou *Globalfoundries, USA*	*Paper ID: 146 (8B.3)	**Simultaneous 2D carrier polarity (dC/dV) and density (dC/dz) distribution measurement of Si/SiC MOSFET based on scanning nonlinear dielectric microscopy** Takehiro Yamaoka et al. *Hitachi High-Technologies Corporation, Japan*
11:50-13:00	**Lunch**			
	Session 9A: 2D Materials and Devices: Reliability and Failure Analysis Session Chair: Mario Lanza *Soochow University, China*		**Session 9B: Emerging Technologies in Failure Analysis Techniques** Session Chair: Zhigang Ji *Liverpool John Moores University, UK*	
13:00-13:30	Paper ID: 333 Invited (9A.1)	**Reliability of 2D Field-Effect Transistors: from First Prototypes to Scalable Devices** Yury Illarionov *TU Wien, Austria*	Invited (9B.1)	**In situ TEM Study on Flexible Electronics Reliability and Failure Analysis** Wu Xing *ECNU, China*
13:30-13:50	Paper ID: 181 (9A.2)	**Performance Variability and Analog Behaviors of Memristive Devices with New Transition Metal Carbide** Fei Gao et al. *Nanjing University of Posts and Telecommunications, China*	Paper ID: 290 (9B.2)	**Study of Front-Side Approach to Retrieve Stored Data in Non Volatile Memory Devices Using Scanning Capacitance Microscopy** Jing Yun Tay, Jason Cheah, Qing Liu and Chee Lip Gan *Nanyang Technological University, Singapore*

13:50-14:10	Paper ID: 324 (9A.3)	**Low Power Resistance Switching Devices and Its High-Density Crossbar Arrays with a Novel 2D Material MXene for Performance Improvement of Reliability** Nan He et al. *Nanjing University of Posts and Telecommunications, China*	Paper ID: 276 (9B.3)	**The impact of endurance degradation in Analog RRAM for in-situ training** Yuyi Liu, Bin Gao, Huaqiang Wu, Meiran Zhao and He Qian *Tsinghua University, China*
^14:10-14:40 *14:10-14:30	^Invited (9A.4)	**Reliability Assessment for HfOx based Neuromorphic Devices / Systems** Bin Gao *Tsinghua University, China*	*Paper ID: 265 (9B.4)	**Generation and tracking of optical signals inside the IC to improve device security and failure analysis** Elham Amini, Jean-Pierre Seifert and Christian Boit *TU Berlin, Germany*
14:30-15:00	**Tea Break**			
	Session 10A: Transistor and 2D Materials Reliability Session Chair: Nagarajan Raghavan *SUTD, Singapore*		**Session 10B: Sample Preparation and Defect Characterisation** Session Chair: Sun Litao *Southeast University, China*	
^15:00-15:30 *15:00-15:20	^Invited (10A.1)	**Erroneous fabrication and reliability characterization of memristors: how to detect it?** Mario Lanza *Soochow University, China*	*Paper ID: 249 (10B.1)	**Application of Laser Deprocessing Technique in Physical Failure Analysis on Memory Bit-counting** Yanlin Pan et al. *Globalfoundries, Singapore*
^15:30-16:00 *15:20-15:40	^Invited (10A.2)	**Defect Properties and Charge Transport in h-BN / MoS2-based FET devices** Kosuke Nagashio *University of Tokyo, Japan*	*Paper ID: 220 (10B.2)	**Application of SIMS for the characterization of Nitrogen in TaN film** Yun Wang et al. *Globalfoundries, Singapore*
15:40-16:00			Paper ID: 273 (10B.3)	**Poly-Si Unetch Failure Due to Etching Rate Dependence of Si Orientation** Dahyun Nam et al. *Samsung Electronics, Korea*
16:00-16:20	Paper ID: 299 (10A.3)	**Tristate resistive switching analysis in graphene/hexagonal boron nitride/graphene cross-point memristors** Kaichen Zhu et al. *Soochow University, China*	Paper ID: 277 (10B.4)	**Three-dimensional Structure Recognition of Circuit Patterns on Semiconductor Devices Using Multiple SEM Images Detected in Different Electron Scattering Angles** Kenji Yasui, Mayuka Osaki, Atsushi Miyamoto and Hitoshi Namai *Hitachi, Japan*

16:20-16:40	Paper ID: 284 (10A.4)	**Light-Illumination-Induced Degradation and Its Long-Term Recovery in Indium-Tin-Zinc Oxide Thin-Film Transistors** Meng Zhang et al. *Shenzhen University, China*	Paper ID: 214 (10B.5)	**4-Point-Bending Characterization of Interfacial Adhesion Strength of Co-Zr-Ta and Co-Zr-Ta Variant Thin-Film Stacks** Xintong Zhu et al. *Globalfoundries, Singapore*
16:40-17:10	**Conference Closing Ceremony** **Best Poster Awards - Annoucement** **Introduction to IPFA 2020, Marina Bay Sands, Singapore**			
End of Day 3				

Poster Paper Information

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
1.1	**129**	**TEM-EDX Line Scan to Investigate O2 Diffusion across Physical Vapor Deposited Al-Cu Layer** Wan Tatt Wai, Ong Jia Sheng, Loh Yeong Jia and Low Lynn Yien *Infineon Technologies, Malaysia*
1.2	**223**	**Application of Nanoindentation method to characterize adhesion strength of polyimide films** Xiaoxuan Li, Xintong Zhu, Xiaodong Li, Yi Liu, Ramasamy Chockalingam, Ramesh Rao Nistala and Zhi Qiang Mo *Globalfoundries, Singapore*
1.3	**205**	**An Efficient and Non-destructive Grounding Method for Passive Voltage Contrast Fault Isolation** Irene Tee, Jie Zhu, Zhiqiang Mo and Kok Wah Lee *Globalfoundries, Singapore*
1.4	**211**	**Endpoint Detection Methods in Implementing AI-assisted Polishing Process** Hao Tan, Jacobus Leo, Shreyas Mohan Parab, Krishnanunni Menon, Yuzhe Zhao, Yanlin Pan, Changqing Chen and Pik Kee Tan *Globalfoundries, Singapore*
1.5	**190**	**An Improved Analysis Method on Si-Photonics Waveguide Sidewall Roughness** Hao Tan, Xintong Zhu, Poh Chuan Ang, Yuzhe Zhao, Krishnanunni Menon, Yanlin Pan, Changqing Chen and Pik Kee Tan *Globalfoundries, Singapore*
1.6	**224**	**Study of Charge Neutralization Techniques to Prevent Copper Corrosion On Post-FIB Wet Stained Sample** Sharon Lee, Li Hong Li, Ley Hong Khoo, Poh Chuan Ang and Zhi Qiang Mo *Globalfoundries, Singapore*
1.7	**320**	**Sample Preparation in Recover Physical Defects on MIM Related failure for Different Devices In Wafer Fabrication** Elaine Ng Hui Peng, Naiyun Xu, Dayanand Nagalingam, Tan Pik Kee, Angela TEO, Fransiscus Rivai and Changqing Chen *Globalfoundries, Singapore*
1.8	**153**	**A Novel MIM sandwich structure of the SCM probe for tool inspection** Yu Chen Huang, Yuan Wei Li, Jerry Tsai and Chenglong Pan *United Microelectronics, Taiwan, R.O.C*
1.9	**148**	**Backside Preparation by Milling Approach of Module Device for Failure Analysis** Kevin Emmanuel Jr Fulla, Mark Anthony Acedillo, Febus Reidj Cruz and Flordeliza Valiente *Maxim Integrated, Philippines*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
1.10	**221**	**Selective Mechanical Backside Grinding of CSP-BGA and SOIC-CAV devices in preparation for Backside Failure Analysis** Melissa Caseria and Dennis Madrinan *Analog Devices, Philippines*
1.11	**232**	**Reliability Hazard Characterization of Wafer-level spatial metrology parameters based on LOF-KNN method** Jinli Zhang, Hailong You and Renxu Jia *Xidian University, China*
1.12	**238**	**A Study of Lead Tip Corrosion and Its Impact to Products Reliability** Yen Fu Liu, Nicolas Liu, C.K. Wu, Sean Tsao and C.H. Wu *Texas Instruments Taiwan Limited, Taiwan, R.O.C*
1.13	**252**	**Sample Preparation for testing from Molded Wafer Level Chip Scale Package** Tang Chih Yi, Yu Chi Wang, C.C. Huang and S.M. Huang *NXP Semiconductors, Taiwan, R.O.C*
1.14	**281**	**Correlation Analysis and Characterization of Micromorphology and Optoelectronic Properties of SiO2/SiC in Pressure Sensor** Limei Rong, Jinze He, Jiangfeng Du, Tiancheng Luo, Rongsen Yang, Kun Gao, Qi Yu, Jiao Xu, Guanghong Zhao and Yugang Yin *University of Electronic Science and Technology of China*
1.15	**302**	**Effect of probe station tips pressure in the characterization of memristors** Mario Lanza, Ying Zuo, Kaichen Zhu, Xu Jing, Biyu Guo, Tao Wang, Jonas Weber, Marco A. Villena and Guenther Benstetter *Soochow University, China*
1.16	**303**	**Reliability considerations about 3D electrical characterization via Scalpel AFM** Shaochuan Chen, Xu Jing, Lanlan Jiang, Yanfeng Ji, Fei Hui, Yuanyuan Shi and Mario Lanza *Soochow University, China*
1.17	**199**	**How To Determine Fluorine Contamination Level On A Normal Al Bondpad?** Younan Hua *Wintech Nano Technology Services, Singapore*
1.18	**310**	**Study of Silicon thickness for electron transparency** Han Keat Tan, Bing Hai Liu, Meai Ling Chooi, Younan Hua and Xiao Min Li *Wintech Nano Technology Services, Singapore*
1.19	**243**	**Study of cross contamination between InP substrate and Silicon substrate during Phosphors depth profile measurement** Mengxue Wu, Lei Zhu, Jiahui Liu, Younan Hua and Xiaomin Li *Wintech Nano Technology Services, Singapore*
2.1	**133**	**VIA Defect Localization Methodology on SOI Technology Mixed Signal IC** Gaojie Wen, Fei Liu, Hao Zhang, Li Tian, Shijun Zheng and Yanfen Wang *NXP Semiconductor, China*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
2.2	**138**	**The Application and Real Case for Electron Beam Absorbance Current in Failure Analysis** Li Tian *NXP Semiconductor, China*
2.3	**227**	**Study on Loop Circuit Function Fail Isolate Method** Jon Ren, Gaojie Wen and Bird Fan *NXP Semiconductor, China*
2.4	**235**	**Fault Isolation based on Functional I-V Characteristic Analysis** Jinrong Song, Diwei Fan, Gaojie Wen, Li Tian, Xiaocui Li and Changyan Qi *NXP Semiconductor, China*
2.5	**244**	**FIB Assist in Routine Laser-based Analysis Techniques and Photon Emission Microscopy on Mixed-Signal Devices** Chi He *NXP Semiconductor, China*
2.6	**152**	**The Solutions of Bit Line Failure Analysis: Low kV E-Beam, EBAC and LVI** Link Chang, Rick HC Wang, Andy CH Chang, Simon TC Wang, Yu Pang Chang and Chaogang Song *United Microelectronic Corporation, Taiwan, R.O.C*
2.7	**176**	**Backside and Topside OBIRCH Defect Localization on Multi-layer Finger Structure MOSFET Capacitor with the aid of Focused Ion Beam (FIB)** Ronald Apolinaria, Febus Reidj Cruz and Flordeliza Valiente *Maxim Integrated, Philippines*
2.8	**253**	**Soft Defect Localization (SDL) of Temperature Dependent Failure using NI-PXI Test Platform in DALS System** Jed Paolo Deligente *Maxim Integrated, Philippines*
2.9	**239**	**Enhancing the SRAM Failure Analysis Process** Raymond Mendaros, Analog Devices General Trias *Philippines*
3.1	**117**	**Silicon Precipitates Counts and Size Study in Aluminium Bond Pads** Wei Lee Lim, Azlin MohdNoor Mohamad Esa and Michael Raj Marks *Infineon Technologies, Malaysia*
3.2	**130**	**Combined Application of AFM-XRD-SIMS to Characterize Crystal Properties in Electroless Nickel Metal Induced by Trace Contaminants** Wan Tatt Wai, Lee Wei Cheat, Lim Saw Sing and Zakaria Nurhanani *Infineon Technologies, Malaysia*
3.3	**215**	**Planar Staining Technique for Photoresist Related Implantation Issue** Li Hong Li, Sharon Lee, Jin Yang, Poh Chuan Ang and Zhi Qiang Mo *Globalfoundries, Singapore*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
3.4	**319**	**Failure Analysis of Solder Joint Cracking in a CBGA Assembly Applied for Aviation Equipment** Hui Xiao, Daojun Luo and Weiming Li *China CEPREI Laboratory, China*
3.5	**122**	**Nanoprobing Analysis on MOSFET Current Drift Caused by Gate Oxide Defect** Wei Huang, Tze Ping Chua, Hong Bo Zhang and Chaogang Song *United Microelectronics Corporation, Singapore*
3.6	**123**	**Using Higher Accelerating Voltage of SEM to Dig Out Implant Defects** Wen Cheng Hsu, Yu Hsiang Shu and Chenglong Pan *United Microelectronics Corporation, Taiwan, R.O.C*
3.7	**306**	**A Study of Bonding Pad Corrosion Caused by Contamination** HAO GAN, LIN SHI, Xiuqun Zhang and Hongsheng Dai *ZTE Corporation, China*
3.8	**207**	**GaAs pHEMT Single Pole Double Throw(SPDT) RF Switch Failure Analysis** Shi Lin, Qiang Li, Hongsheng Dai, Zhida Wang, Huanqiang Jing *ZTE Corporation, China*
3.9	**164**	**Systematic Study on Failure Information of Thick Film Hybrid Integrated Circuit** Zhang Xiaowen, Lv Hongjie and Liu Xing *Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, China*
3.10	**187**	**Analysis of a novel EOS failure due to stray voltage during ICT testing** Weiwei Zhang, Yi Zhang and Yuanxin Lee *H3C Corporation, China*
3.11	**189**	**Case study of on-board optical module failure induced by PDMS** Yu Yang and Lee Yuanxin *H3C Technologies Cooperation, China*
4.1	**115**	**A study on an abnormal oxidation issue of copper bonding wire** Lois Liao et al., *Wintech Nano-Technology Services, Singapore*
4.2	**120**	**Enhanced Package Fault Isolation Method Using Time Domain Reflectometry (TDR) Incorporation with Mathematics** Lee Lan Yin and Kok Keng Chua *Xilinx Asia Pacific, Singapore*
4.3	**180**	**Case Study on Package Level Defect Localization through Optimized Lock-in Thermography Frequency** Carlo Casabuena and Em Julius Dela Cruz *Maxim Integrated, Philippines*
4.4	**186**	**A Failure Analysis of a SOP IC Creep Corrosion on power module** Weiwei Zhang, Yuanxin Lee and Yi Zhang *H3C Corporation, China*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
4.5	**209**	**Electrical field accelerated GND corrosion of copper wire in high humidity conditions** Xuanlong Chen, Jianming Fang, Wenfeng Huang, Yong Wei and Chengcheng Chen *China CEPREI Laboratory, China*
4.6	**246**	**High-resolution 3D X-ray Microscopy for Structural Inspection and Measurement of Semiconductor Package Interconnects** Syahirah Mohammad-Zulkifli, Bernice Zee, Gregorich Thomas, Allen Gu, Yanjing Yang, Weijie Lee and Masako Terada *Advanced Micro Devices, Singapore*
4.7	**258**	**Defect Location and Physical Analysis in Chip-on-chip Device** Zhibin Wang, Zhaoxi Wu, Jiajia Sun and Chao Duan *China Aerospace Components Engineering Center, China*
5.1	**163**	**Investigation of Elimination of E-beam Effect by UV Cure** Aibing Xun and Li Lung Lai *Semiconductor Manufacturing International Corporation, China*
5.2	**169**	**How to Realize Electro Optical Frequency Mapping/Probing (EOFM/EOP) by Test Configure Debug in Failure Analysis of Advanced Mix-signal Devices** Haus Zhang, Jianli Yang, Gaojie Wen, Li Tian and Winter Wang *NXP Semiconductor, China*
5.3	**196**	**Advanced Method to Locate The Defect on Zener Diode to Avoid Cutting The Circuit in Failure Analysis** Qian Xuejian, Li Tian, Wen Gaojie, Zhang Hao and Li Xiaocui *Freescale Semiconductor, China*
5.4	**296**	**Practical Dynamic Laser Stimulation Technique and Code Modification: A Soft Defect Localization Approach for Microcontroller Self-test Failures** Kevin Joshua Cala, Junald Saludares and Wendel Basbas *Microchip Philippines Failure Analysis, Philippines*
5.5	**309**	**Innovative Methodology for Short Circuit Failure Localization by OBIRCH Analysis** Yong Khai Oooi and Jack Yi Jie Ng *Intel Microelectronics, Malaysia*
6.1	**145**	**Advanced TEM application in 10nm below technology node device analysis** Hong Yang, Yongliang Li, Huilong Zhu, Xiaogen Yin and Anyan Du *Institute of Microelectronics, Chinese Academy of Sciences, China*
6.2	**154**	**Advanced 3D Optical Imaging for Die Surface Topographic Analysis** Lai-Seng Yeoh *Cypress Semiconductor, Malaysia*
6.3	**173**	**Si Nano-Crystal Size and Structural Defect Characterization Using Electron Microscopes** Elizabeth Sebastian, Jie Zhu and Zhi Qiang Mo *Globalfoundries, Singapore*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
6.4	**217**	**Case Study on Precise Boron Quantification of Mixed MatrixAuthors** Kian Kok ONG, Yun Wang, Han Wei Teo, Ramesh Rao Nistala and Zhi Qiang Mo *Globalfoundries, Singapore*
6.5	**218**	**Defect Characterization by Differential Phase Contrast Imaging Technique in Scanning Transmission Electron Microscope** Ching-Chun Lin and Kim Hsu *Integrated Service Technology, Taiwan, R.O.C*
6.6	**270**	**In-depth Analysis of 10 nm Exynos Processor using Micro CT and FIB-SEM System** Sharang Sharang, Jiri Dluhos, Dominika Kalasova, Andrey Denisyuk, Rostislav Vana, Tomas Zikmund, Jozef Kaiser and Jozef Vincenc Obona *Tescan Orsay Holding, Czech Republic*
7.1	**139**	**The likelihood of multiple bit-flips due to neutron strikes and its implications on circuit designs** Nanditha Rao and Madhav Desai *IIT Bombay, India*
7.2	**234**	**When provocation tests, design of experiments and advanced statistical modeling complement each other to allow estimation of product sensitivity to a defect: case study of a delamination failure for automotive semiconductors** Corinne Berges *NXP, France*
7.3	**322**	**An overview of failure analysis expert system based on Bayesian networks** Hongjian Wang, Liyuan Liu, Zeya Peng and Youliang Wang *Reliability Research and Analysis Center, CEPREI, China*
8.1	**241**	**Low-Trigger LDMOS-SCR For ESD Protection Of Single Photon Detector** Yang Wang and Xiangliang Jin *Hunan Normal University, China*
8.2	**192**	**A new study of backend process on 0.18um BCD NLDMOS on-state BV characteristics** Shuxian Chen, Feng Lin, Bin Yang, Chunxu Li and Yu Huang *CSMC, China*
8.3	**193**	**A study of n-LDMOS Off-state Breakdown Degradation with 0.18μm BCD Technology** Feng Lin, Bin Yang, Guipeng Sun, Shuxian Chen, Chunxu Li, Yu Huang and Qiong Wang *CSMC, China*
8.4	**206**	**EMMI Abnormal Hotspot Study for Latch-Up Simulation** Chia-Sheng Huang, Xuan-Chao Guo, Zhi-Wei Chen, Shin-Chia Lin and Sheng-Ru Zhang *Powerchip Technology Corporation, Taiwan, R.O.C*
8.5	**177**	**PBTI Study in Native High Voltage Device** Tsai Bo-an, Peng Zi-an, Chuang Hsiao-wen, Chen Chien-fu and Hsu Cheng-yuan *Technology Development Division IV, Powerchip Semiconductor Manufacturing Corporation, Taiwan, R.O.C*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
8.6	**229**	**Modeling IC Snapback Characteristics Using a VCCS Model for Circuit-Level ESD Simulation** Yunhao Li, Yize Wang and Yuan Wang *Peking University, China*
8.7	**314**	**Impact of low temperature on the TSG Vt shift during erase cycling of 3-D NAND Flash memory** Da Li, Lei Jin, Liang Yan, Xinlei Jia, Jianquan Jia, Yali Song, An Zhang, Feng Xu, Wei Hou, Zongliang Huo and Jianhua Feng *Peking University, China*
8.8	**259**	**Analysis of Drain Current and Seebeck Coefficient for Organic TFTs Using Activation Energy** Yong Huang, Junli Yin, Xinlin Wang, Hongyu He and Shengdong Zhang *University of South China, China*
8.9	**260**	**Design of a dual-directional diode-triggered SCR for low voltage ESD protection** Qiang Xu, Hailian Liang and Xiaofeng Gu *Jiangnan University, China*
8.10	**266**	**Investigation of Conductance Fluctuations of Analog RRAM during Weight Update Process with Kinetic Monte Carlo Simulation** Feng Xu, Bin Gao, Huaqiang Wu and He Qian *Tsinghua University, China*
8.11	**282**	**Effect of Active Layer Thickness on Device Performance and Hot Carrier Instability in Metal Induced Crystallized Polycrystalline Silicon Thin-Film Transistors** Zhendong JIANG, Meng ZHANG, Xiaotong Ma, Yan Yan, Guijun Li, Sunbin Deng, Wei Zhou, Rongsheng Chen, Man Wong and Hoi-Sing Kwok *Shenzhen University, China*
8.12	**293**	**Gate-Voltage-Stress-Induced Instability in C8-BTBT Thin-Film Transistors with Aluminum Oxide as Gate Dielectric** Yan YAN, Zizhen HUANG, Xiaotong MA, Zhendong JIANG and Meng ZHANG *Shenzhen University, China*
8.13	**291**	**Analysis of Turn-on Uniformity of Multi-finger DDSCR Devices under ESD Stress** **Yang Wang, Dandan Jia, Xijun Chen and Xiangliang Jin** ***Xiangtan University, China***
8.14	**294**	**Comparative Study of Total Ionizing Dose Effects on the Silicon-Controlled Rectifier Devices for HV and LV ESD protections** Zhuojun Chen, Wenzhao Lu, Ming Wu, Wei Peng, Yun Zeng and Xiangliang Jin *School of Physics and Electronics, Hunan University, China*
8.15	**131**	**Analysis of SEE modes in ferroelectric random access memory using heavy ions** Jianan Wei, Hongxia Guo, Fengqi Zhang, Gang Guo and Chaohui He *XJTU, China*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
8.16	**134**	**Radiation-Hardened Memory Cell for Ultralow Power Space Applications** Chunhua Qi, Tianqi Wang, Chaoming Liu, Guoliang Ma, Liyi Xiao, Heyi Li, Yanqing Zhang, Mingxue Huo and Guofu Zhai *Harbin Institute of Technology, China*
8.17	**149**	**Design and Verification of SRAM Self-Detection Repair Based on ECC and BISR Circuit** Yanqing Zhang, Yinghun Piao, Mingxue Huo, Tianqi Wang, Guoliang Ma, Chaoming Liu, Jianning Ma and Chunhua Qi *Harbin Institute of Technology, China*
8.18	**151**	**Design of Radiation-Hardened Image Compressor Based on Lossless JPEG-LS** Chunhua Qi, Jianning Ma, Mingxue Huo, Tianqi Wang, Guoliang Ma, Chaoming Liu, Yinghun Piao and Yanqing Zhang *Harbin Institute of Technology, China*
9.1	**143**	**Robust Package Development for Automotive Industrial Application** Kheaw Chung Chng, Kok Keng Chua, Su Fang Chew and Xueren Zhang *Xilinx Asia Pacific, Singapore*
9.2	**216**	**Calculating Activation Energy (Ea) of SRAM Product Using The Vmin Variation Method** Wu-Han Tseng, Shuen-Chao Kuo and Kuan-Chieh Huang *Powerchip Semiconductor Corporation, Taiwan, R.O.C*
9.3	**225**	**Research on SRAM Exhibiting Abnormal Behaviors Electrical Characteristics after Accelerated Stress in Reliability** Yi-Heng Chen and Yi-Ying Chen *Powerchip Semiconductor Corporation, Taiwan, R.O.C*
10.1	**127**	**Degradation behaviour of electrical properties of inverted metamorphic four-junction (IMM4J) solar cells under 1 MeV electron irradiation** Zhang Yanqing, Wang Tianqi, Chaoming Liu, Ma Guoliang, Huo Mingxue and Qi Chunhua *Harbin Institute of Technology, China*
11.1	**116**	**Effect of Primary Kick-on Atoms on Conductivity Compensation in N-type 4H-SiC Irradiated by 1 MeV Electron, 25 MeV C Ions and 40 MeV Si Ions** Heyi Li, Chaoming Liu, Yanqing Zhang, Chunhua Qi, Yidan Wei, Tianqi Wang, Guoliang Ma, Shangli Dong and Mingxue Huo *Harbin Institute of Technology, China*
11.2	**280**	**Small Signal Microwave Characteristics and Optimization of δ-doped layer positioning in sub-micron InGaAs HEMT** Sharidya Rahman, Sharifah Fatmadiana Wan Muhamad Hatta, Norhayati Soin and Yasmin Abdul Wahab *University of Malaya, Malaysia*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
11.3	**292**	**Failure Analysis and Improvement of Superjunction MOSFET under UIS Stress Condition** Min Ren, Yining Ma, Shengrong Zhong, Wei Li, Songrong Wu, Zehong Li, Wei Gao and Bo Zhang *University of Electronic Science and Technology of China, China*
11.4	**297**	**Breakdown Voltage Impact on Lifetime of 1200V IGBT modules under H3TRB-HVDC testing** Haitao Deng, Jinlei Meng and Bo Wang *ABB, China*
11.5	**317**	**Comparative study of HVIGBTS(NPT,PT) under most soft switching conditions** Benbahouche Lynda and Boukadouma Salima *Ferhat Abbas Sétif University, Algeria*
11.6	**327**	**A Robust Dual Directional SCR without Current Saturation Effect for ESD Applications** Feibo Du, Xiaoyu Dong, Chengjin Yang, Yichen Xu, Zhiwei Liu, Jizhi Liu and Juin J. Liou *University of Electronic Science and Technology of China, China*
11.7	**286**	**Failure Analysis of the Effect of Hydrogen on GaAs Device** Chao Duan, Zhimin Ding, ZhaoXi Wu, Xiaoqing Wang, Chao Li and Xu Wang *China Aerospace Components Engineering Center, China*
11.8	**119**	**A single-event irradiation failure analysis test system for high speed digital-to-analog converter** Wei Yafeng, Li Jing and Yu Zhou *China Electronics Technology Group Corporation, China*
11.9	**198**	**Defect Density Reduction of Thin SiO2 MOSFET through Oxidation Pre-cleaning improvement – a Fast Wafer Level Reliability Monitoring** Mohd Hanif Kamaruddin, Norhayati Soin, Christopher Veriven, Chiao Mei How and Chung Keow Ang *Infineon Technologies, Malaysia*
11.10	**201**	**Electrical Performances and Physics Based Analysis of 650V E-mode GaN Devices at High Temperatures** Chi Zhang, Sheng Li, Siyang Liu, Jiaxing Wei, Wangran Wu and Weifeng Sun *Southeast University, China*
11.11	**202**	**Electrical Degradations of p-GaN HEMT under High Off-state Bias Stress with Negative Gate Voltage** Chi Zhang, Sheng Li, Siyang Liu, Jiaxing Wei, Wangran Wu and Weifeng Sun *Southeast University, China*
11.12	**213**	**A Novel Reverse Conducting SOI-LIGBT with Double Integrated NMOS for Enhanced Reverse Recovery** Ajiang Li, Shaohong Li, Long Zhang, Jing Zhu, Tian Tian, Yanqin Zou, Guichuang Zhu and Weifeng Sun *Southeast University, China*

Poster ID	Paper ID	Poster Session (Day 2, 12:00 - 14:00) Poster Session Chair: Nagarajan Raghavan, *SUTD, Singapore*
11.13	**250**	**Investigations on the Short-Circuit Degradation and its Mechanism of 1.2-KV 19-A SiC power MOSFETs** Jingliang Wang, Yiqiang Chen, Zhiyuan He, Yunfei En, Xinbing Xu, Yun Huang and Kuiwei Geng *South China University of Technology, China*
11.14	**269**	**Leakage Current Degradation in SiC Junction Barrier Schottky Diodes under Heavy Ion Microbeam** Shuang Cao, Qingkui Yu, Guanghua Du, Jinlong Guo, He Wang, Hongwei Zhang and Yi Sun *China Academy of Space Technology, China*
11.15	**274**	**Breakdown Mechanism of AlGaN/GaN-based HFET With Carbon-doped GaN Buffer Layer grown on Si substrate** Yiqiang Ni, Liuan Li, Liang He and Yang Liu *Electronics Research Institute of the Ministry of Industry and Information Technology, China*
12.1	**144**	**Irradiation Effects of 1 MeV Electron on Monolayer MoS2 Field Effect Transistors** Yanqing Zhang, Chunhua Qi, Xuesong Zheng, Zhengyong Hua, Jiaming Zhou, Heyi Li, Chaoming Liu, Yidan Wei, Tianqi Wang, Guoliang Ma, Shangli Dong and Mingxue Huo *Harbin Institute of Technology, China*
12.2	**170**	**Vertical SCR for ESD protection under 28nm PS Process** ZeKun Xu, Shu Rong Dong, Tao Hu, Wei Huang and Wei Guo *Zhejiang University, China*
12.3	**171**	**Improved LDMOS for ESD Protection of High Voltage BCD Process** Hong-yu Shen, Shu-rong Dong, Ze-kun Xu, Tao Hu, Wei Guo and Wei Huang *Zhejiang University, China*
12.4	**304**	**Non-conductive dielectric breakdown in multilayer h-BN stacks** Chao Wen, Xianhu Liang, Bin Yuan, Kaichen Zhu, Tao Wang, Tingting Han, Yiping Xiao, Xuehua Li and Mario Lanza *Soochow University, China*