IEEE Transactions on Quantum Engineering

Received 16 March 2023; revised 23 May 2023; accepted 17 June 2023; date of publication 26 June 2023; date of current version 4 August 2023.

Digital Object Identifier 10.1109/TQE.2023.3289257

Ultrathin TaN Damascene Nanowire Structures on 300-mm Si Wafers for Quantum Applications

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This work was supported by the Air Force Research Lab (AFRL), Rome, NY, under Grant FA8750-19-1-0031 and Grant FA864921P0773.

ABSTRACT We report on the development and characterization of superconducting damascene tantalum nitride (TaN) nanowires, 100 nm–3 μm wide, with TaN thicknesses varying from 5 to 35 nm, using 193-nm optical lithography and chemical mechanical planarization among other 300-mm wafer-scale processes. The TaN film composition chosen for nanowire fabrication was informed by a detailed study of unpatterned TaN films with varying nitrogen to tantalum ratios, formed by reactive sputtering. We also discuss the influence of encapsulation by copper and disordered atomic layer deposited TaN on the critical current of superconducting nanowires. Superconducting critical current density (measured at 12 mK) ranges from 0.12 to 0.85 MA/cm^2 depending on nanowire width and film thickness. The potential of ultrathin TaN nanowires at 300-mm scale is discussed in the context of applications such as on-chip integration for readout of superconducting qubits, in single-photon detection for quantum computing, as well as in large single-photon detecting focal plane arrays for cosmology in a broader range of wavelengths.

INDEX TERMS Damascene nanowires, quantum applications, superconducting nanowires, ultrathin tantalum nitride (TaN) films, 300 mm Si substrates.

I. INTRODUCTION

Tantalum nitride (TaN) is a material that has been used as a copper diffusion barrier in integrated circuits (ICs) [1], [2], [3], [4], along with many other applications ranging from corrosion-resistant coatings [5], [6] to superconducting quantum devices [7]. Superconducting nanowires are critical for applications in photonic quantum computing, single-photon detectors [9], [10], single-flux quantum (SFQ) logic circuits for qubit readout [11], neuromorphic computing [12], and in areas ranging from quantum cryptography to remote sensing [13]. TaN superconducting nanowire single-photon detectors (SNSPDs) have been shown to extend the detection bandwidth to longer wavelengths, along with higher detection efficiency [8], enabling, for example, new applications in cosmology when fabricated into large-scale arrays. TaN devices at 300-mm wafer scale can leverage the advances made by the semiconductor industry in process control, improving yield, pattern fidelity, and wafer-to-wafer predictability of performance [14]. Hence, the development of this process technology will enable scaling of quantum computing architectures, SFQ logic circuits, and SNSPD arrays.

Various studies on sputtered TaN films have shown the dependence of film properties on process parameters such as the ratio of N_2 and Ar flow rates [4], [15], [16], [17], [18], [21], sputtering power [19], and substrate temperature [20]. Breznay et al. [22] demonstrated disorder-induced superconductor-to-insulator transition (SIT) as a function of

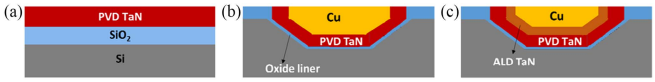

FIGURE 1. Schematic cross-sections of different types of film stack prepared for this work. (a) Blanket wafers with Si/50 nm SiO_2/PVD TaN for five different percentages of in-film nitrogen content. (b) Patterned wafer with damascene PVD TaN nanowires with Cu encapsulation. (c) Patterned wafer with damascene PVD TaN nanowires with an intervening layer of ALD TaN between PVD TaN and Cu.

nitrogen content and film thickness and a field-induced tunable SIT in superconducting TaN films. Detailed studies of the superconducting characteristics of TaN nanowires fabricated using 300-mm wafer processing tools are not widely available in the literature. In this study, the development of superconducting TaN films and copper-encapsulated TaN nanowires at 300-mm wafer scale is reported. TaN films are deposited by reactive sputtering of a pure Ta target in an N_2/Ar plasma. Patterning is done by 193-nm optical lithography, reactive ion etch, and chemical mechanical planarization (CMP) resulting in damascene nanowires [23] of varying geometries across the 300-mm wafer. Cu encapsulation can improve contact resistance during measurement and has other advantages to be described later. Damascene processing of TaN nanowires encapsulated with Cu leverages the considerable CMP process development of Cu interconnect by the complementary metal-oxide-semiconductor (CMOS) IC industry [24]. The first section of this article describes the characterization of unpatterned TaN films to understand film property variation as a function of deposition parameters. The next section describes the fabrication processes for patterned nanowires, followed by the room-temperature characterization of the nanowires. The current versus voltage (I–V) traces measured at mK temperatures as well as the superconducting critical current (I_c) versus temperature behavior are then discussed. The article ends with a discussion of future applications that are potentially enabled by this technology.

II. EXPERIMENTAL

Reactively sputtered ultrathin PVD TaN films were developed at 300-mm scale using a sputter-deposition chamber with a pure Ta target. Blanket TaN films were deposited at different partial pressures of nitrogen for characterization of properties such as stoichiometry, deposition rate, and resistivity, as shown in Fig. 1(a). Patterned structures of PVD TaN nanowires were fabricated with different encapsulations of Cu and atomic layer deposited (ALD) TaN, as shown in Fig. 1(b) and (c). The nanowires were encapsulated with Cu in most instances, in order to avoid oxidation of TaN upon exposure to ambient conditions. Cu encapsulation has implications for thermal conduction along the length of the superconducting nanowire. In contrast, adding an intervening layer of highly disordered metallic ALD TaN between the superconducting TaN and Cu ensures minimal leakage of Cooper pairs out of the superconducting PVD TaN [25]. We used ALD TaN films similar to that commonly used in the CMOS IC industry but substantially thicker (25 nm versus 1–3 nm) [26], [27].

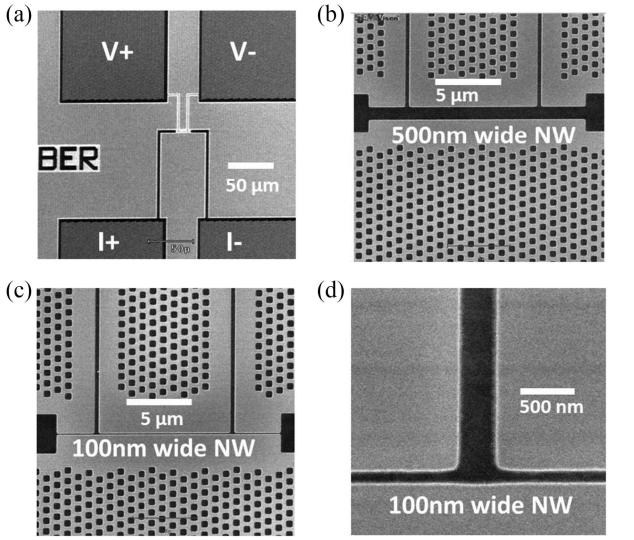

FIGURE 2. Top view SEM micrographs of Cu encapsulated TaN nanowires showing. (a) Four-probe measurement scheme, V+, V- are voltage contacts and I+, I- are current contacts. (b) 500-nm-wide nanowire. (c) 100-nm-wide nanowire. (d) Zoomed view of 100-nm-wide nanowire at the location where it is connected to the voltage measurement tap.

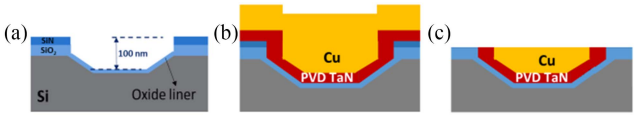

FIGURE 3. Steps in the fabrication scheme. (a) Schematic showing wafer cross-section after trench formation in Si/50 nm SiO_2/20 nm SiN and 10-nm oxide liner growth. (b) Schematic showing wafer cross-section after deposition of PVD TaN/Cu. (c) Schematic showing wafer cross-section after completion of CMP.

PVD TaN nanowires of varying thicknesses (5, 20, and 35 nm) and varying in-film nitrogen content were fabricated through control of the deposition times and nitrogen partial pressures during the deposition process. Each chip had multiple 10-μm-long PVD TaN nanowires, with widths ranging from 100 nm to 3 μm, designed to permit resistance and I_c measurements by a four-point-probe technique, as shown in Fig. 2(a). Fig. 2(b) and (c) shows the top-view of 500-nm-wide and 100-nm-wide nanowires. Fig. 2(d) is a scanning electron microscope (SEM) image at a higher magnification of a 100-nm-wide nanowire.

To fabricate damascene TaN structures, an SiO_2 (50 nm)/SiN (20 nm) bilayer was deposited on a silicon (100) substrate, followed by the formation of a trench using a sequence of 193-nm optical lithography, RIE, and anisotropic silicon etch using hydroxide-based chemistry. For some wafers, a 10-nm-thick thermal oxide liner was grown [as shown in Fig. 3(a)], to allow higher quality room-temperature leakage measurements. Then a PVD TaN (5–35 nm)/Cu (30 nm) bilayer film was deposited using a multichamber sputter deposition system. During TaN deposition, the nitrogen partial pressure is controlled to create films with N/Ta ratios that vary from 0.35 to 0.7. Then a 450-nm-thick Cu was electrodeposited to fill the

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trenches and cover the field areas around the trenches, as shown in Fig. 3(b). The wafer was then processed through a CMP process. The CMP process leverages knowledge accumulated by the IC industry since early 2000s—where connections between transistors are made with damascene Cu wires in an insulating silicon oxide matrix, with TaN as the copper diffusion barrier that separates Cu from the oxide. Hence, the CMP process for removing Cu and TaN on the field and removing controllable amounts of the dielectric in the field area is well known [27], [28], [29]. Appropriate polish pressures and times have to be tuned for the specific tool and consumable set being utilized and to account for the thicknesses of the prepolish metal stack and its variation across the wafer diameter. The resultant structure, after the completion of CMP, is shown in the schematic of Fig. 3(c).

Some of the many chips diced from the four wafers processed with different thicknesses, as well as those with an ALD TaN "intervening layer" of 25 nm, were mounted for testing on a printed circuit board (PCB) interfaced through cryogenic QDevil low-pass filters to a Keithley 2602A source-measure unit. The PCB carrying the chip under test was cryogenically cooled in a dilution fridge at the Innovare Advancement Center, Rome, NY, with a base temperature of 10 mK.

III. RESULTS AND DISCUSSION

A. PVD TAN BLANKET FILM CHARACTERIZATION

The blanket PVD TaN wafers were analyzed by a variety of techniques to characterize film properties. Fig. 4 shows how the nitrogen content of the TaN thin film was characterized by sputter-profiling X-ray photoelectron spectroscopy (XPS). The signal from the "bulk" region of the thin film (away from top and bottom interfaces) was averaged to establish the in-film N/Ta ratio, as shown in Fig. 4(a). It should be noted that the oxygen content reported by XPS in the bulk of the TaN film is likely due to characterization technique artifacts (sputter mixing from the surface and background subtraction effects). The PVD process does not permit such oxygen incorporation deep inside the film. Secondary ion mass spectroscopy (SIMS) analysis of these PVD films [see Fig. 4(b)] confirms that the (red) oxygen signal diminishes by several orders of magnitude to a noise level after the 2 nm of depth from the surface (first 20 s of sputtering by the cesium beam). Fig. 4(c) shows how the in-film N/Ta ratio is determined by the N_2 fraction in the N_2/Ar gas mixture that forms the plasma used during reactive sputtering of the Ta target.

X-ray diffraction (XRD) spectra of the various PVD TaN films are shown in Fig. 5 for in-plane and out-of-plane configurations. It was established that the film with N/Ta = 0.35 exhibits an *fcc* crystal structure with a lattice constant of 0.43 nm.

For films with higher N/Ta ratio, there is a clear shift in the XRD spectra. Sputtered TaN is known to form multiple equilibrium and metastable phases along with their mixtures as a

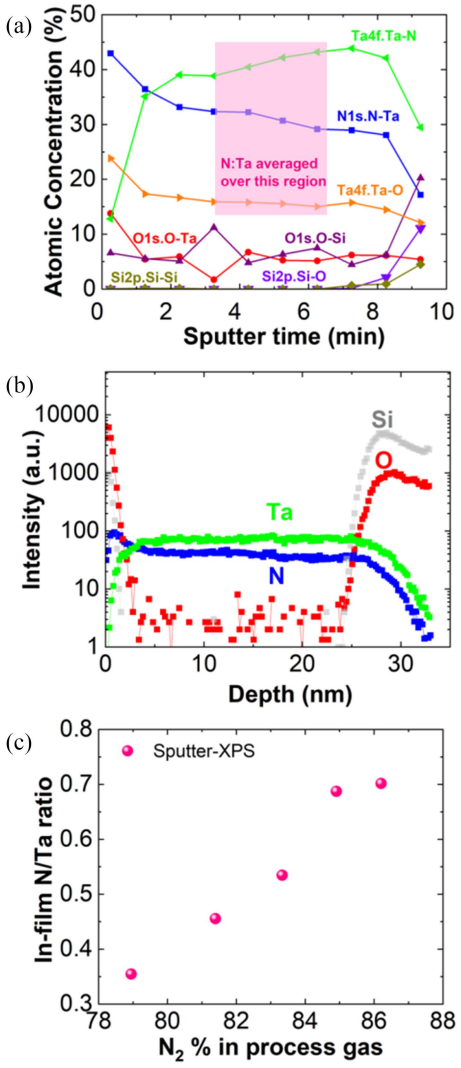

FIGURE 4. (a) Example of sputter-profiled XPS analysis of PVD TaN. The traces are labeled by the element and its core shell (1s, 2p, and 4f) that generated the X-ray photoelectron; the label also includes its bonding configuration, e.g., TaN indicates Ta bonded to nitrogen. (b) Example of SIMS analysis. (c) Correlating in-film N/Ta ratio to process conditions.

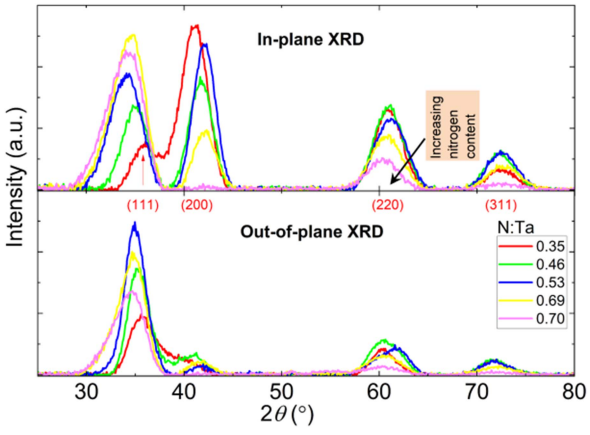

FIGURE 5. XRD spectra for the PVD TaN films with varying N/Ta ratios.

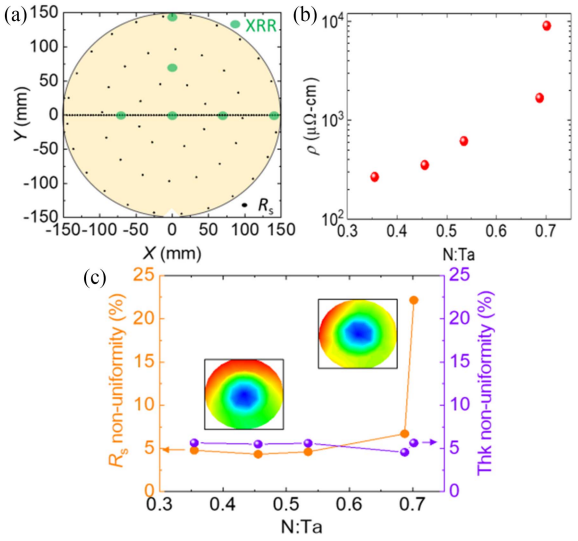

FIGURE 6. (a) Wafer map showing R_s measurement sites as black dots (49 polar map and 81 diameter scan) and XRR sites (green dots). (b) Resistivity at wafer center versus in-film N/Ta ratio for blanket TaN films without Cu. (c) Nonuniformity of the PVD TaN films as a function of N/Ta ratio; the contour maps that are inset are intended to show the azimuthal variation of R_s, with color scale of each map extending from maximum (red) to minimum values (blue).

function of deposition conditions [30]. We have confirmed that the spectra for higher N/Ta ratios cannot be explained by a mixture of *fcc* and *bcc* phases. However, invoking a body-centered tetragonal with a = 0.432 nm and c = 0.52 nm permits all the XRD peaks of the higher nitrogen content samples to be fitted (the reflections are 002, 200, 220, and 222, in increasing 2θ order). The maximum residual is 1%, which could be attributed to in-film stress.

Fig. 6(a) shows the locations on the wafer where X-ray reflectometry (XRR) and four-point probe measurements of sheet resistance (R_s) have been performed at room temperature. At the wafer center, both datasets are obtained at the same point permitting the calculation of resistivity of the PVD TaN film (as the product of R_s and thickness). The dependence of PVD TaN resistivity as a function of the in-film N/Ta ratio is shown in Fig. 6(b). The start of the sigmoidal transition to the insulating state can be observed in this figure (note that the *y*-axis is logarithmic).

In Fig. 6(c), the within-wafer nonuniformity (NU) (standard deviation, expressed as a % of the mean value) of thickness and R_s is shown as a function of N/Ta ratio. The thickness NU was calculated from six points of XRR data. R_s NU is determined from 49 points distributed across the wafer (center point, 49, 98, and 145 mm radius) and from 81 points along the diameter, as shown by black dots in Fig. 6(a). It can be seen that the thickness uniformity stays stable at $\sim$ 5.5% for all conditions tested. The R_s NU is likewise low for most conditions, shooting up only for the highest N/Ta ratio tested. At the highest N/Ta ratio, the high NU in R_s is driven by compositional difference from wafer center to edge. The contour maps that are inset in Fig. 6(c), indicate the R_s variation is primarily radial with an azimuthal variation near the wafer edge that is dependent on the gas flow dynamics in the chamber.

TABLE 1 Description of Five Blanket Wafers Prepared for Room-Temperature Characterizations

TaN thickness (nm)	N/Ta ratio	ρ (μΩ-cm)	Dep rate (nm/s)	Thk NU (%)	R_s NU (%)
21.88	0.35	267.0	0.73	5.6	4.8
21.76	0.46	352.1	0.73	5.5	4.3
21.55	0.53	615.0	0.72	5.6	4.6
20.16	0.69	1683.6	0.67	4.6	6.7
17.94	0.7	9045.2	0.60	5.6	22.1

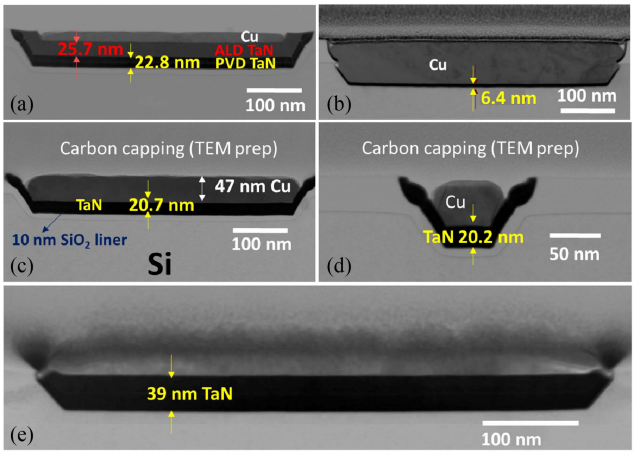

FIGURE 7. TEM cross-sections of (a) 20 nm (nominal) thick PVD TaN nanowire (500 nm wide) with intervening ALD TaN between PVD TaN and Cu. (b) Five nanometer (nominal) thick PVD TaN nanowire (500 nm wide). (c) Twenty nanometer (nominal) thick PVD TaN nanowires – 500 nm wide and (d) 100 nm wide. (e) Thirty-five-nanometer (nominal) PVD TaN nanowire – 500 nm wide.

Table 1 summarizes all the measured properties of PVD TaN blanket films at room temperature. The TaN thickness reported in column 1 is determined from transmission electron microscopy (TEM) and the N/Ta ratios in column 2 are calculated from sputter-profiled XPS, as described above. The last two columns present the NU of thickness and R_s, respectively.

B. PVD TAN PATTERNED FILM CHARACTERIZATION

From the studies of resistivity and phase variation with N/Ta ratio, we chose a fixed value of N/Ta of 0.53 (below the onset of metal to insulator transition) to study the superconducting characteristics of different thicknesses of PVD TaN nanowires and for different encapsulation.

Fig. 7 shows the cross-sectional TEM images, for 500-nm-wide nanowires of varying PVD TaN thickness (nominally 5, 20, and 35 nm) and PVD TaN with intervening ALD TaN along with an image of a 100-nm-wide nanowire at 20-nm PVD TaN thickness. The thickness of the Cu encapsulating the PVD TaN can also be seen to be decreasing as the PVD TaN thickness increases. This is a consequence of the CMP process utilized to create the damascene nanowires.

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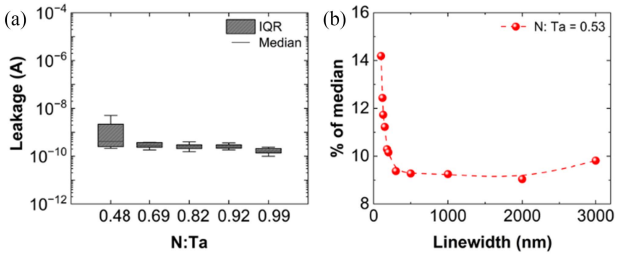

FIGURE 8. Electrical tests at room temperature showing (a) leakage between adjacent nanowires for different N/Ta ratios, presented as a box-and-whisker chart (where the box indicates the inner quartile range (IQR) and the whiskers indicate 1.5 times the IQR. (b) Within-wafer NU of R_s for all copper encapsulated TaN nanowire linewidths at N/Ta = 0.53.

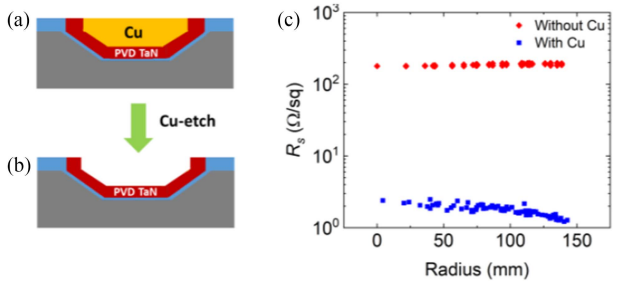

FIGURE 9. Schematic cross-sections of nanowire. (a) After CMP. (b) After Cu etching. (c) Across wafer R_s of PVD TaN nanowire (35 nm thick nomi nally) with and without Cu encapsulation for a 120-nm-wide nanowire.

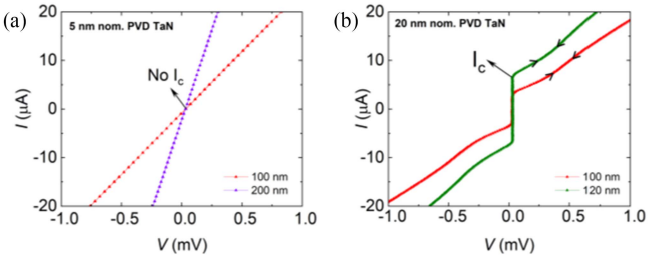

FIGURE 10. (a) No superconductivity at 12 mK for 5 nm (nominal) thick PVD TaN encapsulated by Cu. (b) Superconducting behavior with clear critical current I_c (defined as the current at which PVD TaN switches from superconducting state to normal state, indicated by the arrow) measured at 12 mK for 20 nm (nominal) thick PVD TaN nanowires encapsulated by Cu.

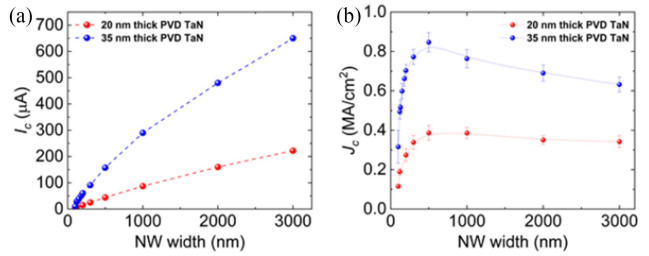

FIGURE 11. (a) Critical current at 12 mK versus nanowire width for Cu encapsulated PVD TaN films of two thicknesses, both having N/Ta=0.53. (b) Computed J_c(12 mK) of PVD TaN nanowires, using TEM-based area estimation and I_c(12 mK).

Fig. 8 shows the results of electrical tests from 26 sites distributed across the wafer surface to confirm the leakage between adjacent 105 μm long nanowires (spaced by 1 μm) with different N/Ta ratios. The room-temperature leakage values were in the range of nA for all devices, as shown in Fig. 8(a). It should be noted that room-temperature leakage mechanisms are "frozen out" at cryogenic temperatures, and hence serve mainly to confirm that adjacent nanowires are not shorted together by metal residues in the field after CMP is completed.

Fig. 8(b) shows the within-wafer NU of R_s for all the nanowire widths (for N/Ta value of 0.53). It should be noted that the resistance of the copper-encapsulated TaN nanowires is dominated by copper—since it has two orders of magnitude lower resistivity than TaN. Hence, the resistance and resistance NU measurements at room temperature are best interpreted as indicative of linewidth and its NU across the wafer. NU in resistance decreases steadily from ~14% as the linewidth increases to 300 nm, settling at values of ~9–10% for wider lines.

Because the R_s measurements shown in Fig. 8 were Cu-dominated, in order to measure the resistance of the 35 nm TaN itself, copper was etched off the wafer with dilute sulfuric acid in a single-wafer 300-mm wafer etching tool. The line resistance was measured again for 120 nm wide nanowires, with the results shown in Fig. 9(c). The resultant TaN R_s within-wafer NU obtained is better than 5%. This suggests an equivalently good spread of nanowire I_c across the wafer.

C. PVD TAN NANOWIRE CRYOGENIC CHARACTERIZATION

After confirming good leakage and R_s characteristics at room temperature, the wafers with PVD TaN/Cu nanowires (with N/Ta = 0.53) were diced into chips and packaged for measurement at millikelvin temperatures in a dilution fridge. Fig. 10(a) shows the lack of superconducting behavior for the nominally 5 nm (6.4 nm by TEM) PVD TaN nanowires. In contrast, Fig. 10(b) shows that a 20-nm PVD TaN film exhibits clear superconducting behavior. The lack of superconductivity in the 6.4-nm thin TaN is possibly driven by the reverse proximity effect of nearby copper. The diffusion of a large number of quasi-particles from Cu into the 6.4-nm film, as well as the out-diffusion of Cooper-pairs and subsequent decay into electrons in the normal metal, possibly explains the suppression of superconductivity in this thin film.

In Fig. 11(a), the I_c(12 mK) measured on nanowires with 20- and 35-nm nominal thicknesses are shown as a function of the nanowire width. The cross-sectional area of the PVD TaN nanowire was extracted from TEM images using the open-source image analysis software, ImageJ [31]. This information was then used to compute the critical current density (J_c) of the nanowires. This is shown in Fig. 11(b). It can be seen that the J_c(12 mK) of the 20- and 35-nm-thick PVD TaN nanowires first increases with line width, reaches a maximum value (0.85 MA/cm [2] for 35-nm thickness and 0.39 MA/cm [2] for 20-nm-thick nanowires) at 500-nm width and then decreases with further increase in nanowire width. This behavior, with a maximum in J_c(w) curve, has been

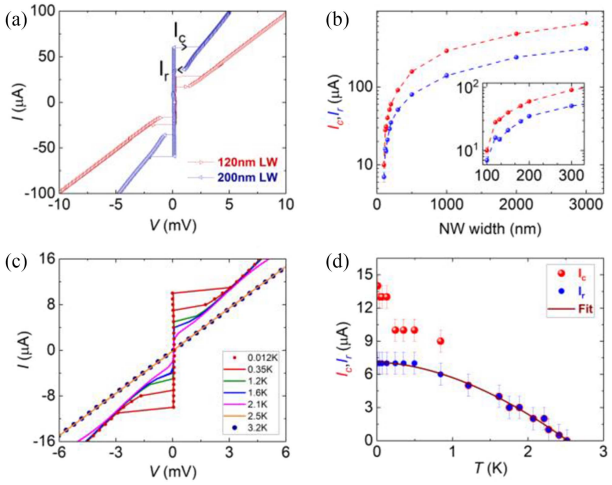

FIGURE 12. Cryogenic data for Cu encapsulated 35 nm (nominal) thick PVD TaN nanowires (N/Ta = 0.53). (a) *I–V* traces showing hysteretic behavior at 12 mK. (b) I_c, I_r (at 12 mK) on log scale as a function of nanowire width where the inset shows the zoomed-in view at smaller linewidths. (c) *I–V* traces at different temperatures showing T_c of 2.5 K for a nanowire width of 100 nm. (d) I_c, I_r as a function of temperature, I_r (T) is fitted with a variant of SBT model for a nanowire width of 100 nm.

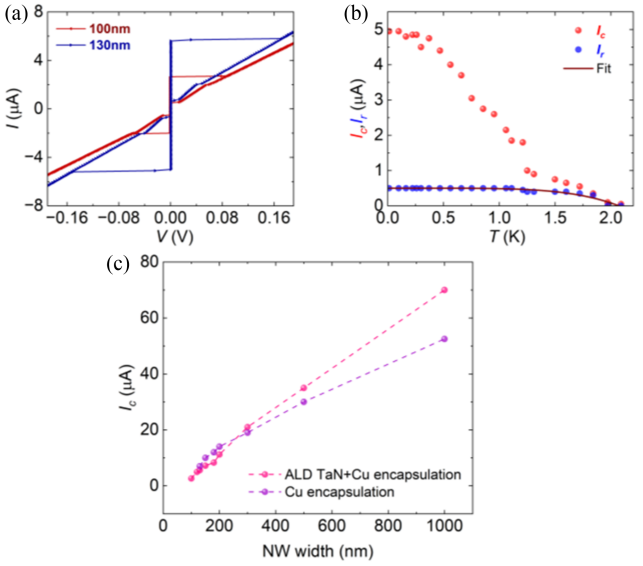

FIGURE 13. Cryogenic measurements of 20 nm (nominal) thick PVD TaN (N/Ta = 0.53) nanowires with ALD TaN+Cu encapsulation. (a) *I–V* traces showing hysteretic behavior. (b) I_c, I_r as a function of temperature for a nanowire width of 100 nm, error bars are smaller than the size of the dot for each measurement point, I_r (T) is fitted with a variant of SBT model resulting in exponent n value of 5. (c) Comparison of I_c(w) for 20 nm thick PVD TaN nanowire for different encapsulations for nanowire widths varying from 100 to 1000 nm.

observed on NbN and TaN nanowires [32], [33], where the nonmonotonic behavior is attributed to the competition between various phenomena. For nanowires narrower than 500 nm, the effective cross section associated with superconducting current transport decreases faster than the decrease in width due to the greater fraction occupied by the normal regions near the edges. For the nanowires wider than 500 nm, the decrease in measured current density could arise from penetration and movement of self-generated vortices. However, further theoretical and experimental analyses are required to be definitive.

Measurement of the *I–V* traces at millikelvin temperatures for 35 nm (nominal) nanowires showed hysteresis, with consistent and repeatable values for switching and retrapping currents, as indicated in Fig. 12(a). The critical current I_c refers to the current at which it switches from superconducting to normal state, while the retrapping current I_r is the current at which it switches from normal state to superconducting state on the return path of current, as shown by arrows in Fig. 12(a). As mentioned in TEM cross sections of Fig. 7, as the PVD TaN thickness increases, the Cu thickness decreases in a linear fashion. This translates directly into the ability of the Cu layer to transport heat away. This can explain the observation of hysteresis in 35-nm-thick nanowires [see Fig. 12(a)] with distinctly different values for the I_c(12 mK), I_r(12 mK), and no hysteresis in 20-nm thick nanowires [see Fig. 10(b)]. In Fig. 12(b), I_c(12 mK) and I_r(12 mK) plotted on a log scale show a near-constant separation over various linewidths from 120 to 3000 nm, indicating that I_c(12 mK)/I_r(12 mK) is ∼1.9 (±10%). The decrease in this ratio for the 100-nm line remains to be understood.

Fig. 12(c) shows the measured *I–V* traces during warm-up with a clear identification of superconducting transition. While the temperature at which *I–V* becomes linear and nanowire turns to resistive state is observed to be 2.5 K for the 35-nm-thick nanowire, we note that an accurate determination of T_c in a dilution fridge is fraught, due to thermal lag between the sample and the temperature sensor. The I_r was also measured during warm-up using the same methodology. The results are shown in Fig. 12(d). The large regions with little data are due to the 1-μ-A step-size used, but the overall dependence of the I_c and I_r on temperature is quite clear. It is interesting to note that the behavior for PVD TaN nanowires shown in Fig. 12(d) largely mimics the observations made by Dane et al. [34] on NbN superconducting nanowires, showing features consistent with a variant of the Skocpol–Beasley–Tinkham (SBT) model which has been used to model hot-spots in superconducting nanowires [35].

The data in Fig. 12(d) is fitted with the following heat balance equation [34]:

$$\beta w^2 \left(T_{hs}^n - T_b^n\right) = I_{hs}^2 R_n \tag{1}$$

where β is a generic thermal boundary conductance with units of W/m^{2}K^n, T_b is the bath or substrate temperature, T_{hs} is the hot-spot temperature, w is the width of the wire, I_{hs} is the hot-spot current or retrapping current I_r. As per the previous reports [34], [35], the value of exponent "n" is intended to capture the relevant physics associated with the system. For the fitting of I_r(T) shown in Fig. 12(d), β/R_n, T_{hs}, and n are taken as free parameters which gives the best-fit value of n to be 1.76. The difference between this value of n and that reported for NbN strips [34] is discussed later in the text. Fig. 13(a) shows the effect of encapsulation where an

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intervening layer of metallic ALD TaN is present between the superconducting TaN and Cu. A large hysteresis between the I_c(12 mK) and I_r(12 mK) is observed, as shown in Fig. 13(a). This large hysteresis can be explained by the fact that the hot spots in PVD TaN are not in direct contact with Cu. In contrast, for the case shown earlier in Fig. 10(b), copper is in direct contact with PVD TaN, and hence acts as an effective heat sink, resulting in nonhysteretic behavior in *I–V* curves [36]. Fig. 13(b) shows the critical current, I_c and I_r extracted from the measured *I–V* traces at different temperatures during warm-up for the 20-nm-thick and 100-nm-wide nanowire with ALD TaN+Cu encapsulation.

Fig. 13(c) shows the I_c(12 mK) comparison of 20-nm-thick PVD TaN with different encapsulations. I_c(12 mK) is higher for the case with ALD TaN+Cu encapsulation for higher linewidths which can be explained by the blocking of Cooper pair transport at PVD TaN/Cu interface and hence the reduced reverse proximity effect. The small, residual, differences in I_c(12 mK) for lower linewidths could be due to measurement noise [36]. It is to be noted that the Cu-encapsulated 20-nm PVD TaN chip shown in Fig. 13 was fabricated in a separate run from the chips shown in Fig. 11. These measurements on PVD TaN with varying heat-sinks are at variance with a recent report [34] on NbN nanowires with different substrates (to modify heat sink capabilities), since the I_c, I_r dependence does not fit a common value of their exponent (n) for the data shown in Figs. 12(d) and 13(b), as their data does. The fit to the nonlinear SBT model gives a value of exponent n as 5 if n is kept as a free-fitting parameter (equation 0.1) in Fig. 13(b). Further, theoretical modeling and measurements are needed to understand the difference in the exponent n value for different encapsulations (shunt resistances) of PVD TaN nanowires [36].

IV. SUMMARY AND CONCLUSION

In conclusion, we demonstrate encapsulated damascene TaN superconducting nanowires for the first time on 300-mm scale. Better than 6% within-wafer uniformity of R_s and thickness of PVD TaN is demonstrated. Onset of metal-to-insulator transition is observed as nitrogen content is increased. TaN nanowires (N/Ta = 0.53) show I_c(12 mK) values in the range 3–650 μA for nanowire widths ranging from 100 to 3000 nm and for PVD TaN thickness range from 20 to 35 nm. The maximum J_c(12 mK) of 0.39 MA/cm [2] and 0.85 MA/cm [2] was observed on Cu-encapsulated 500 nm wide nanowires that were 20 and 35 nm thick, respectively. Reproducible observations of hysteresis in 35 nm TaN nanowire have aspects consistent with predictions of a variant of the SBT model. We demonstrate the effect of nanowire width, thickness, and encapsulation on the superconducting properties (J_c(12 mK), I_c(12 mK)) of the PVD TaN nanowires. These observations suggest that PVD TaN superconducting nanowires can be utilized for applications in superconducting optoelectronic neuromorphic computing as well as super-inductors in quantum computing circuits.

The lower T_c of PVD TaN is advantageous for SNSPD applications as it is easier to break the Cooper pairs, increasing detection bandwidth to longer wavelengths. Knowledge of the critical current of TaN nanowires and its variability, obtained by this study will be important for designing large arrays of SNSPDs at 300-mm wafer scale, for use in cosmology. Room temperature measurements of nanowire resistance indicate better than 5% standard deviation across the 300-mm wafer, which suggests a similar spread in critical currents. In this application, since the incident photon arrives perpendicular to the chip surface, it will be necessary to remove the copper—which is a topic of an ongoing study. While the smallest linewidth demonstrated in this work is 100 nm, the use of 193-nm optical lithography enables smaller dimensions to be fabricated just as readily, increasing the optical detection bandwidth to even longer wavelengths are useful for cosmology.

The incorporation of copper in thermal contact with the superconducting nanowire has been shown to help with thermalization of hot-spots, as indicated by the lack of hysteresis for the 20-nm PVD TaN nanowires encapsulated by copper. The thickness of the Cu in the damascene nanowire would need to be carefully optimized to allow for faster reset times while still allowing the hot-spot to be formed under illumination. Such an optimized nanowire could improve the speed of photon detection in waveguide-integrated single photon detectors by decreasing the reset time. If the area consumed by a shunt resistor can be eliminated by a suitable choice of the copper thickness, the footprint of the SNSPD may also be smaller. Additionally, future studies of the kinetic inductance of well-controlled TaN nanowires fabricated across a 300-mm wafer will enable simple, space-efficient super-inductors to be designed and employed in SFQ. Use of TaN super-inductors in SFQ circuits offers the possibility that interconnects are not relied upon to provide required inductances, but are used to connect small-area kinetic inductances, and Josephson junctions.

ACKNOWLEDGMENT

The authors gratefully acknowledge the help provided by Matthew Bracken of NY CREATES for cross-sectional analyses by scanning electron microscopy. The authors also gratefully acknowledge the work of Andrew Brownell and Nick Barton in packaging the devices used in this article. Approved for Public Release; Distribution Unlimited (PA# AFRL-2023-2489). Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of Air Force Research Laboratory.

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