Multibit Full Comparator Logic in Quantum-Dot Cellular Automata

S. Perri, *Senior Member, IEEE*, F. Spagnolo, *Member, IEEE*, F. Frustaci, *Senior Member, IEEE*, and P. Corsonello, *Member, IEEE*

***Abstract*—In the last few years, binary comparators have received a great deal of attention as parts of complex computational data-paths. However, while several multi-bit architectures have been demonstrated using conventional CMOS technologies, few examples of n-bit comparators, with n higher than 4, can be found in literature for designs based on emerging nanotechnologies, such as the Quantum Dot Cellular Automata, the Nano Magnetic Logic, and many others. This brief proposes a novel approach to design efficient multi-bit binary comparators using the Quantum Dot Cellular Automata nanotechnology. The approach here presented allows improving state-of-the-art competitors in terms of computational complexity and average energy consumption. As an example, in comparison with its direct counterparts, the 32-bit comparator designed as proposed here saves up to 26%, 23% and 11% of the occupied area, the used basic cells and the average energy consumption, respectively. When implemented using the Nano Magnetic Logic, the 4-bit version of the novel comparator uses 1183 magnets and 38 clock phases.**

***Index Terms*—Binary comparators, majority gates, quantum dot cellular automata (QCA).**

I. Introduction

SEVERAL emerging nanotechnologies, such as the Quantum dot Cellular Automata (QCA) [1], the Nano Magnetic Logic (NML) [2], the carbon nanotube [3], etc., are recognized as promising solutions to overcome the limits of conventional CMOS technology. In the recent past, QCA-based binary arithmetic circuits, including adders, multipliers and comparators received a great deal of attention [4]–[19]. However, among them, parallel binary comparators realized in such emerging technologies still represents a challenge. They are basic computational modules extensively used in many digital circuits and systems applications. Unfortunately, while their realization using the traditional CMOS approach is relatively straightforward, designing efficient parallel comparators using QCA or NML poses several practical difficulties. This is mainly because the same basic nanostructure, for instance the QCA cell [1], is used for both logic gates and wires, and the fundamental logic elements inherently available in such technologies are limited. In particular, QCA logic circuits rely only on Majority Gates (MGs) and Inverters (INVs) as elementary building blocks. For these reasons, conventional logic and architecture designs suitable for the CMOS world are mostly inefficient when adopted in such nanotechnologies, thus making completely new designs necessary. Furthermore, logic and physical designs of QCA-based circuits are much more strictly related. This implies that traditional approaches based on the replica of elementary building blocks for multi-bit circuits cannot be easily exploited in such emerging environments.

This brief presents a novel and easy-to-use approach suitable for the design of efficient QCA-ased multi-bit parallel comparators. A novel logic formulation is introduced to reduce the complexity and the energy consumption of tree-based comparator architectures constituted by replicas of two very simple encoding sub-circuits, responsible for comparing 2-bit subwords of the operands, and a third module furnishing the final comparison result. The high regularity achieved in this way allows partitioning the cells used into proper clock zones in a simpler way.

All the designs here presented were laid out and characterized using the QCA Designer-E 2.2 software tool. Post-layout results show that the 32-bit version of the novel comparator complying with the 2DDWave clocking scheme [20] requires 2587 cells, occupies an overall area of ∼5.9um^2, uses 18 clock phases to perform the generic operation and dissipates an average energy of ∼8.02e-2 eV. At a parity of the adopted basic clocking scheme, it achieves a complexity (i.e., the number of used MGs) and an average energy consumption ∼22% and ∼11% lower than [14], respectively.

The proposed methodology has been also applied to realize a 4-bit NML-based comparator. Results obtained with the ToPoliNano CAD Tool show that the proposed NML-based comparator requires 1183 magnets and uses 38 clock phases.

The rest of this brief is organized as follows: Section II provides a brief background; the novel comparator logic is introduced in Section III; then, Section IV presents post-layout results and comparisons with existing counterparts; finally, conclusions are drawn in Section V.

II. Background

With its four quantum dots and two free electrons, the generic QCA basic cell can assume only two possible

Manuscript received 3 March 2022; revised 24 June 2022; accepted 20 July 2022. Date of publication 25 July 2022; date of current version 28 October 2022. The work of F. Spagnolo was supported by the PON Ricerca & Innovazione—Ministero dell'Università e della Ricerca under Grant 1062_R24_INNOVAZIONE. This brief was recommended by Associate Editor P. Girard. *(Corresponding author: P. Corsonello.)*

S. Perri is with the Department of Mechanical, Energy and Management Engineering, University of Calabria, 87036 Rende, Italy (e-mail: s.perri@unical.it).

F. Spagnolo, F. Frustaci, and P. Corsonello are with the Department of Informatics, Modeling, Electronics and Systems Engineering, University of Calabria, 87036 Rende, Italy (e-mail: f.spagnolo@dimes.unical.it; f.frustaci@dimes.unical.it; p.corsonello@unical.it).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2022.3193561.

Digital Object Identifier 10.1109/TCSII.2022.3193561

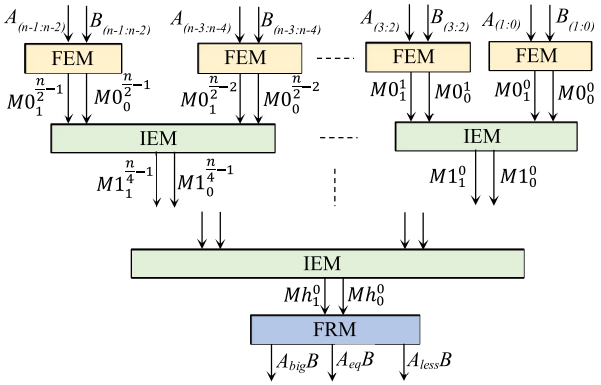

Fig. 1. The top-level architecture of the novel n-bit full comparator.

polarizations that are associated to the bit values '0' and '1' [1]. Properly combining multiple instances of the basic cell, the fundamental logic elements, i.e., MGs, INVs and wires, are obtained. More complex logic functions are implemented by exploiting the interaction between adjacent QCA cells and employing either the co-planar or the multilayer routing strategy [1].

In order to guarantee the correct data-flow directionality, the cells within a QCA-based design are partitioned into the so-called clock zones, each associated to a proper clock signal. Each clock zone in the computational path behaves like a D-latch, thus making such a design intrinsically pipelined, with a latency depending on the number of cascaded clock zones.

In the last few years, efficient QCA implementations have been proposed for several binary arithmetic functions, with a special effort focused on the comparators [7]–[20].

The designs proposed in [7], [8], [10], [13], [16]–[18] can compare just 1-bit inputs. Some of them are able to simply establish if the inputs a and b are equal [7], whereas others can establish if $a < b$ or $a > b$ [10]. Finally, other designs operate as full comparators, thus recognizing separately, i.e., through three different output signals, whether $a = b$, $a < b$ or $a > b$ [8], [13], [16]–[19].

Representative examples of n-bit comparators are described in [9], [11], [12], [14], [15], [19]. The serial structure provided in [9] exploits one 1-bit comparator and two 1-bit registers to process the n bits of the operands $A_{(n-1:0)}$ and $B_{(n-1:0)}$ serially. As its main advantage, this full comparator limits the amount of utilized resources, but at the expense of an equally limited throughput. The solution presented in [11] leads to a faster implementation, but it recognizes only the condition $A \geq B$.

All the approaches proposed in [12], [14], [15], [19] allow designing n-bit parallel full comparators. However, while the tree-based (TB) architecture presented in [12] was demonstrated for n up to 8, the two different architectures introduced in [14], namely the low-cost cascade-based (CB) and the fast TB comparators, where characterized for n ranging between 2 and 32.

The full comparator recently presented in [15], was designed by exploiting a novel 5-input MG and it was characterized considering operands word-lengths up to 4-bit. Finally, [19] presents pre-layout results for a comparator

$A_{(2i+1:2i)}$	$B_{(2i+1:2i)}$	$M0_1^i$	$M0_0^i$	Condition
0 0	0 0	1	0	$A=B$
0 0	0 1	0	0	$A<B$
0 0	1 0	0	0	$A<B$
0 0	1 1	0	0	$A<B$
0 1	0 0	1	1	$A>B$
0 1	0 1	0	1	$A=B$
0 1	1 0	0	0	$A<B$
0 1	1 1	0	0	$A<B$
1 0	0 0	1	1	$A>B$
1 0	0 1	1	1	$A>B$
1 0	1 0	1	0	$A=B$
1 0	1 1	0	0	$A<B$
1 1	0 0	1	1	$A>B$
1 1	0 1	1	1	$A>B$
1 1	1 0	1	1	$A>B$
1 1	1 1	0	1	$A=B$

(a)

Mk_1^{2x+1}	Mk_0^{2x+1}	Mk_1^{2x}	Mk_0^{2x}	Mj_1^x	Mj_0^x	Condition
0	0	0	0	0	0	$A<B$
0	0	0	1	0	0	$A<B$
0	0	1	0	0	0	$A<B$
0	0	1	1	0	0	$A<B$
0	1	0	0	0	0	$A<B$
0	1	0	1	0	1	$A=B$
0	1	1	0	1	0	$A=B$
0	1	1	1	1	1	$A>B$
1	0	0	0	0	0	$A<B$
1	0	0	1	0	1	$A=B$
1	0	1	0	1	0	$A=B$
1	0	1	1	1	1	$A>B$
1	1	0	0	1	1	$A>B$
1	1	0	1	1	1	$A>B$
1	1	1	0	1	1	$A>B$
1	1	1	1	1	1	$A>B$

(b)

Fig. 2. The encoding logic implemented within: (a) the FEM; (b) the IEM.

structure that allows reducing the amount of MGs used by both the CB and TB architectures proposed in [14].

III. The Novel n-Bit QCA-Based Full Comparator

As depicted in Fig. 1, the novel parallel full comparator exploits a TB architecture. It splits the operands $A_{(n-1:0)}$ and $B_{(n-1:0)}$ into $\frac{n}{2}$ 2-bit sub-words, which are processed by as many instances of the First Encoding Module (FEM). The i-th FEM, with $i = 0, \ldots, \frac{n}{2}-1$, receives $A_{(2i+1:2i)}$ and $B_{(2i+1:2i)}$ as inputs and, as summarized in Fig. 2a, it encodes the occurring condition, among $A > B$, $A = B$ and $A < B$, by means of the signals $M0_1^i$ and $M0_0^i$ defined in (1). When $A_{(n-1:0)}$ and $B_{(n-1:0)}$ are unsigned numbers, all the FEMs apply the encoding logic reported in Fig. 2a and (1a)-(1b).

$$M0_1^i = MG\left(A_{(2i+1)},\ \overline{B}_{(2i+1)},\ \overline{B}_{(2i)}\right) \quad (1a)$$

$$M0_0^i = MG\left(A_{(2i+1)},\ \overline{B}_{(2i+1)}, A_{(2i)}\right) \quad (1b)$$

$$M0_1^{\frac{n}{2}-1} = MG\left(\overline{A}_{(2i+1)}, B_{(2i+1)}\ , \overline{B}_{(2i)}\ \right) \quad (1c)$$

$$M0_0^{\frac{n}{2}-1} = MG\left(\overline{A}_{(2i+1)}, B_{(2i+1)}\ , A_{(2i)}\right) \quad (1d)$$

On the contrary, when $A_{(n-1:0)}$ and $B_{(n-1:0)}$ are 2's complement numbers, the signals $M0_1^{\frac{n}{2}-1}$ and $M0_0^{\frac{n}{2}-1}$, related to the most significant bits of the operands, are computed by (1c)-(1d).

The outputs produced by the FEMs are then merged through $h = \log_2 \frac{n}{2}$ levels of Intermediate Encoding Modules (IEMs). The j-th level, with $j = 1, \ldots, h$, consists of $y =$

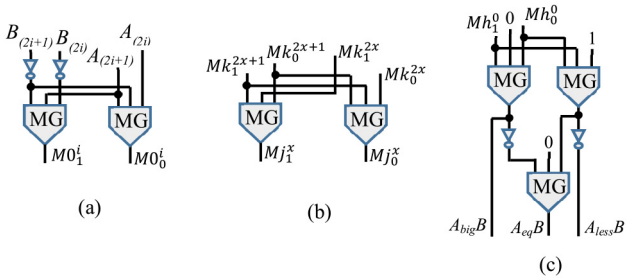

Fig. 3. The circuit architecture of: (a) the FEM; (b) the IEM; (c) the FRM.

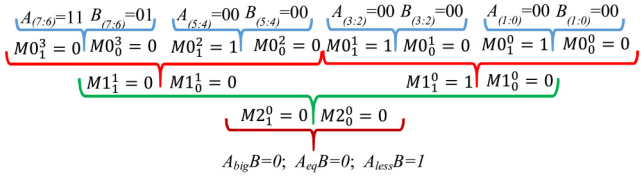

Fig. 4. An example of computation.

$\log_2\left[\frac{n}{2} - 2 \times (j-1)\right]$ IEMs, each responsible for encoding the comparison condition occurring on (2^{j+1})-bit sub-words of the operands, as reported in Fig. 2b. The signals Mj_1^x and Mj_0^x, with $x = 0, \ldots, y-1$, are furnished by the x-th IEM within the j-th level as given in (2), with $k = j-1$.

$$Mj_1^x = MG\left(Mk_1^{2x+1}, Mk_0^{2x+1}, Mk_1^{2x}\right) \tag{2a}$$

$$Mj_0^x = MG\left(Mk_1^{2x+1}, Mk_0^{2x+1}, Mk_0^{2x}\right) \tag{2b}$$

The h-th level of IEMs outputs the last encoded signals Mh_1^0 and Mh_0^0 that are then processed by the Final Result Module (FRM). The latter implements the logic given in (3) to establish which of the output signals must be asserted to flag the recognized condition on the entire operands $A_{(n-1:0)}$ and $B_{(n-1:0)}$.

$$A_{big}B = MG(Mh_1^0, Mh_0^0, 0) \tag{3a}$$

$$A_{less}B = \overline{MG(Mh_1^0, Mh_0^0, 1)} \tag{3b}$$

$$A_{eq}B = MG(\overline{A_{big}B}, \overline{A_{less}B}, 0) \tag{3c}$$

Fig. 3 shows the circuit architectures of the FEM, the IEM and the FRM blocks.

To better explain the running of the novel comparator, let us examine the example reported in Fig. 4 that refers to the case in which the 2's complement 8-bit numbers $A_{(7:0)} = 11000000$ (i.e., -64) and $B_{(7:0)} = 01000000$ (i.e., 64) are compared. With n being equal to 8, $\frac{n}{2} = 4$ instances of FEM are required to process as many 2-bit sub-words of the operands. The signals $M0_1^i$ and $M0_0^i$, with $i = 0, \ldots, 3$, are inputted to the $h = 2$ levels of IEMs: as shown in Fig. 4, the first one (for which $j = 1$) consists of $y = 2$ IEMs, whereas the second one (for which $j = 2$) uses $y = 1$ IEM. The two levels of IEMs set both the signals $M2_1^0$ and $M2_0^0$ to 0 that, as above shown in Fig. 2b, encodes the condition $A<B$. Finally, the FRM furnishes $A_{big}B = 0$, $A_{eq}B = 0$ and $A_{less}B = 1$.

$$\#MGs = 2 \times \sum_{l=1}^{\log_2 n} \left(\frac{n}{2^l}\right) + 3 \tag{4a}$$

TABLE I
PRELIMINARY COMPARISON RESULTS

Design	Computational capability	n	#MGs	#INVs	#MGs_CP
[11]	A≥B	2	4	2	2
		4	11	4	3
		8	26	8	4
		16	57	16	5
		32	120	32	6
[12]	Full	2	10	7	4
		4	22	13	5
		8	46	25	9
[14] CB	Full	2	5	3	3
		4	11	5	4
		8	21	9	5
		16	43	17	8
		32	85	33	13
[14] TB	Full	16	35	17	7
		32	83	33	9
[15]	Full	2	9	4	3
		4	21	8	4
[19] CB	Full	2	5	3	3
		4	9	5	4
		8	17	9	6
		16	33	17	10
		32	65	33	18
[19] TB	Full	16	35	17	7
		32	67	33	11
New	Full	4	9	6	4
		8	17	10	5
		16	33	18	6
		32	65	34	7

$$\#INVs = n + 2 \tag{4b}$$

$$\#MGs\_CP = \log_2 \frac{n}{2} + 3 \tag{4c}$$

It is worth noting that the proposed approach leads to highly regular full comparator architectures. In fact, in contrast to the TB structures presented in [14] and [19], that, depending on the operands word-length n, employ up to six different basic modules, a binary comparator designed as proposed here employs, independently of n, only three simple modules properly arranged within the TB structure. Moreover, while the six basic modules utilized in [14] and [19] consist of up to six MGs and three INVs, as depicted in Fig. 3, the FEM, IEM and FRM blocks used within the novel comparators are significantly simpler.

The design complexity of the novel comparators can be evaluated in terms of the amount of used MGs and INVs, and the number of MGs within the worst computational path (#MGs_CP), as given in (4). Preliminary comparison results summarized in Table I show that, at a parity of the operands word-length and the computational capability, the novel comparator exhibits the shortest computational path and uses the fewest MGs. However, in order to achieve reliable comparison results, the post-implementation characteristics must be analyzed. Indeed, compliance with the QCA layout rules [21] may require additional clock phases. As an example, thermodynamic effects influence minimum and maximum number of cells in a single clock zone.

In accordance with [7]–[15], the proposed designs use a minimum of 2 cells and a maximum of 16 cells cascaded per clock zone. Moreover, due to their higher robustness [21], multilayer crossovers are preferred to coplanar ones. Clocking wires are assumed to be buried below the QCA base layer

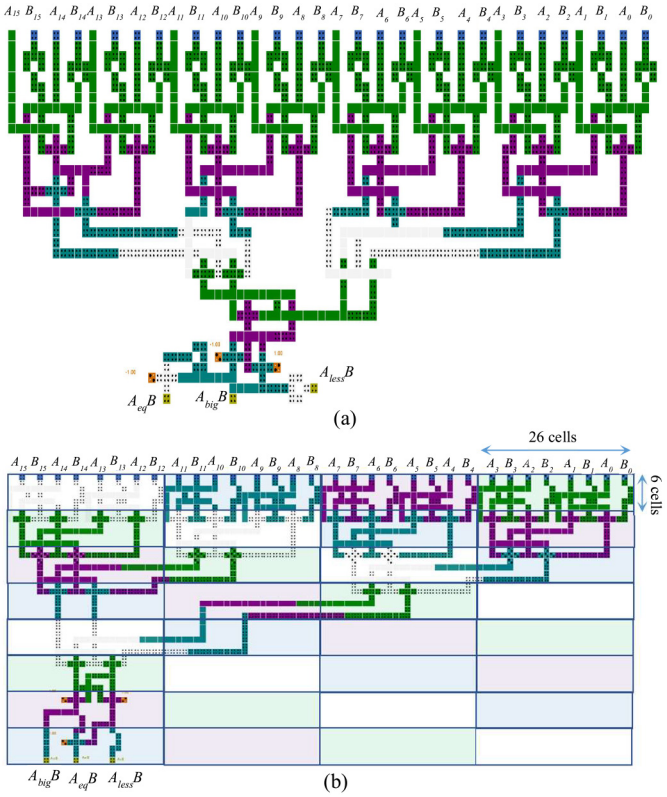

Fig. 5. Layout samples of the novel 16-bit comparator complying with: (a) the basic clocking scheme; (b) the 2DDWave clocking scheme.

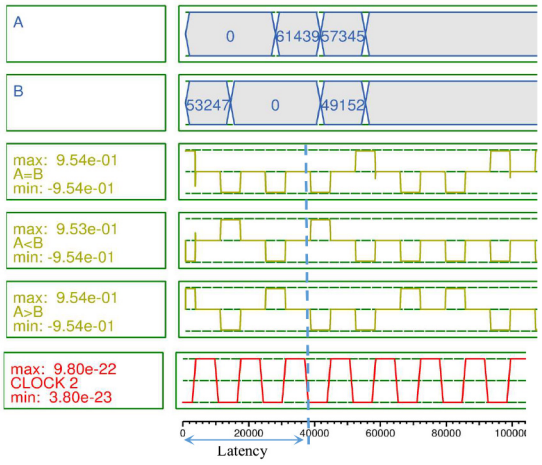

Fig. 6. Some simulation results related to the 16-bit comparator of Fig. 5b.

and to be endowed with small metal pads that assure a uniform electric field and precise control on inter-dot barrier of the cells. Accordingly, the new layouts have been partitioned into uniform, regular and bounded clock zones. In particular, the novel comparators have been laid-out to comply with the 2DDWave clocking scheme demonstrated in [20] and they have been characterized through the QCA Designer-E 2.2 software tool with default settings.

Samples of the implemented layouts are depicted in Fig. 5, whereas Fig. 6 shows some simulation results. Post-layout results are collected in Table II and compared with several existing counterparts. In order to have a touchstone, also the

TABLE II
POST-LAYOUT COMPARISON RESULTS

Design	n	Cell count	#CO	Size [μm^2]	Latency		Energy [eV]
					Cycles	#Phases	
[7]	1	67	-	0.072	3/4	3	-
[8]	1	100	-	0.109	1 1/4	5	-
[9]	7	221	-	0.289	9	36	-
[10]	1	353	-	0.459	2 1/4	9	-
[11]	2	138	-	0.162	1 1/4	5	-
[12]	1	97	-	0.135	1	4	-
	4	722	-	1.63	3 1/2	14	-
	8	1620	-	4.3	4 1/2	18	-
[13]	1	262	-	n.a.	2 1/4	9	-
[14] CB	2	155	-	0.15	1	4	-
	4	297	-	0.41	1 1/4	5	-
	8	699	-	0.79	1 3/4	7	-
	16	1392	-	1.5	2 1/2	10	-
	32	2783	-	2.66	3 3/4	15	-
[14] TB	8	756	35	0.75	1 3/4	7	2.36e-2
	16	1316	79	1.68	2	8	4.65e-2
	32	2951	160	2.88	2 3/4	11	9.79e-2
[15]	2	321	-	0.31	1 1/4	5	-
	4	853	-	1.06	1 3/4	7	-
[19] TB	16	1713	78	1.69	2 1/2	10	4.5e-2
New	8	579	37	0.55	1 3/4	7	2.18e-2
	16	1179	73	1.31	2	8	4.3e-2
	32	2467	147	2.65	2 3/4	11	8.73e-2
New 2DDWave	8	533	32	0.78	1 3/4	7	2.06e-2
	16	1175	64	2.05	2 3/4	11	3.75e-2
	32	2587	128	5.99	4 1/2	18	8.02e-2

TB comparators presented in [14] and [19] have been characterized in terms of energy consumption. It can be seen that, in comparison with [14], at a parity of the basic layout rules, the new comparator saves up to 26%, 23% and 11% of the occupied area, the used QCA cells and the average energy consumption, respectively.

An energy saving up to 19% is reached when the 2DDWave clocking scheme is adopted. In this case, the amount of used cells does not significantly change with respect to the layouts implemented using the basic clocking scheme. However as expected, the occupied area increases due to the geometric restrictions dictated by the 2DDWave scheme in terms of length and width of each clock zone [20].

The reliability of the proposed designs has been analyzed using the probabilistic transfer matrices (PTM) approach [22] assuming that the primary inputs are uniformly distributed and that each gate has an error probability $p = 0.1$. At first, for the basic modules FEM, IEM and FRM has been estimated the reliability 0.7216, 0.81 and 0.6152, respectively. Then, the fidelity of 0.6739 has been estimated for the output signals furnished by the new 4-bit comparator.

To further analyze the compared architectures, the generalized cost function *CF* proposed in [23] has been extended as given in (5) to take into account the consumed energy (E). There, #MGs and #INVs represent the amount of utilized logic gates, #CO the number of crossovers and #Phases the delay. Note that all the weightings are set to 1.

$$CF = (\#MGs + \#INVs + \#CO) \times \#Phases \times E \qquad (5)$$

The reduced energy consumption and size, in conjunction with the lower number of crossovers, make the new circuits able to achieve a CF up to 13% and 27% better than [14] and [19].

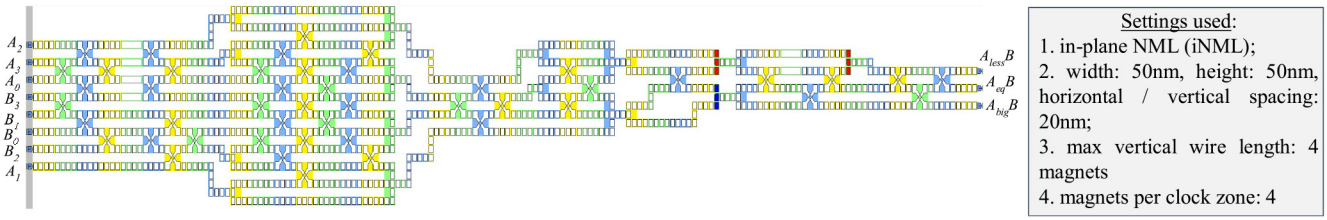

Fig. 7. The layout of the 4-bit NML-based comparator.

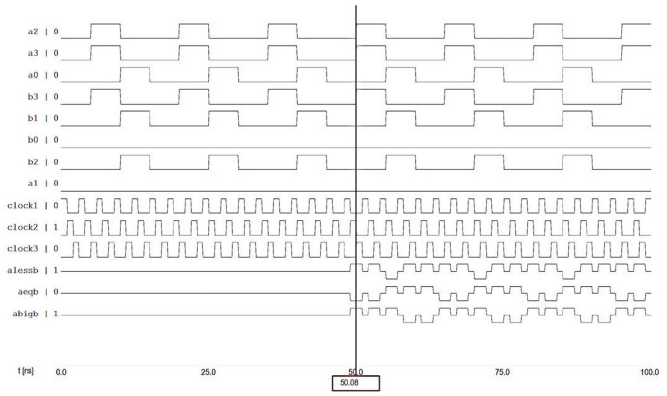

Fig. 8. Simulations of the 4-bit NML-based comparator.

Finally, the 4-bit version of the novel comparator has been implemented using the NML, thus demonstrating that the proposed logic can be efficiently exploited also with different nanotechnologies. The layout obtained using the ToPoliNano CAD Tool is shown in Fig. 7, whereas some simulation results are reported in Fig. 8. The proposed NML-based comparator requires 1183 magnets and uses 38 clock phases.

IV. Conclusion

The novel logic here presented allows designing efficient multi-bit QCA-based full comparators. Only three elementary modules, named FEM, IEM and FRM, are required to process multi-bit operands. Such an approach leads to highly regular TB architectures. Moreover, in comparison to state-of-the-art competitors, the comparators designed as proposed here achieve reduced computational complexity and average energy consumption.

References

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernestein, "Quantum cellular automata," *Nanotechnology*, vol. 4, no. 1, pp. 49–57, 1993.
[2] G. H. Bernstein *et al.*, "Magnetic QCA systems," *Microelectron. J.*, vol. 36, pp. 619–624, Jul. 2005.
[3] J. Ali, G. Jing, W. Qian, L. Mark, and D. Hongjie, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, no. 6949, pp. 654–657, 2003.
[4] S. Perri, F. Spagnolo, F. Frustaci, and P. Corsonello, "Accuracy improved low-energy multi-bit approximate adders in QCA," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 11, pp. 3456–3460, Nov. 2021.
[5] Z. Chu, Z. Li, Y. Xia, L. Wang, and W. Liu, "BCD adder designs based on three-input XOR and majority gates," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 6, pp. 1942–1946, Jun. 2021.
[6] T. Zhang, V. Pudi, and W. Liu, "New majority gate-based parallel BCD adder designs for quantum-dot cellular automata," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 7, pp. 1232–1236, Jul. 2019.
[7] J. R. Janulis, P. D. Tougaw, S. C. Henderson, and E. W. Johnson, "Serial bit-stream analysis using quantum-dot cellular automata," *IEEE Trans. Nanotechnol.*, vol. 3, no. 1, pp. 158–164, Mar. 2004.
[8] Q. Ke-Ming and X. Yin-Shui, "Quantum-dots cellular automata comparator," in *Proc. Int. Conf. ASIC (ASICON)*, Guilin, China, Oct. 2007, pp. 1297–1300.
[9] B. Lampreht *et al.*, "Quantum-dot cellular automata serial comparator," in *Proc. EUROMICRO Conf. Digit. Syst. Des. Archit. Methods Tools*, Parma, Italy, Sep. 2008, pp. 447–452.
[10] Y. Xia and K. Qiu, "Design and application of universal logic gate based on quantum-dot cellular automata," in *Proc. IEEE Int. Conf. Commun. Technol.*, Hangzhou, China, Nov. 2008, pp. 335–338.
[11] M. D. Wagh, Y. Sun, and V. Annampedu, "Implementation of comparison function using quantum-dot cellular automata," in *Proc. Nanotechnol. Conf. Trade Show (NSTI-NANOTECH)*, Boston, MA, USA, Jun. 2008, pp. 76–79.
[12] Y.-S. Xia and K.-M. Qiu, "Comparator design based on quantum-dot cellular automata," *J. Electron. Inf. Technol.*, vol. 31, no. 6, pp. 1517–1520, 2009.
[13] S.-Y. Ying, T.-P. Pei, and L.-R. Xiao, "Efficient design of QCA optimal universal logic gate ULG.2 and its application," in *Proc. Int. Conf. Comput. Appl. Syst. Model. (ICCASM)*, Taiyuan, China, Oct. 2010, pp. 392–396.
[14] S. Perri, P. Corsonello, and G. Cocorullo, "Design of efficient binary comparators in quantum-dot cellular automata," *IEEE Trans. Nanotechnol.*, vol. 13, no. 2, pp. 192–202, Mar. 2014.
[15] L. Jun-Wen and X. Yin-Shui, "A novel design of quantum-dots cellular automata comparator using five-input majority gate," in *Proc. IEEE Int. Conf. Solid-State Integr. Circuit Technol. (ICSICT)*, Qingdao, China, Oct. 2018, pp. 1–3.
[16] S. S. Roy, C. Mukherjee, S. Panda, A. K. Mukhopadhyay, and B. Maji, "Layered T comparator design using quantum-dot cellular automata," in *Proc. Devices Integr. Circuit (DevIC)*, Kalyani, India, Mar. 2017, pp. 90–94.
[17] S. Ahmed, S. M. Bhat, and V. Kakkar, "Design of efficient 1-bit comparator in quantum dot cellular automata nano-computing," in *Proc. IEEE-HYDCON*, Hyderabad, India, Sep. 2020, pp. 1–6.
[18] L. Wang and G. Xie, "A novel XOR/XNOR structure for modular design of QCA circuits," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 12, pp. 3327–3331, Dec. 2020.
[19] K. Dubey, R. Marshal, and G. Lakshminarayanan, "Design of majority logic based comparator," in *Proc. Int. Conf. Comput. Commun. Netw. Technol. (ICCCNT)*, Bengaluru, India, Jul. 2018, pp. 1–6.
[20] V. Vankamamidi, M. Ottavi, and F. Lombardi, "Two-dimensional schemes for clocking/timing of QCA circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 27, no. 1, pp. 34–44, Jan. 2008.
[21] W. Liu, L. Lu, M. O'Neill, and E. E. Swartzlander, "Design rules for quantum-dot cellular automata," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Rio de Janeiro, Brazil, May 2011, pp. 2361–2364.
[22] S. Krishnaswamy, G. F. Viamontes, I. L. Markov, and J. P. Hayes, "Probabilistic transfer matrices in symbolic reliability analysis of logic circuits," *ACM Trans. Design Autom. Electron. Syst.*, vol. 13, no. 1, pp. 1–35, 2008.
[23] W. Liu, L. Lu, M. O'Neill, and E. E. Swartzlander, "A first step toward cost functions for quantum-dot cellular automata designs," *IEEE Trans. Nanotechnol.*, vol. 13, no. 3, pp. 476–487, May 2014.

Open Access funding provided by 'Università della Calabria' within the CRUI CARE Agreement