Multirate Timestamp Modeling for Ultralow-Jitter Frequency Synthesis: A Tutorial

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Abstract—In this tutorial brief, we introduce a unified wideband phase-noise theory framework of frequency synthesis based on a multirate timestamp modeling with "two z-variables". We apply it to model and analyze two types of ultra-low jitter (i.e., sub-50 fs) phase-locking techniques: 1) high-bandwidth PLLs with high phase-detector gain (with emphasis on all-digital PLLs), and 2) injection locking (IL) or recently proposed charge-sharing locking (CSL), serving as a unified guide on achieving the sub-50 fs jitter. All analytical results are numerically verified through time-domain behavioral simulations, demonstrating that the theoretically maximum bandwidths are around 30% and 44% of the reference frequency in PLLs and IL, respectively.

Index Terms—5G, ADPLL, charge-sharing locking (CSL), injection locking (IL), low-jitter, multirate timestamp, subsampling (SS), two z-variables.

I. INTRODUCTION

A FREQUENCY synthesizer of ultra-low jitter (i.e., sub-50 fs) is a key block to enable the emerging 5G/6G wireless and other high-speed communication standards [1]–[3]. There are two main routes being pursued towards achieving such tough jitter performance: high-bandwidth PLLs with a high phase-detector (PD) gain [4]–[14], and injection-locking (IL) [15]–[24] or a recently introduced generalization of it, charge-sharing locking (CSL) [2], [25]. It is becoming increasingly obvious that the phase noise (PN) modeling in these high-bandwidth techniques must be radically different from what is currently used in the regular-bandwidth PLLs (e.g., s-domain). Thus, a unified system modeling technique that can explain all significant PN phenomena in both high-bandwidth PLL and CSL/IL synthesizers is highly desired. In this tutorial, we examine a multirate timestamp modeling technique [26]–[32] based on our recently published method of

"two z-variables" [2], serving as a unified guide for designing frequency synthesizers of ultra-low jitter.

II. BASICS OF MULTIRATE TIMESTAMP MODELING

A. Timestamps of Reference and Oscillator Clocks

As illustrated in Fig. 1(a) and (b), an nth timestamp of the reference (with an average period of T_{ref}), $t_{\text{ref}}[n]$, and a kth timestamp of the free-running oscillator (with an average period of T_{osc}), $t_{\text{osc}}[k]$, are modeled as

$$\begin{cases} t_{\text{ref}}[n] = nT_{\text{ref}} + \Delta t_{\text{ref}}[n] \\ t_{\text{osc}}[k] = kT_{\text{osc}} + \Delta t_{\text{osc}}[k] = \sum_{m=1}^{k}(T_{\text{osc}} + \Delta T_{\text{osc}}[m]) \end{cases} \tag{1}$$

where $\Delta t_{\text{ref}}[n]$ is the reference's "instantaneous absolute jitter", while $\Delta t_{\text{osc}}[k]$ and $\Delta T_{\text{osc}}[k]$ are the oscillator's instantaneous "absolute jitter" and "period jitter", respectively (all the timestamp sequences are assumed null when $n \le 0$ or $k \le 0$). Accordingly, we introduce two z-variables, z_{ref} and z_{osc}, for the z-transforms of the above multirate timestamps, denoted as $\widehat{T}(\cdot)$. Assuming $NT_{\text{osc}} = T_{\text{ref}}$ with N being the frequency multiplication ratio, normalizing $|\widehat{T}(\cdot)|^2$ into phase domain, and employing

$$z_{\text{ref}} = e^{j2\pi \Delta f/f_{\text{ref}}} \text{ and } z_{\text{osc}} = e^{j2\pi \Delta f/f_{\text{osc}}}, \tag{2}$$

wideband PN analysis can be conducted with a frequency offset of interest $|\Delta f|$ of up to $f_{\text{osc}}/2$, where $f_{\text{osc}} = 1/T_{\text{osc}}$ and $f_{\text{ref}} = 1/T_{\text{ref}}$.

B. Upsampling and ZOH of Reference-Rate Timestamps

To interface the timestamps of a low sampling rate (i.e., f_{ref}) with those of a high sampling-rate (i.e., f_{osc}), an upsampling followed by discrete-time "zero-order holding" (ZOH) is illustrated in Fig. 1(a), with their z-transforms as

$$\widehat{T}_{\text{ref,up}}(z_{\text{osc}}) = \widehat{T}_{\text{ref}}(z_{\text{osc}}^N) = \widehat{T}_{\text{ref}}(z_{\text{ref}}) \tag{3}$$

$$H_{\text{zoh}} = \frac{\widehat{T}_{\text{ref,up-zoh}}}{\widehat{T}_{\text{ref,up}}} = \frac{1 - z_{\text{ref}}^{-1}}{1 - z_{\text{osc}}^{-1}} = \left\{ \frac{1}{N} \frac{1 - z_{\text{ref}}^{-1}}{1 - z_{\text{osc}}^{-1}} \right\} \cdot N \tag{4}$$

where z_{ref}^{-1} and z_{osc}^{-1} represent one reference and one oscillator delay (in which $z_{\text{ref}}^{-1} = z_{\text{osc}}^{-N}$), respectively, and the dc gain of H_{zoh} is N. The PN of $t_{\text{ref,up-zoh}}[k]$ can be calculated as

$$\mathcal{L}_{\text{ref,up-zoh}}(z_{\text{osc}}(\Delta f)) = \left| \frac{1}{N} \frac{1 - z_{\text{ref}}^{-1}}{1 - z_{\text{osc}}^{-1}} \right|^2 \cdot N^2 \mathcal{L}_{\text{ref}}(z_{\text{ref}}(\Delta f)) \tag{5}$$

where $\mathcal{L}_{\text{ref}}$ represents the PN of $t_{\text{ref}}[n]$, while Δf in $\mathcal{L}_{\text{ref,up-zoh}}$ extends to $f_{\text{osc}}/2$ by virtue of aliasing $\mathcal{L}_{\text{ref}}(z_{\text{ref}}(\Delta f + mf_{\text{ref}})) =$
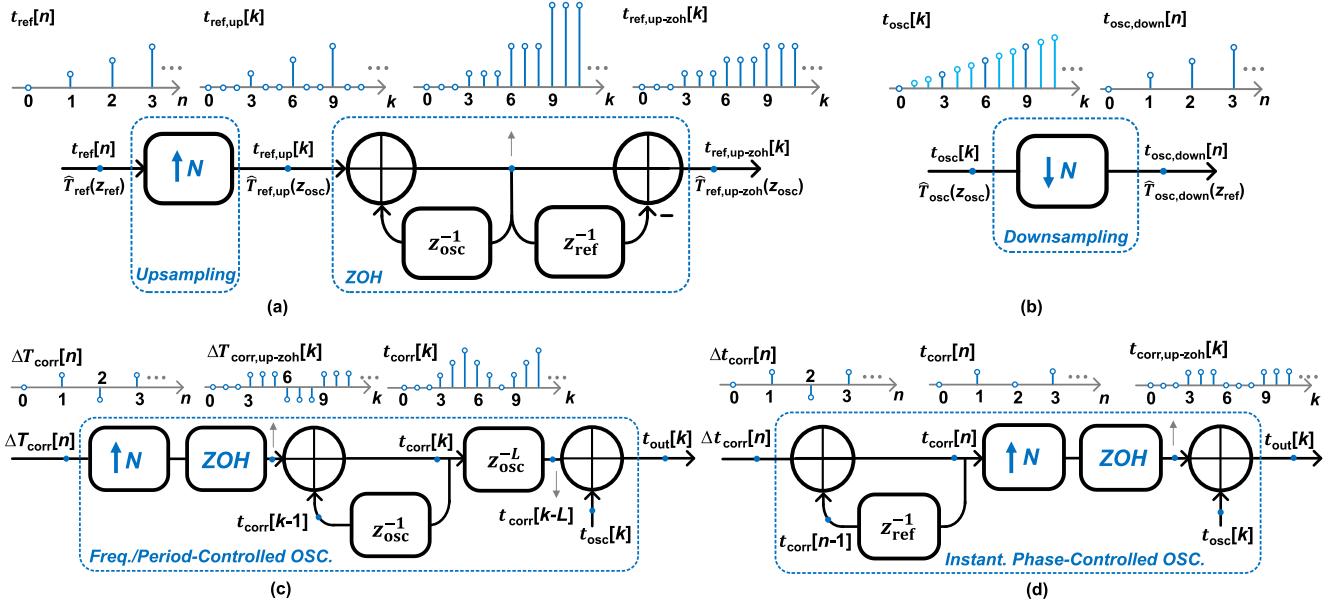
Fig. 1. (a) Upsampling and zero-order holding (ZOH) of a reference's timestamps: from $t_{ref}[n]$ to $t_{ref,up\text{-}zoh}[k]$. (b) Downsampling of timestamps of a free-running oscillator: from $t_{osc}[k]$ to $t_{osc,down}[n]$. Multirate timestamp models of (c) frequency/period-controlled oscillators (e.g., VCOs or DCOs), and (d) instantaneous phase-controlled oscillators (e.g., CSL or IL). Examples with $N = 3$ and all the timestamp sequences are null when $n \leq 0$ or $k \leq 0$.

$\mathcal{L}_{ref}(z_{ref}(\Delta f))$ for $|\Delta f| > f_{ref}/2$. The N^2 factor, due to the upsampling and ZOH, models the PN scaling from the reference's to the oscillator's phase domains. Further, $\mathcal{L}_{ref}(z_{ref})$ can be modeled by the power spectral density (PSD) of Gaussian noise as (neglecting the flicker PN)

$$\mathcal{L}_{ref}(z_{ref}(\Delta f)) \approx \frac{(2\pi\sigma_{\Delta t,ref}/T_{ref})^2}{f_{ref}} \tag{6}$$

where $\sigma_{\Delta t,ref}$ is the root-mean-square (rms) value of $\Delta t_{ref}[n]$ (i.e., rms jitter) and $|\Delta f| < f_{ref}/2$. For a high-performance system, we can reasonably consider $f_{ref} = 200\,\text{MHz}$ with $\sigma_{\Delta t,ref}$ of $35.6{\sim}112.5\,\text{fs}$ (also including contributions by the reference on-chip distribution network), which respectively corresponds to the PN of $10^{-170/10} \sim 10^{-160/10}\,\text{rad}^2/\text{Hz}$ (i.e., $-170 \sim -160\,\text{dBc/Hz}$).

C. Downsampling of Oscillator-Rate Timestamps

To bridge from the high (i.e., f_{osc}) to low (i.e., f_{ref}) sampling-rate timestamps, we point out the intrinsic oscillator downsampling [see Fig. 1(b)] taking place in all phase-locked systems, including divider-based PLLs (e.g., charge-pump PLLs (CP-PLLs) [33]), divider-less PLLs (e.g., all-digital PLLs (ADPLLs) [30], [34] or sub-sampling PLLs (SS-PLLs) [4]), and CSL/IL [2]. Accordingly, we have [2]:

$$\widehat{T}_{osc,down}(z_{ref}) = \frac{1}{N}\widehat{T}_{osc}(z_{ref}^{\frac{1}{N}}) + \frac{1}{N}\sum_{m=1}^{N-1}\widehat{T}_{osc}(z_{ref}^{\frac{1}{N}}e^{-j2\pi\frac{m}{N}})$$

$$\approx \frac{1}{N}\widehat{T}_{osc}(z_{osc}) \tag{7}$$

where $\widehat{T}_{osc}(z_{osc})$ is the z-transform of $t_{osc}[k]$, while its spectral replicas due to downsampling are neglected.[1] The PN of

[1]A detailed discussion of PN folding by downsampling causing the oscillator PN increasing 3 dB beyond the "loop" cutoff frequency in ideal CSL/IL is presented in [2], culminating in [2, Fig. 7(a)]. However, this can be neglected in most practical PLL/IL systems (refer to [2, Fig. 7(b)–(d) and Fig. 17] and [32, Fig. 9(right)] for such examples).

$t_{osc,down}[n]$ can be calculated as

$$\mathcal{L}_{osc,down}(z_{ref}(\Delta f)) \approx \frac{1}{N^2} \cdot \mathcal{L}_{osc}(z_{osc}(\Delta f)) \tag{8}$$

where $|\Delta f| < f_{ref}/2$ in $\mathcal{L}_{osc,down}$. The $1/N^2$ factor, induced by downsampling, represents the PN scaling from the f_{osc} to f_{ref} domains. $\mathcal{L}_{osc}(z_{osc})$ can be modeled as a PSD of Gaussian noise passing through an accumulator as (neglecting $1/f^3$ PN)

$$\mathcal{L}_{osc}(z_{osc}(\Delta f)) \approx \frac{(2\pi\sigma_{\Delta T,osc}/T_{osc})^2}{f_{osc}} \cdot \left|\frac{1}{1-z_{osc}^{-1}}\right|^2 \tag{9}$$

where $\sigma_{\Delta T,osc}$ is the rms value of $\Delta T_{osc}[k]$ and $|\Delta f| < f_{osc}/2$. For advanced CMOS oscillators [35]–[40] with flicker PN suppressing techniques [41]–[47], substituting $\mathcal{L}_{osc} = 10^{-140/10}\,\text{rad}^2/\text{Hz}$ (i.e., $-140\,\text{dBc/Hz}$) at $\Delta f = 10\,\text{MHz}$ and $f_{osc} = 10\,\text{GHz}$ into (9) yields $\sigma_{\Delta T,osc} = 1\,\text{fs}$.

D. Freq./Period-Controlled & Phase-Controlled Oscillators

Fig. 1(c) shows the multirate timestamp model for the "frequency/period-controlled oscillators" (e.g., VCOs or digitally-controlled oscillators (DCOs)) for use in PLLs. Its period-correcting f_{ref}-rate samples $\Delta T_{corr}[n]$ (e.g., modeling the tuning capacitance effect in an LC-tank) are upsampled, zero-order held, and accumulated in each oscillator cycle, resulting in the correcting timestamps $t_{corr}[k]$ for the intrinsic $t_{osc}[k]$. The delay of z_{osc}^{-L} is discussed in Section III-A.

On the other hand, for the "phase-controlled oscillator" [see Fig. 1(d)], the correcting timestamps $t_{corr,up\text{-}zoh}[k]$ *instantaneously* adjust the intrinsic $t_{osc}[k]$ once every reference cycle. This represents the changing charge at the reference rate in the LC-tank. The reference-rate accumulator models the memory effect of the timestamp correction (i.e., phase correction). In contrast to the frequency-controlled oscillators in PLLs featuring at least one oscillator delay (i.e., z_{osc}^{-1}), there is practically no loop delay here (in practice, $\ll T_{osc}$).
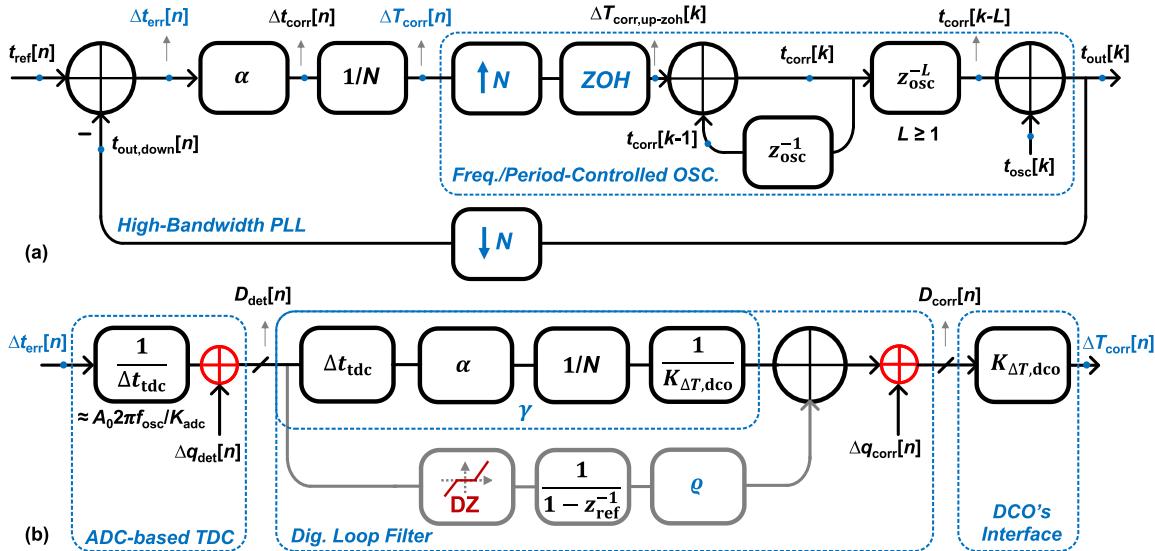
Fig. 2. (a) Conceptual multirate timestamp model suitable for a high-bandwidth PLL. (b) Implementation details of the ADPLL blocks (ADC-based TDC and digital loop filter) that convert $\Delta t_{\mathrm{err}}[n]$ into $\Delta T_{\mathrm{corr}}[n]$.

III. MULTIRATE TIMESTAMP MODELS

A. Multirate Timestamp Model of High-Bandwidth PLLs

Combining the frequency/period-controlled oscillator and downsampler, the multirate timestamp model for a conceptual PLL is illustrated in Fig. 2(a). Its possible implementation within the context of a high-bandwidth ADPLL is shown in Fig. 2(b).[2] It focuses on the time-to-digital converter (TDC) based on an analog-to-digital converter (ADC) and digital loop filter with proportional (i.e., α) and integral (i.e., ρ) paths.

Since the phase of the frequency-tunable oscillator cannot be corrected immediately, $t_{\mathrm{corr}}[k]$ calculated at the end of nth reference cycle (i.e., $k = nN$) will not be visible until at least the next oscillator cycle.[3] Thus, a loop delay of z_{osc}^{-L} ($L \geq 1$) is introduced between $t_{\mathrm{corr}}[k]$ and $t_{\mathrm{osc}}[k]$. L is an integer here, readily estimated by inspection (or a quick simulation) of the PLL structure. For example, $L = 1$ accounts for bang-bang PLLs, $L \approx \lceil \tau_{\mathrm{pulse}}/T_{\mathrm{osc}} \rceil + 1$ for SS-PLLs, while $L \approx \lceil N/2 \rceil + 1$ is for modeling an ADPLL which detects Δt_{err} at the rising edges of f_{ref} yet updates the DCO's tuning word at the f_{ref}'s falling edges.[4] It should be emphasized that the loop delay z_{osc}^{-L} is for modeling the delay of $t_{\mathrm{corr}}[k]$ rather than for $t_{\mathrm{osc}}[k]$. Thus, z_{osc}^{-L} should not be set in the feedback path, neither before [32] nor after the downsampler.

1) ADC-Based TDC: To break the resolution limitation of a single inverter delay (e.g., $\sim 10\,\mathrm{ps}$ in 28-nm CMOS) in conventional TDCs [34], [49], [50], the idea of skillfully combining sampling of the sharp oscillator [4], [7] or reference[5] [51]

edges with an ADC [6], [46], [52]–[54] appears a promising solution, while its fractional-N operation may rely on a digital-to-time converter (DTC) [9], [10], [55]–[57] or DAC [5], [46], [53], [58]. Considering such a conceptual ADC-based TDC 'sampling' the oscillator's slope, its TDC gain, Δt_{tdc} (unit: s/bit), is derived as

$$\Delta t_{\mathrm{tdc}} = \frac{K_{\mathrm{adc}}}{K_{\mathrm{TD}}} = \frac{K_{\mathrm{adc}}}{\mathrm{d}V_{\mathrm{osc}}/\mathrm{d}t|_{t=0}} = \frac{K_{\mathrm{adc}}}{A_0 2\pi f_{\mathrm{osc}}} \tag{10}$$

where $V_{\mathrm{osc}} = A_0 \sin 2\pi f_{\mathrm{osc}} t$. K_{adc} (unit: V/bit) is the ADC gain, while K_{TD} (unit:V/s) is the gain ("PD-gain") of timestamp detector (TD). Its digital output D_{det} is[6]

$$D_{\mathrm{det}}[n] = \Delta t_{\mathrm{err}}[n]/\Delta t_{\mathrm{tdc}} + \Delta q_{\mathrm{det}}[n] \tag{11}$$

where $\Delta q_{\mathrm{det}}[n]$ (unit: bit) is the detection quantizaiton noise and $|\Delta q_{\mathrm{det}}[n]| \leq 0.5$ bit. Since $\Delta t_{\mathrm{err}}[n]$ is fairly randomly distributed when phase locked, the variance of $\Delta q_{\mathrm{det}}[n]$, $\sigma_{\Delta q,\mathrm{det}}$, is about $1/\sqrt{12}$ bit [34]. Normalizing $\sigma_{\Delta q,\mathrm{det}}$ into the reference PN domain (i.e., $2\pi\sigma_{\Delta q,\mathrm{det}}/(1/\Delta t_{\mathrm{tdc}})/T_{\mathrm{ref}}$), we get

$$\mathcal{L}_{\Delta q,\mathrm{det}}(z_{\mathrm{ref}}(\Delta f)) \approx \frac{(2\pi\,\Delta t_{\mathrm{tdc}}/T_{\mathrm{ref}})^2/12}{f_{\mathrm{ref}}} \tag{12}$$

where $|\Delta f| < f_{\mathrm{ref}}/2$. Comparing (6) and (12), once $\Delta t_{\mathrm{tdc}} \approx \sigma_{\Delta t,\mathrm{ref}}$ (e.g., $\sim 100\,\mathrm{fs/bit}$), $\mathcal{L}_{\Delta q,\mathrm{det}}$ could be practically neglected. Assuming $A_0 = 0.5\,\mathrm{V}$, $f_{\mathrm{osc}} = 10\,\mathrm{GHz}$, and $K_{\mathrm{adc}} = 3.14\,\mathrm{mV/bit}$, we get $\Delta t_{\mathrm{tdc}} = 100\,\mathrm{fs/bit}$, where the high TD-gain (e.g., $K_{\mathrm{TD}} = 3.14\,\mathrm{mV}/100\,\mathrm{fs} > 10\,\mathrm{GV/s}$) is the key factor[7] in achieving such fine Δt_{tdc}.

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[2] The multirate timestamp modeling for a type-II CP-PLL's analog loop filter (R and C in series) [48] and charge-pump (I_{cp}) could be written as $\Delta T_{\mathrm{corr}}[n] = \Delta t_{\mathrm{err}}[n] \cdot I_{\mathrm{cp}}/T_{\mathrm{ref}} \cdot (R + T_{\mathrm{ref}}/C/(1-z_{\mathrm{ref}}^{-1})) \cdot K_{\mathrm{vco}} \cdot T_{\mathrm{osc}}/f_{\mathrm{osc}}$, where $I_{\mathrm{cp}}/T_{\mathrm{ref}}$ is used to normalize $\Delta t_{\mathrm{err}}[n]$ into a correcting current sequence (i.e., average current in each reference cycle). Replacing I_{cp} with $A_0 2\pi f_{\mathrm{osc}} \cdot g_m \cdot \tau_{\mathrm{pulse}}$, the SS-PLL's [4] model could be obtained.

[3] For further details, refer to the DCO's timestamp's model in Verilog-AMS on [44, p. 74] (the model can accept an asynchronous change at the frequency/period-tuning input within an oscillator cycle and execute it at the next oscillator cycle).

[4] For example, if $N = 49$ or 50, the updated $t_{\mathrm{corr}}[k]$ is assumed appearing at the 26th T_{osc} within the reference cycle (i.e., $L = 26$).

[5] The PD-gain (i.e., slope or TD-gain) from the reference's sinusoidal waveform is roughly $N\times$ lower than from the oscillator's, thus limiting the jitter performance. A remedy proposed in [9], [11] is to condition the reference's or divider's waveform by a sharp RC filter before sampling.

[6] By subtracting 2^{M-1}, an M-bit ADC output is from $[2^M - 1 : 0]$ to $[2^{M-1}-1 : -2^{M-1}]$ (i.e., mid-tread quantizer with "0" output) for a linear and well-defined PD-gain rather than an input-dependent PD-gain in a bang-bang operation (or other mid-riser quantizers without the "0" output).

[7] Similarly, the "PD/CP noise" (added after CP) could also be fully suppressed by the high PD/TD-gain of the phase detector when referring it to the reference PN (e.g., "PD/CP noise" will be divided by $(A_0 2\pi f_{\mathrm{osc}} \cdot g_m \cdot \tau_{\mathrm{pulse}})^2$ in SS-PLL rather than by much smaller I_{cp}^2 [59] in CP-PLL). This points to the nonexistence of the so-called "not multiplied by N^2" for "PD/CP noise"[4] due to the divider-less arrangement [2].
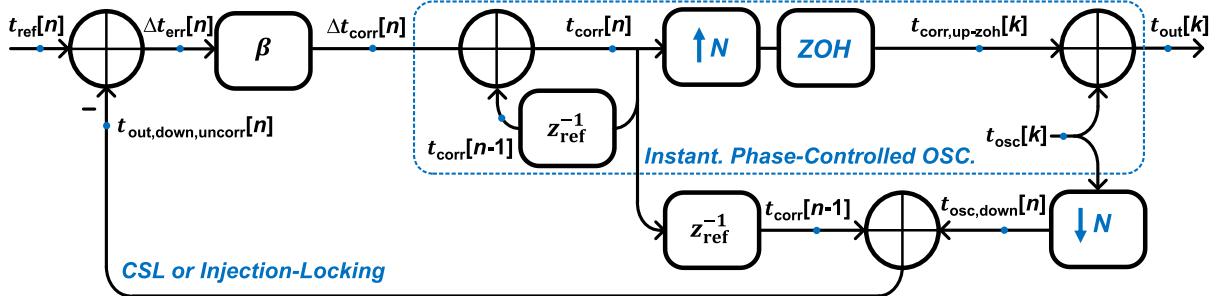
Fig. 3.   Multirate timestamp model of CSL or IL oscillators [2].

2) Digital Loop Filter: In fact, the timestamp error Δt_{err} consists of the reference and oscillator PN components (zero-mean) and the part induced by the frequency offset of the free-running oscillator (i.e., $NT_{\text{osc}} - T_{\text{ref}} \neq 0$, inducing a static phase offset in type-I PLLs in Fig. 2(a) and a spurious tone in CSL/IL [2]). Assume the frequency offset is minimized by the integral path ρ (controlling the convergence speed) with a controlled deadzone (DZ) [2],[8] the PLL now degenerates into a type-I PLL for the phase noise correction and the integral path will not normally conflict with the proportional path. Then,

$$D_{\text{corr}}[n] = D_{\text{det}}[n] \times \gamma + \Delta q_{\text{corr}}[n] \tag{13}$$

where γ and $\Delta q_{\text{corr}}[n]$ (unit: bit) are the "TDC-to-DCO code ratio" and the DCO quantization noise, respectively. For example, in a practical digital implementation, γ could be set as 2^{-1} or 2^{-2} by arithmetic right bit shifting (i.e., ">>>"), mathematically the same as $\gamma = 2^0$ with a coarser TDC step of $2\Delta t_{\text{tdc}}$ or $4\Delta t_{\text{tdc}}$. It could be also set as 2^1 or 2^2 by left bit shifting (i.e., "<<<") or 2^0 without any shifting. If γ is regarded as an integer, we assume $\Delta q_{\text{corr}}[n] = 0$. To understand how to choose γ (where $\rho << \gamma$), we define a PLL "timestamp correcting factor", α, as

$$\alpha \equiv \frac{N\Delta T_{\text{corr}}}{\Delta t_{\text{err}}} \approx \frac{D_{\text{corr}}NK_{\Delta T,\text{dco}}}{D_{\text{det}}\Delta t_{\text{tdc}}}$$
$$= \gamma \frac{NK_{\Delta T,\text{dco}}}{\Delta t_{\text{tdc}}} = \gamma \frac{K_{\Delta T,\text{dco}}/T_{\text{osc}}}{\Delta t_{\text{tdc}}/T_{\text{ref}}} \leq 1 \tag{14}$$

where $N\Delta T_{\text{corr}}$ is the maximum timestamp error correcting value [see Fig. 1(c)] in one reference cycle. $K_{\Delta T,\text{dco}}/T_{\text{osc}}$ ($\approx K_{\text{dco}}/f_{\text{osc}}$) and $\Delta t_{\text{tdc}}/T_{\text{ref}}$ are the normalized DCO gain and TDC gain (unit: ppm/bit), respectively. Furthermore, $\alpha \leq 1$ aims to prevent over-correcting that would cause instability, especially with a longer loop delay. For $\alpha \approx 0.5$, $\Delta t_{\text{tdc}} = 100\,\text{fs/bit}$, and $f_{\text{ref}} = 200\,\text{MHz}$ (i.e., $\Delta t_{\text{tdc}}/T_{\text{ref}} = 20\,\text{ppm/bit}$), it may require $K_{\Delta T,\text{dco}}/T_{\text{osc}}$ of $\sim 10\,\text{ppm/bit}$ and the corresponding customized switched-capacitor's resolution of $\sim 10\,\text{aF/bit}$ in a 10 GHz DCO [2]. The z-transform of $t_{\text{out}}[k]$ in Fig. 2 is

$$\widehat{T}_{\text{out}}(z_{\text{osc}}) \approx \frac{1}{N} \frac{H_{\text{corr}}}{1 + H_{\text{corr}}/N} N\widehat{T}_{\text{ref}}(z_{\text{ref}})$$
$$+ \left(1 - \frac{1}{N} \frac{H_{\text{corr}}}{1 + H_{\text{corr}}/N}\right)\widehat{T}_{\text{osc}}(z_{\text{osc}}) \tag{15}$$

[8]For a symmetric DZ (as well as ρ), this could be implemented by arithmetic right bit shifting (at least ">>> 1") with a ensuing corrective increment ("+1") for the negative values.

where

$$H_{\text{corr}} = \alpha \frac{1}{N} \frac{1 - z_{\text{ref}}^{-1}}{1 - z_{\text{osc}}^{-1}} \frac{1}{1 - z_{\text{osc}}^{-1}} z_{\text{osc}}^{-L} \tag{16}$$

is a transfer function of the feedforward path. By normalizing $|\widehat{T}_{\text{out}}(z_{\text{osc}})|^2$ into phase domain, we get

$$\mathcal{L}_{\text{out}}(z_{\text{osc}}) \approx \left| \frac{1}{N} \frac{H_{\text{corr}}}{1 + H_{\text{corr}}/N} \right|^2 \cdot N^2 (\mathcal{L}_{\text{ref}}(z_{\text{ref}}) + \mathcal{L}_{\Delta q,\text{det}}(z_{\text{ref}}))$$
$$+ \left| 1 - \frac{1}{N} \frac{H_{\text{corr}}}{1 + H_{\text{corr}}/N} \right|^2 \cdot \mathcal{L}_{\text{osc}}(z_{\text{osc}}) \tag{17}$$

where there are no cross-products between $\widehat{T}_{\text{ref}}$ and $\widehat{T}_{\text{osc}}$ due to their independence. It should be also noted that a noise added from $t_{\text{ref}}[n]$ (e.g., $\mathcal{L}_{\text{ref}}$), $\Delta t_{\text{err}}[n]$ (e.g., $\mathcal{L}_{\Delta q,\text{det}}$) or $t_{\text{out,down}}[n]$ experiences the same transfer function to the output.

B. Multirate Timestamp Model of CSL (or IL)

On the other hand, a new multirate timestamp model for CSL (or IL) was recently introduced (see Fig. 3) based on the "instantaneous phase-controlled oscillator" [2]. The timestamp error $\Delta t_{\text{err}}[n]$ is attenuated by the CSL/IL strength factor β (i.e., "timestamp correcting factor" in CSL/IL) to obtain the input correcting timestamps $\Delta t_{\text{corr}}[n]$, and

$$\beta \equiv \frac{\Delta t_{\text{corr}}}{\Delta t_{\text{err}}} \leq 1 \tag{18}$$

which depends on pulse width, switch size, and capacitance ratio [2]. Both α in (14) and β in (18) have the same physical meaning, describing the strength of correcting Δt_{err} and determining the bandwidth in PLL and CSL/IL for jitter optimization, respectively.

Since there is no significant delay in the feedforward path due to the nature of CSL/IL (unlike that in Fig. 2), it cannot directly downsample the final $t_{\text{out}}[k]$ by N to feed it back for the comparison with $t_{\text{ref}}[n]$, otherwise leading to incomputable discrete-time "delay-free loop" (such as [60, Fig. 3]). Instead, we introduce the uncorrected $t_{\text{out}}[k]$ at $t = nT_{\text{ref}}^- = nT_{\text{ref}} - \epsilon_t$ ($\epsilon_t \ll T_{\text{osc}}$), as

$$t_{\text{out,down,uncorr}}[n] = t_{\text{corr}}[n-1] + t_{\text{osc,down}}[n] \tag{19}$$

where $t_{\text{corr}}[n-1]$ is the $(n-1)$th correcting timestamp (i.e., before being updated to $t_{\text{corr}}[n]$ at $t = nT_{\text{ref}}^-$) for the free-running oscillator. The downsampled signal $t_{\text{osc,down}}[n]$ of $t_{\text{osc}}[k]$ is assumed identical to the latter when $t = nT_{\text{ref}}^-$
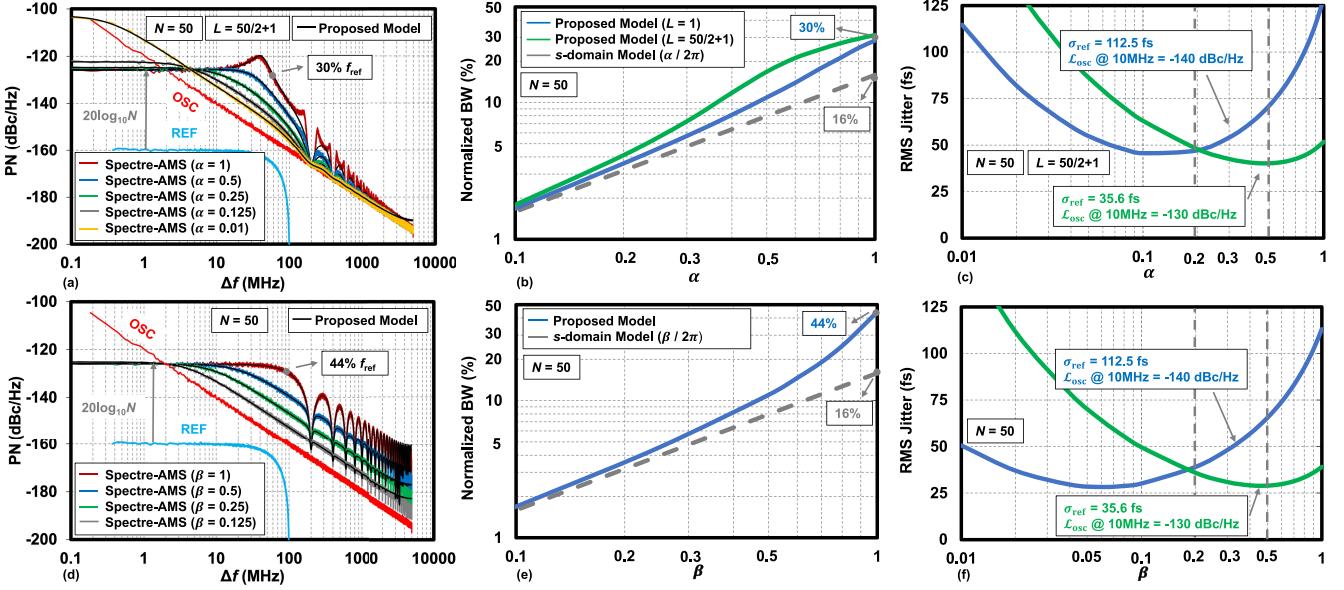
Fig. 4. Calculated [based on (17) and (21)] and simulated PN for different α (e.g., Sweeping Δt_{tdc} with $K_{\Delta T,dco}/T_{osc} = 10\,\text{ppm/bit}$ and $\gamma N K_{\Delta T,dco} = 50\,\text{fs/bit}$) in (a) ADPLL and for different β in (d) CSL/IL [Conditions: $f_{ref} = 200\,\text{MHz}$ with $\sigma_{\Delta t,ref} = 112.5\,\text{fs}$; $f_{osc} = 10\,\text{GHz}$ with $\mathcal{L}_{osc}$ @ $10\,\text{MHz} = 10^{-140/10}\,\text{rad}^2/\text{Hz}$]. Calculated normalized bandwidth with f_{ref} in (b) ADPLL for $L = 1$ or $L = \lceil N/2 \rceil + 1$ and (e) in IL/CSL. Calculated rms jitter vs. different α in (c) ADPLL and different β in (f) CSL/IL.

and $t = nT_{ref}$ due to $\epsilon_t \ll T_{osc}$. The z-transform of $t_{out}[k]$, $\widehat{T}_{out}(z_{osc})$, in Fig. 3 can be derived as

$$\widehat{T}_{out}(z_{osc}) \approx \frac{1}{N} \frac{1 - z_{ref}^{-1}}{1 - z_{osc}^{-1}} \frac{\beta}{1 - (1-\beta)z_{ref}^{-1}} N\widehat{T}_{ref}(z_{ref})$$

$$+ \left(1 - \frac{1}{N} \frac{1 - z_{ref}^{-1}}{1 - z_{osc}^{-1}} \frac{\beta}{1 - (1-\beta)z_{ref}^{-1}} \right) \widehat{T}_{osc}(z_{osc}) \quad (20)$$

and the corresponding PN is

$$\mathcal{L}_{out}(z_{osc}) \approx \left| \frac{1}{N} \frac{1 - z_{ref}^{-1}}{1 - z_{osc}^{-1}} \frac{\beta}{1 - (1-\beta)z_{ref}^{-1}} \right|^2 \cdot N^2 \mathcal{L}_{ref}(z_{ref})$$

$$+ \left| 1 - \frac{1}{N} \frac{1 - z_{ref}^{-1}}{1 - z_{osc}^{-1}} \frac{\beta}{1 - (1-\beta)z_{ref}^{-1}} \right|^2 \cdot \mathcal{L}_{osc}(z_{osc}). \quad (21)$$

IV. NUMERICAL VERIFICATION AND DISCUSSION

To verify the introduced formulas: (17) for ADPLL and (21) for CSL/IL, we compare them with their corresponding time-domain behavioral simulation results using Verilog-AMS in Cadence Spectre-AMS Designer [2], [26], [44]. The analytical results [i.e., black curves in Fig. 4(a) and (d)] have a near perfect agreement with the behavioral simulations, thus demonstrating the efficacy of the proposed modeling techniques. For the ADPLL in Fig. 4(a)–(c), we fix the 10 GHz DCO with $K_{\Delta T,dco}/T_{osc} = 10\,\text{ppm/bit}$ and $\gamma N K_{\Delta T,dco} = 50\,\text{fs/bit}$, yet sweep Δt_{tdc} for obtaining different α. The β of CSL/IL in Fig. 4(d)–(f) is set directly. Due to the loop-delay (e.g., $L = \lceil N/2 \rceil + 1$), a large α (i.e., close to 1) will cause "jitter peaking" in the PN plots [see dark-red curve in Fig. 4(a)], introducing possible instability and amplifying the input PN; however, the CSL/IL is unconditionally stable even for $\beta = 1$. The in-band PN in CSL/IL is determined by the reference PN [see Fig. 4(d)], while the ADPLL's PN could be dominated by the TDC quantization noise [see the yellow curve in Fig. 4(a)]. Fig. 4(b) and (e) shows that the theoretically maximum PN bandwidths of the PLL with $L = 1$ and the CSL/IL

are respectively 30% and 44% of f_{ref}.[9] They are much larger than $f_{ref}/2\pi$ (i.e., 16% of f_{ref}) predicted by the conventional s-domain models [34], [60], [63] (which is accurate only when α or $\beta < 0.1$).

The rms jitter [i.e., integration of (17) and (21) from 1 kHz to $f_{osc}/2$] optimized with different α and β is illustrated in Fig. 4(c) and (f) under two noise configurations: 1) dominant purity of the oscillator (i.e., $\sigma_{ref} = 112.5\,\text{fs}$; $\mathcal{L}_{osc}$ @ $10\,\text{MHz} = -140\,\text{dBc/Hz}$), and 2) dominant purity of the reference ($\sigma_{ref} = 35.6\,\text{fs}$; $\mathcal{L}_{osc}$ @ $10\,\text{MHz} = -130\,\text{dBc/Hz}$). To achieve the sub-50 fs jitter, a different optimization strategy is required in each case. While the conventional optimization techniques can be used for the oscillator-purity-dominant ADPLL and IL (CSL) of case #1, case #2 highlights the findings in this brief: the reference-purity-dominant ADPLL and IL (CSL) should push their bandwidths to the remarkably high values corresponding to α & β of 0.2–0.5, well beyond the conventional setting of α & $\beta < 0.1$.

V. CONCLUSION

A frequency synthesizer of ultra-low jitter (i.e., sub-50 fs) is required in the next-generation of wireless and wireline communications. However, as its bandwidth increases, implying that the reference purity becomes more dominant, the current modeling and system simulation techniques fail to accurately predict its performance. A multirate timestamp modeling technique based on "two z-variables" provides an intuitive and powerful tool in understanding, distinguishing, and optimizing these wideband, low-jitter frequency synthesis techniques including high-bandwidth PLLs with high PD/TD-gain and injection locking. ADPLL employing an ADC-based TDC and charge-sharing locking (CSL) are the two promising techniques to reach well into the sub-50 fs jitter.

[9] The bandwidths are obtained by forcing the first term of (17) (excluding $N^2(\mathcal{L}_{ref} + \mathcal{L}_{\Delta q,det})$) and (21) (excluding $N^2 \mathcal{L}_{ref}$) to 1/2. For attempts to reach these limits, we refer to [61] and [62].

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