A Reconfigurable 5-Channel Ring-Oscillator-Based TDC for Direct Time-of-Flight 3D Imaging

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***Abstract*—Time-correlated single-photon counting (TCSPC) 3D imaging requires the digitization of photon arrival times across an array of single-photon avalanche diodes (SPADs). The most critical performance metrics of time-to-digital converters (TDC) in TCSPC applications are their conversion rate (CR), area, and power consumption. This brief presents a multi-channel RO-based TDC architecture whose power consumption scales with its configurable resolution for power-sensitive applications. Further power savings are achieved by sharing one RO among multiple TDC channels. We have demonstrated that sharing one RO among five channels reduces the power consumption by more than 75% relative to non-shared architectures. Here, a 5-channel 12-bit TDC is fabricated in 65 nm CMOS with an area of 1920 um^2 per channel. It demonstrates CR up to 125 MHz and offers a resolution configurable over the range of 24–133 ps. At a CR of 125 MHz, the TDC power consumption per channel is 0.1 mW and 1 mW per channel at 133 ps and 24 ps resolution, respectively.**

***Index Terms*—Counter, data converter, LiDAR, ring oscillator, single-photon avalanche diode (SPAD), time-correlated single-photon counting (TCSPC), time-of-flight (ToF), time-to-digital converter (TDC).**

I. Introduction

IN TYPICAL single-photon avalanche diode (SPAD)-based solid-state direct time-of-flight (ToF) systems, shown in Fig. 1 [1], each of the SPAD's detections requires time-stamping to measure the distance to the reflective target. The output of each SPAD in time-correlated single-photon counting (TCSPC) systems is a sequence of pulses coinciding with the first photon arrival within each repetition period, T_{mod}. Typically, less than one photon is detected per SPAD per repetition period. Hence, time-to-digital converters (TDC) can be shared among several SPADs to reduce the circuit area and power consumption [2].

Analyzing SPAD-based TCSPC systems reveals tradeoffs between the TDC parameters and the measured distance accuracy [2], [3]. Considering these tradeoffs reveals the most critical performance metrics of TDCs in TCSPC applications: their conversion rate (CR), area, and power consumption. Increasing the CR affords an increased 3D imaging frame rate. It also allows each TDC to be shared among more SPADs, which minimizes the overall TDC area. Minimizing the area and power consumption permits the integration of all TDCs on the 3D imager system-in-package (SiP).

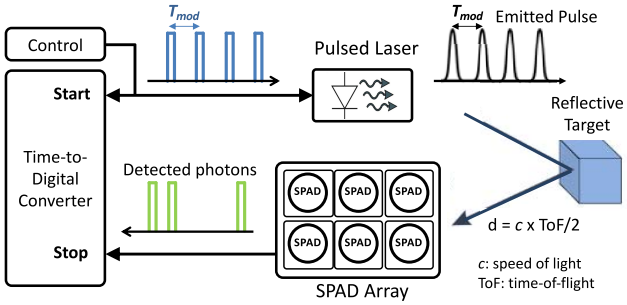

Fig. 1. A typical SPAD-based TCSPC 3D imaging system block diagram; a pulsed laser illuminates the target and an array of SPAD photo-detectors (pixels) detect the received light with single-photon sensitivity. The time-to-digital converter digitizes the photon time-of-flight (ToF).

This brief focuses on ring-oscillator (RO)-based TDCs since they offer a number of advantages over other TDC types for application in TCSPC imaging systems [4], [5]. In this brief, we present an architecture based on RO sharing that offers lower power consumption and smaller area than non-shared RO schemes. The counter doesn't consume a dominant portion of the total power, and sharing the counter between channels adds to the complexity with little benefit in the area or power saving. The presented TDC power consumption scales with resolution by simply changing the RO frequency. Having a configurable system increases the TCSPC modules' versatility and is particularly beneficial for power-sensitive applications such as hand-held devices. We demonstrate the architecture with the design of a five-channel TDC with a shared RO. Section II briefly establishes the requirements on TDCs for SPAD-based TCSPC systems. Section III studies the design of a multi-channel TDC with configurable resolution and scalable power for TCSPC applications. Section IV describes the test and measurement results of the prototype five-channel TDC.

II. Background: Multi-Channel TDCs

TDCs have a much slower CR requirement than the shared case in per-pixel TDC architecture. The choice between shared or per-pixel TDC depends on the system and application. High background noise in a LiDAR system necessitates increasing throughput at lower power, favoring the shared approach [2], [6]. Multi-channel TDCs are attractive for SPAD imaging arrays [7], [8]. An analysis of TDC-sharing in TCSPC systems [2] has shown that when using a TDC with a specific CR, there is an optimum number of TDCs for each application scenario, above which the area and power consumption will

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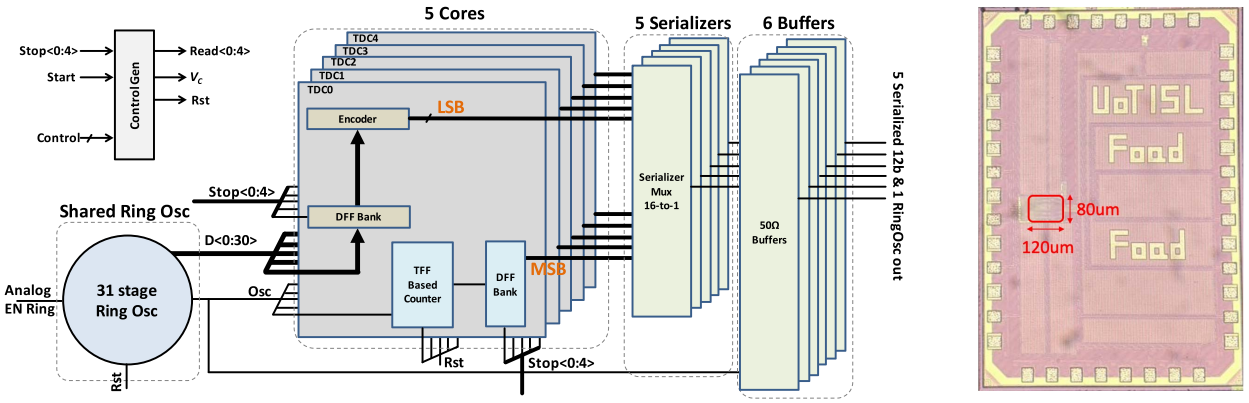


Fig. 2. (a) The arrayble RO-based 5-channel TDC structure consisting of a shared gated ring oscillator and five counters. (b) Microphotograph of the proposed TDC fabricated in 65nm CMOS technology with an active area of 120×80 μm^2, excluding serializers and buffers.

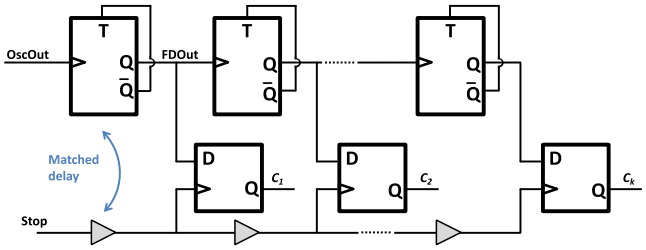


Fig. 3. Counter schematic along with the sampler: the delay cells in the sampler ensure the propagation of the counter has ended before sampling.

increase without enhancing the TCSPC accuracy. The size of the SPAD array connected to the shared TDC and the rate of incoming detections from each SPAD in the array prescribe the required number of TDC channels. For a typical TCSPC application similar to [2], in the TDC sharing scheme (when the TDC is shared among 8×8 SPADs), a 5-channel TDC with CR more than 100 MHz or a single-channel TDC with CR more than 610 MHz is required to achieve at least 50% of the maximum achievable histogram signal-to-noise ratio (3dB penalty) [2].

TDC array power consumption grows with the number of SPADs and photon arrival rate and eventually becomes a limiting factor in design. For example, a 3D SPAD array imager with QVGA resolution (320×240) implemented with per-pixel TDCs and a 2 W power budget for the sensor requires that each TDC consume less than 2/(320×240) = 26 μW. TDC sharing can alleviate the power requirement. Under measurement conditions similar to [2], satisfying the same power budget of 2 W while utilizing a 5-channel TDC shared among 8×8 SPADs requires 26×(8×8)/5 = 333 μW per TDC channel.

III. Five-Channel Configurable RO-Based TDC Design

Figure 2(a) shows the proposed configurable arrayble RO-based TDC structure for SPAD-based TCSPC applications. The last delay stage of the voltage-controlled RO (VCRO) interfaces with a counter. This design uses an asynchronous counter, shown in Fig. 3, consisting of a cascade of toggle flip-flops (TFF) as frequency dividers (FD). Although there is no propagation delay in synchronous counters, and they can offer faster operation than asynchronous counters, they require extra logic [9]. In this design, all FD stages are identical. It may be tempting to downscale the FD stages as the frequency halves after each stage. However, scaling down the divider stages in proportion to their input frequency increases their jitter [10]. The counter output is sampled to obtain the coarse time measurement MSBs. The state of the ring oscillator is sampled and encoded into the LSBs.

The number of coarse and fine bits provides a tradeoff between the area and power of the ring and counters that determines the number of stages in the ring oscillator. In this section, we consider the tradeoffs between the number of delay stages in the RO, N, and the counter size for a given total TDC resolution, 12 bits in this case. Decoding the ring multi-phase outputs yields $N_f = \log_2(N+1)$ fine bits. The power consumption of the proposed 12-bit TDC structure with a shared ring oscillator, P_{TDC}, is dominated by the power of the ring oscillator, P_{Ring}, counter, P_{Counter}, and time-sampling D-type flip-flop banks, P_{DFF}, as follows (see Fig. 2(a)):

$$P_{\text{TDC}} \approx P_{\text{Ring}} + P_{\text{Counter}} + P_{\text{DFF}}. \tag{1}$$

The power consumption of the ring with $N = 2^{N_f} - 1$ stages, which oscillates at f_{osc}, is a function of the state transition energy, E, and the average time required to charge/discharge the multi-phase output, $2t_D$, but it is independent of the number of delay stages,

$$P_{\text{Ring}} \approx f_{\text{osc}} \cdot N \cdot E = E/2t_D. \tag{2}$$

The similar toggle flip-flop (TFF)-based FD stages in the counters need E_{TFF} energy to change state for a single clock edge. With n_{ch} representing the number of the TDC channels, the five counters (one counter per TDC channel) draw power proportional to their parasitic capacitances and the RO frequency,

$$\begin{aligned} P_{\text{Counter}} &= n_{\text{ch}} \cdot f_{\text{osc}} \cdot \sum_{k=1}^{12-N_f} \frac{E_{\text{TFF}}}{2^k} \\ &= 5 \cdot \frac{1}{2 \cdot \left(2^{N_f} - 1\right) \cdot t_D} \cdot E_{\text{TFF}} \left(1 - \frac{1}{2^{12-N_f}}\right) \end{aligned} \tag{3}$$

Faster TFFs in the counter require more area and power, hence larger E_{TFF}, but allow for fewer delay stages in the ring

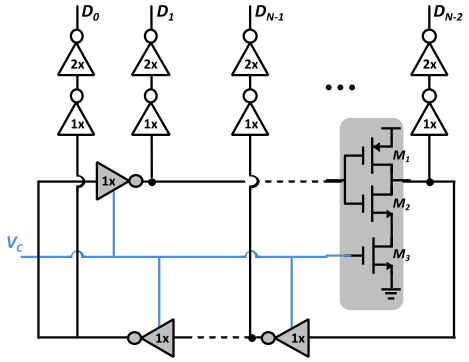


Fig. 4. Ring oscillator schematic: the output of the gated inverter is loaded with one same-sized inverter of the next stage and one buffer.

oscillator, N, which we shall see reduces power consumption in the sampling flip-flops, P_{DFF}. The sampling flip-flops consume an energy of E_{DFF} for each clock edge are connected to the counters' output and the multi-phase output of the RO to sample the stop-time. Their power consumption depends also on the frequency of the stop signal, f_{stop},

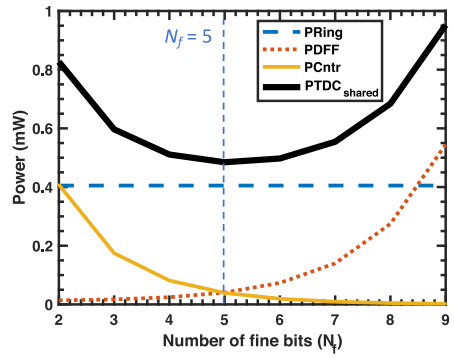
$$P_{\mathrm{DFF}} = n_{\mathrm{ch}} \cdot f_{\mathrm{stop}} \cdot \left\{ \sum_{k=1}^{N} E_{\mathrm{DFF,Ring}} + \sum_{k=1}^{12-N_f} E_{\mathrm{DFF,Counter}} \right\} = 5 \cdot f_{\mathrm{stop}} \cdot E_{\mathrm{DFF}} \cdot \left\{ \left(2^{N_f} - 1\right) + 12 - N_f \right\}. \quad (4)$$

Substituting (2), (3) and (4) in (1) gives an expression for the 12-bit 5-channel TDC power consumption as a function of N_f. The designer can use this expression to choose the number of stages in the ring.

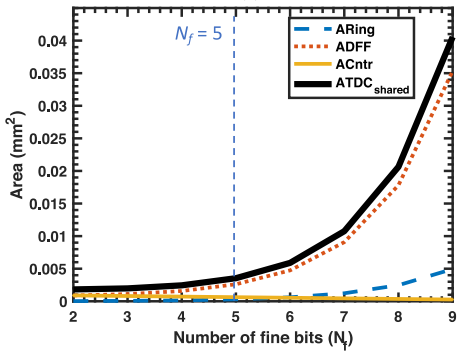
When sharing a RO, the RO needs to drive more counters/DFFs, 5× in this case, and thus requires more buffering and more drive strength than if each channel had its own RO. The drivers' power consumption and propagation delay eventually limit the RO sharing benefits for an increased number of channels. The multi-phase output of the ring oscillator interfaces with the counter and sampling flip-flops through a two-stage buffer with an overall size almost three times the area of the RO delay element A_{Inv} (see Fig. 4). The core area of the corresponding 12-bit 5-channel TDC comprising the stop-time sampling flip-flops with an area of A_{DFF} and the counter TFFs with an area of A_{TFF} is approximately

$$A_{\mathrm{TDC}} \approx 4\left(2^{N_f} - 1\right)A_{\mathrm{Inv}} + 5\left\{\left(2^{N_f} - 1\right) + 12 - N_f\right\}A_{\mathrm{DFF}} + 5\left(12 - N_f\right)A_{\mathrm{TFF}}. \quad (5)$$

An increase in N_f contributes to greater area and power consumption of the sampling flip-flops (P_{DFF}) but results in a lower ring oscillation frequency and a lower number of coarse bits reducing the counter area and power (P_{counter}). The tradeoffs depend on the constituent subcircuit designs and the CMOS technology node via E_{DFF}, E_{TFF}, A_{DFF}, A_{TFF}, A_{INV}, etc. For this design in 65nm CMOS, the results in Fig. 5 show that $N = 31$ stages in the ring (corresponding to $N_f = 5$ fine bits) provides the lowest overall power with very little increase in area compared to the minimum-area architecture. Sharing the ring oscillator among the TDC channels reduces the power consumption by more than 75% and area by more than 25% compared to non-shared architecture.



(a)



(b)

Fig. 5. The choice of the number of stages in the ring oscillator: (a) estimated total power consumption of the 5-channel TDC with a shared ring oscillator versus the number of fine bits (N_f); the minimum is around five fine bits. (b) Estimated total area of the 5-channel TDC with a shared ring oscillator versus N_f; the total area of the DFF grows dramatically as N_f increases. $N_f = 5$ is chosen.

IV. Test Setup and Measurements Results

A. TDC Operation

An on-chip control signal generator circuit generates the reset (*Rst*) and enable signals (V_C) from the rising edge of the *Start* signal. The *Rst* signal resets the gated RO's internal state to a pre-set value. The ring-enable signal, V_C, activates the ring and controls the frequency of the oscillation by manipulating the gate voltage of NMOS transistor M3 in Fig. 4. SPAD array output pulses generate *Stop* signals corresponding to photon arrivals in a TCSPC system (see Fig. 1). The TDC CR should be high enough to digitize the SPAD array output pulses reliably [3]. In the measurement setup, a repetitive signal with a frequency of f_{stop} triggers the *Stop* of the TDC channels and emulates the SPAD output pulse where $1/f_{\mathrm{stop}}$ represents the minimum time expected between photon arrivals. The control signal generator circuit creates a sequence of *Read* pulses corresponding to the rising edge of the *Stop* signal to latch the output state of the RO and the counter sampling DFF bank in Fig. 2(a).

It takes some time for the clock transition to propagate to the last FD stage of the counter. Moreover, the asynchronous divider sends out the 7 bits with different delays. There is a retiming stage to ensure proper sampling of the asynchronous counters. The frequency of the Stop signal, f_{stop}, is the TDC CR. The pad-limited design includes one 16:1 multiplexer-based 2 Gbps serializer per TDC channel to serialize the 12-bit parallel outputs of each channel. A 50 Ω buffer transmits the serialized data off-chip. Post-layout simulations confirm that

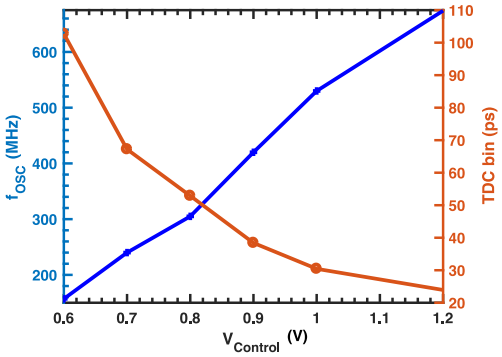


Fig. 6. The V_C voltage controls the oscillation frequency of the RO, offering a measured average gain of 861 MHz/V when it is swept from 0.6 to 1.2 V.

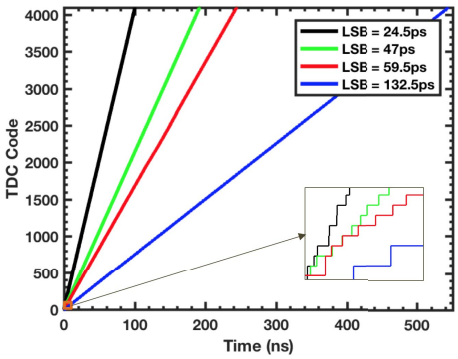


Fig. 7. Output characteristics of the configurable TDC when the LSB width is set to 24.5 ps, 47 ps, 59.5 ps, and 132.5 ps.

the TDC CR can go up to 1 GS/s, which would require a serializer capable of operating at 16 Gbps. It is worth mentioning that an interface circuit can dynamically allocate the free TDC channels to the incoming stop pulses, for instance, in a daisy chain approach [11]. This architecture can handle even coincident events as the channels are independent. It can digitize a stop pulse sequence with a rate of 1 GHz per channel, totaling 5 GHz for the five-channel TDC.

B. TDC Prototype Measurement

Figure 2(b) shows a microphotograph of the proposed 5-channel TDC fabricated in 65 GP CMOS technology. The chip occupies an active area of 120 µm x 80 µm, excluding the serializers and output buffers. The analog V_C voltage controls the oscillation frequency of the VCRO and, hence, the TDC resolution. The controllable TDC resolution offers a means to scale the range, resolution, and power consumption of the TCSPC system dynamically. The measured average gain of the VCRO is 861 MHz/V when V_C is swept from 0.6 to 1.2 volts, as shown in Fig. 6, which matches the post-layout SS-corner simulation results. Locking the VCRO to a PLL whose core oscillator is a replica of the same VCRO can improve the nonlinearity of the VCRO to gain linearity exceeding 99% [5]. This approach can also help to mitigate the process, voltage supply, and temperature (PVT) variations on the time accuracy of the TDC. With a variable resolution from 20 to 130 ps, the 12-bit TDC can cover maximum ranges from 12 to 80 meters.

Figure 7 shows the configurable TDC's output characteristics when the LSB is set to 24.5 ps, 47 ps, 59.5 ps, and 132.5 ps. The standard deviation of the corresponding DNL and INL in the presence of interference from other channels, normalized to one LSB, are 0.95 and 1.87, 0.54 and 1.51, 0.55 and 1.5, and 1.58 and 2.89, respectively (Fig. 8). The measured ToF accuracy in [12] and [13] is 0.4% and 0.34%, respectively, which shows that TDC nonlinearity (INL, DNL) is not the dominant source of error. A 0.1 ns precision corresponds to 1.5 cm, and 0.1 ns over 100 ns means a distance measurement error of 0.1%. This is a relaxed INL/DNL requirement on the TDC design. The TDC can adapt to power-sensitive applications by trading resolution for power. At the CR of 125 MHz per channel, it consumes 1.03 mW per channel at a time resolution of 24.5 ps when the RO is running at 660 MHz and 0.11 mW per channel at a time resolution of 132.5 ps when the RO is running at 122 MHz.

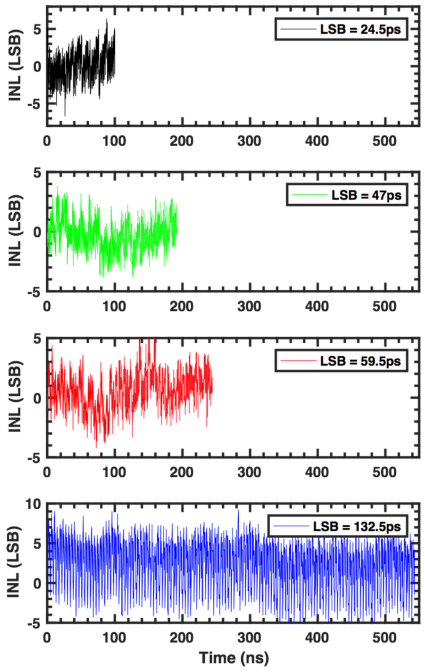


Fig. 8. TDC INL for LSB of 24.5 ps (σ = 1.87 LSB), 47 ps (σ = 1.51 LSB), 59.5 ps (σ = 1.5 LSB), and 132.5 ps (σ = 2.89 LSB).

Table I provides a comparison with other state-of-the-art TDCs. The design in [14] uses a 12-stage RO with pseudo-differential delay cells along with a voltage-to-time converter (VTC) to implement an ADC/TDC multiplex LiDAR system consuming over 5 mW. The VTC block uses a charge-current and-capacitor-based architecture and takes almost half of the reported area. An interpolator and the corresponding DFFs are utilized to improve the LSB. The authors report a marginally acceptable CR (500 MHz compared to the required 610 MHz) with 7× more power consumption and 30× the TDC area than ours. The LSB and power are not configurable. The 12-bit TDC in [11] uses a 4-stage RO architecture with a differential gated inverter for the delay stage. The ring oscillator is not shared among the counters. Although it consumes almost the same power as the proposed TDC, the CR is lower by more than one order of magnitude, failing to satisfy the required CR mentioned in Section II. It occupies double the area, and the LSB and power are not configurable. The designs in [12] and [13] operate at lower CR than required,

TABLE I
COMPARISON OF STATE-OF-THE-ART RO-BASED TDCS FOR RANGING APPLICATIONS

Ref	Tech (nm)	CR (MHz)	LSB (ps)	Range bits	Range ns	DNL (ns)	INL (ns)	Power per Ch. (mW)	Area per Ch. (um²)
This Work	**65**	**125 (1000[a])**	**24.5**	**12**	**100**	**0.103[b]**	**0.15**	**1.03[c]**	**1920**
			47		**193**	**0.119[b]**	**0.15**	**0.33[c]**	
			59.5		**244**	**0.172[b]**	**0.27**	**0.28[c]**	
			132.5		**543**	**0.834[b]**	**1.09**	**0.11[c]**	
TCAS I '19 [14]	65	500	6.25	15	205	0.002	0.007	5.2	60000
JSSC '19 [11]	180	40[d]	48.8	12	200	0.023	0.081	0.3	4200
JSSC '19 [12]	65[e]	-	61-204	14	999-3342	0.061-0.204	0.183-0.612	0.5–0.2[f]	550[g]
JSSC '19 [13]	40[e]	-	35/560	14/4	560-1600	0.002-0.028	0.004-0.056	-[h]	150[g]

[a] CR is 1 GHz in post-layout simulations. The 2-Gbps serializer in this prototype limits measurements to 125 MHz. [b] 0.1 ns precision corresponds to 1.5 cm, and 0.1 ns over 100 ns means a distance measurement error of 0.1%. [c] Power consumption at f_{stop} = 125 MHz, based on (4), the power consumption depends on f_{stop} [d] Inferred from the measurement setup [e] Stacked technology [f] Measured at f_{stop} = 2 MHz [g] The reported area is just the RO and counter. The sampling, encoder and digital circuits are not included. [h] Not reported; The RO alone consumes 6.8 mW and the power consumption of the whole sensor including TDCs, the laser and SPAD array is 77.6 mW

which would limit the frame rate. A decision tree with a dead-time of less than 2.4 ns preceding the TDC manages photon detection in [12]. A 10-bit asynchronous counter sampler uses DFFs allowing the counter to operate more than twice as fast as the high-speed 0.98 GHz clock from the RO. The latency of the 10-bit asynchronous counter sampler alone will limit the CR to less than 196 MHz. Adding the latency of the RO state decoder in their design will further limit the CR. The laser repetition rate in measurements is set to 1 MHz. In-pixel histogram measurements in [13] show around 80 counts with 60k laser repetitions per histogram. It suggests that the conversion rate for the TDC must be greater than 4.8 MHz. The RO alone consumes 6.8 mW [13]. The reported area in [12] and [13] excludes the sampling, encoder, and other TDC digital circuits and includes only the RO and counter. Thus, this brief is the only TDC to provide the required CR while satisfying the power consumption and other specifications mentioned in Section II. It is configurable and, thanks to its architecture, easily arrayble.

V. CONCLUSION

This brief shows how the resolution is traded for power savings, providing a family of results that adapt to application necessities. A 5-channel 12-bit TDC is presented in 65 nm CMOS. A control voltage allows the RO frequency to be decreased, thereby increasing the full-scale range and decreasing the power of the TDC to adapt to longer range or power-sensitive applications. We investigate the tradeoffs governing the number of stages in the ring, N. Although increasing N results in a lower counter activity rate and fewer required bits in the counter, it requires a greater area and higher power consumption for the state-sampling flip-flops. Adding more counter stages increases the number of TDC bits with negligible increase in area and power consumption. An analysis of the tradeoffs between area, power consumption and the number of coarse bits in the counter and the N_f fine bits extracted from the state of the ring oscillator ultimately determines the number of stages in the ring oscillator. As a result of our analysis, a configurable 5-channel RO-based TDC with 31 delay stages in the ring is designed in 65 nm CMOS technology. Sharing the ring oscillator among the five TDC channels reduces the power consumption by more than 75% and area by more than 25% relative to non-shared architecture.

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