A 38.6-fJ/Conv.-Step Inverter-Based Continuous-Time Bandpass ΔΣ ADC in 28 nm Using Asynchronous SAR Quantizer

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***Abstract*—We propose a self-biased inverter-based amplifier for realizing a high-speed low-power second-order single-loop continuous-time bandpass delta-sigma modulator (CT-BP-ΔΣM). The design is amenable to nanoscale CMOS and exploits a single self-biased pseudo-differential inverter with a positive feedback to replace conventional op-amps used in an integrator configuration. The modulator also uses a 5-bit asynchronous successive approximation register (ASAR) quantizer. With a 30 MHz bandwidth at 400 MS/s sampling rate and 100 MHz intermediate frequency (IF), the modulator achieves 61 dB dynamic range (DR) and 58 dB SNDR while consuming 2.5 mW from a 1V supply. The core area in 28 nm LP CMOS is 0.04 mm^2. A 38.6 fJ/conv.-step figure of merit is achieved.**

***Index Terms*—ADC, asynchronous successive approximation register (ASAR), bandpass, continuous-time (CT), delta-sigma modulator (ΔΣM), inverter-based, single-loop.**

I. Introduction

HIGH-SPEED, high-resolution and low-power analog-to-digital converters (ADC) in low-voltage nanoscale CMOS are in great demand by modern broadband wireless communication systems and IOT applications [1]. Continuous-time delta-sigma modulators (CT-ΔΣM) are attractive as they promise to fulfill requirements of such systems. CT-ΔΣM provides significant power savings due to reduction of bandwidth requirements of its circuitry as compared to the alternative switched-capacitor (SC) implementations [2]. It also offers a high dynamic range (DR) and implicit anti-aliasing [3]. However, with the deep scaling of CMOS technology, the resulting low supply voltage has put significant challenges on the ADC circuit design. Specifically, the operational transconductance amplifier (OTA) is now a bottleneck in filter designs typically used in ΔΣM [4], [5]. There are some reported attempts to resolve these problems [4]–[10]. Reference [4] proposes an inverter-based SC circuitry. Digitally assisted OTAs [6], comparator-based SC circuits [7] and dynamic amplifiers [10] are some other techniques to overcome the OTA limitations. In [8], a new power reduction technique inserts a low-pass filter (LPF) in front of the modulator's loop filter (LF) to eliminate high-frequency components in the loop. However, the LPF changes the noise transfer function (NTF) and signal transfer function (STF) of the ADC. As a result, one more compensation element for restoring NTF and STF is needed. Using a single-amplifier biquad structure in the loop filter is another power reduction solution employed in [9].

Reference [11], [12] present a single op-amp resonator as a filter for a bandpass (BP)-ΔΣM. An advantage of that approach is the use of only one op-amp to reduce the loop noise. However, the most significant drawback is high power and area consumption. To alleviate that issue, [13] replaces the op-amp with a digitally assisted biasing inverter at a cost of increased circuit complexity. Reference [5] introduces a ring amplifier (RA) by employing stabilization techniques to overcome instability and performance issues due to the lack of periodic reset.

The goal of this brief is to implement the modulator with a single-stage op-amp to overcome the wasting of power and bandwidth of the prior-art solutions. Consequently, we propose to replace the traditional resonator in the continuous-time bandpass delta-sigma modulator (CT-BP-ΔΣM), as presented in [12], with a self-biased inverter-based resonator in order to significantly reduce the power and silicon area. Compared to [14], which proposes the fully differential inverter-based op-amp with extra circuits to bias common-mode output voltages and separate supply voltages for fine-tuning of the dc gain of the integrators (Q tuning), the proposed architecture eliminates the use of extra stages by employing a self-biasing technique [15], [16]. Reference [17] employs the amplifier from [16] in the SC LPF ΔΣM. Being completely complementary and self-biased results in better reliability to process, voltage, and temperature (PVT) variations.

In [1], the single op-amp resonator is burdened by many passive components. Here, we propose a 2nd-order architecture merging the positive feedback with a high-pass filter (HPF) in order to reduce the number of burdensome components.

A lower clock frequency of the ΔΣM, and thus significant power savings, can be obtained by lowering its oversampling ratio (OSR). To that effect, we employ a multibit quantizer via a SAR-assisted technique [18]. To further improve the quantizer, we turn the synchronous SAR into an asynchronous SAR (ASAR) architecture so that it can operate at a lowered clock frequency, while still satisfying the required conversion time [19].

As a proof of concept, a new 2nd-order self-biased inverter-based CT-BP-ΔΣM employing a 5-bit ASAR quantizer is

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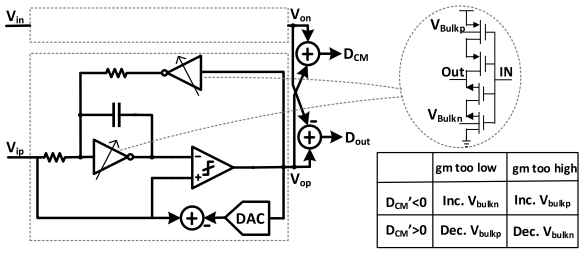

Fig. 1. Inverter-based modulator presented in [13].

realized in 28 nm CMOS. It achieves 38.6 fJ/conv.-step at 400 MS/s sampling frequency and 30 MHz bandwidth, while consuming only 2.5 mW.

The rest of this brief is as follows. Section II discusses the architecture considerations and comparison with previous works. Section III introduces details of the circuit design. In Section IV, the measurement setup and results are described.

II. System Design

A. Traditional Architectures

The simplified diagram of an inverter-based modulator is shown in Fig. 1 [13]. The main issue is biasing of the inverter, which is done digitally. Such digitally assisted controlling of the bias increases the overall complexity, area, and power. The digital algorithm (shown in the accompanying table) explains how the D_{CM}' (inversion of D_{CM}) controls the backgate of the PMOS and NMOS (V_{bulkp} and V_{bulkn}) transistors of the inverters.

The second issue is the 1-bit quantizer which tends to reduce the overall linearity due to its sensitivity to jitter, especially in comparison with multi-bit quantizers.

The third issue is related to the output common-mode voltage of the introduced pseudo-differential modulator. It is defined by two single-ended quantizer DAC feedback loops and is not constant. Hence, achieving high CMRR is possible by subtracting the output voltages in the digital domain.

In [11], a 4th-order modulator based on a single op-amp resonator per each of the two 2nd-order filters was introduced. That architecture promotes simplicity by avoiding the multiple feedback paths per resonator. However, designing op-amps in highly scaled CMOS appears to be increasingly difficult and they tend to rather consume excessive power for IOT applications. Furthermore, the center frequency of the modulator changes due to PVT variations and mismatch of passive components. Calibrating the capacitors maintains the center frequency and quality (Q) factor of the modulator. It is carried out by a 4-bit digitally controlled capacitor bank in parallel with each main capacitor of the modulator.

B. Proposed Architecture

Fig. 2 illustrates a block diagram of our proposed ADC topology. It is based on a ΔΣM assisted by a 5-bit ASAR quantizer.

The NTF of the design for an ideal 2nd-order loop filter is expressed as:

$$NTF = \frac{s^2 + \omega_0^2}{s^2 + \omega_0 s + \omega_0^2} \tag{1}$$

The ΔΣ DAC is a 5-bit current-mode DAC including the cascaded switch drivers, latches and current cells as used in [18].

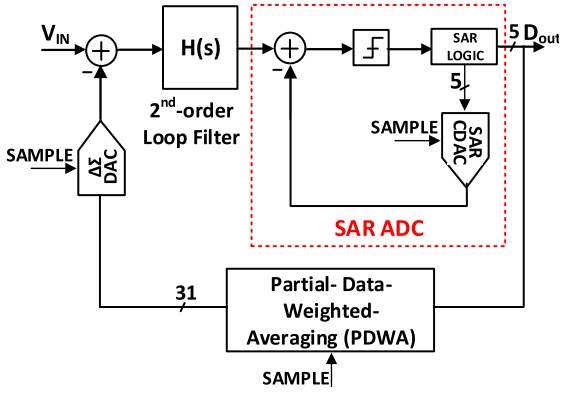

Fig. 2. Block diagram of the proposed ASAR ΣΔ modulator.

The innovation here lies in the 2nd-order loop filter employing self-biased pseudo-differential inverter-based op-amp, which is explained in next section.

III. Circuit Implementation

A. Inverter-Based Resonator

Reference [20] proposed a self-biased noncomplementary differential op-amp, while externally biased but fully complementary differential op-amp was proposed in [21]. In contrast to these op-amps, the presented architecture incorporates both self-biasing and fully complementary configurations. The new scheme is applied in a resonator to achieve lower power consumption and smaller area.

The proposed differential configuration of the 2nd-order resonator based on a pseudo-differential inverter is shown in Fig. 3(a). The architecture is configured as a LPF but it also merges an HPF into its positive feedback to realize a high Q-factor resonator that allows optimizing the NTF zeros for a maximum SNR. By this configuration, the resonance condition and the Q-factor depend just on the values of passive components [11]. The transfer function of this resonator

$$H(s) = \frac{R_1 C_1 \omega_0^2 s}{s^2 + (R_2 C_2 + R_1 C_1 - R_2 C_1)\omega_0^2 s + \omega_0^2} \tag{2}$$

is same as an ideal 2nd-order resonator if $R_2C_2 + R_1C_1 - R_2C_1$ equals to zero and $R_{in} = R_2$. By this condition, it starts to resonate. If we further restrict $R_2 = 2R_1$, $C_1 = 2C_2$, we can construct an ideal 2nd-order resonator with a resonant frequency $\omega_0^2 = \frac{1}{R_1 C_1 R_2 C_2}$.

Mismatch of the passive components can affect the resonant frequency; as a result, the center frequency of the CT-BP-ΔΣM and the quality factor change. Only the calibration of capacitors is sufficient to set the center frequency [11].

Fig. 3(b) shows the structure of pseudo-differential inverter, which employs a self-biasing technique. The input stage comprises input pairs ($M_{1\text{-}4}$) with stacked biasing transistors ($M_{5\text{-}8}$) which control the output common-mode (CM) level.

This structure avoids using an externally driven biasing. The self-biasing transistors are connected to the main amplifier to reduce the effects caused by PVT and CM variations. For instance, if V_{DD} increases, the gate-source voltage of M_7, $|V_{gs7}|$, first increases. Then, the bias current flowing through M_7 and M_5 also increases. This causes the current to increase in the input transistors, thus raising the output voltage. As a result, the output voltage forces V_{sg7} and its current returning to their initial values. Consequently, the V_{DD} variations will

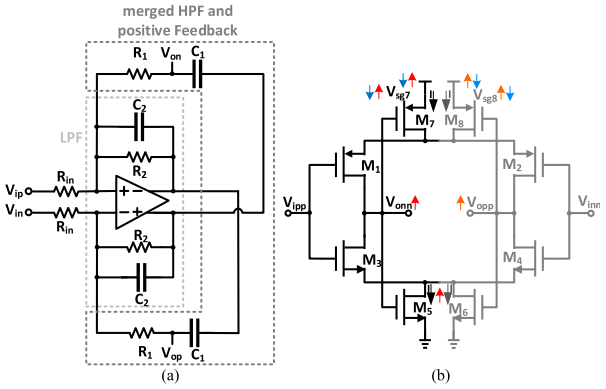

Fig. 3. (a) Differential configuration of the pseudo-differential inverter-based resonator. (b) Pseudo-differential inverter and operational principle of compensating for supply voltage variations.

TABLE I
OUTPUT CM LEVEL UNDER PVT VARIATIONS

Corners	tt	sf		fs		ss		ff	
Supply voltage (V)	1	1.01	0.99	1.01	0.99	1.01	0.99	1.01	0.99
Tempreature (°C)	85	-40	125	-40	125	-40	125	-40	125
Output CM (mV)	696	684 707	684 707	680 699	680 699	681 702	681 702	681 704	681 704

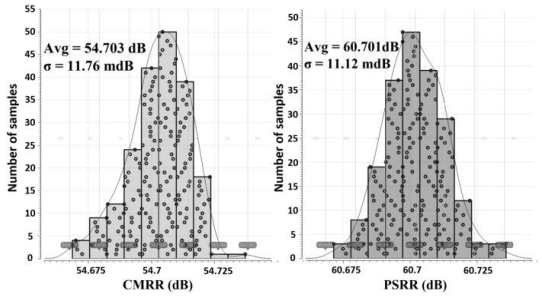

Fig. 4. CMRR and PSRR due to mismatch.

be largely compensated. The red arrows in Fig. 3(b) show immediate responses to the increases in V_{DD} and the blue lines indicate the circuit's eventual compensation. V_{ipp}, V_{inn}, V_{opp}, and V_{onn} are the positive and negative inputs and positive and negative outputs of the inverter, respectively. Table I verifies the output CM level stability over PVT variations. In addition, Monte Carlo simulations of PSRR and CMRR due to mismatch are shown in Fig. 4. Two open-loop buffers (two cascaded inverters, each) are connected to the outputs of the resonator to prevent kickback noise from the SAR quantizer.

B. 5-Bit ASAR–Based Quantizer

Fig. 5 shows the asynchronous SAR (ASAR)-based quantizer. A 5-bit ASAR ADC with a monotonic switching technique [19] is employed. The top four MSBs, C_1-C_4, are divided into two equal sub-capacitive arrays (see Fig. 6) and each differential array switches in complementary directions. This keeps the input CM voltage of comparator fixed, which reduces the signal-dependent dynamic offset of the comparator [22].

A bootstrapped switch can alleviate the clock feedthrough [3]. The unit capacitor C_u is a 5 fF finger-type capacitor. The total sampling time for the ASAR operation is 0.2 of clock cycle. The main building blocks of the ASAR control logic are the two D flip-flop (DFF) arrays. The lower DFF chain (shift register) generates an internal phase ($CK_1 \ldots CK_N$) to drive the upper DFF array (DAC register) to control the switches of DAC capacitors. CMP_OP is a positive

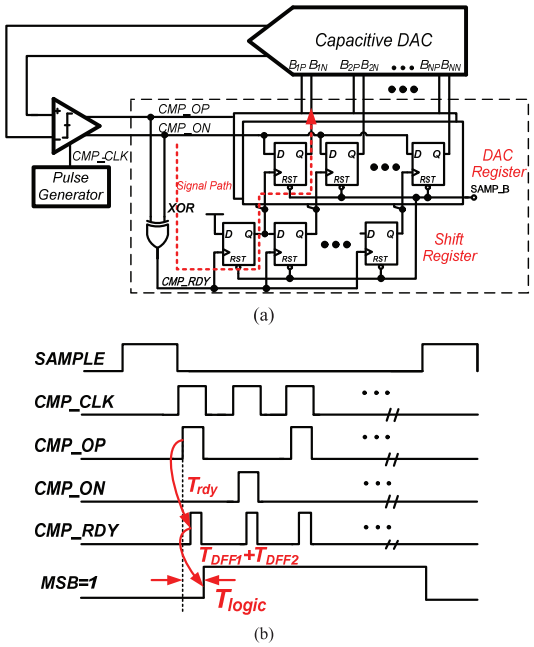

Fig. 5. (a) Simplified block diagram, (b) timing sequence of the SAR quantizer.

output of the comparator while CMP_RDY is a ready signal when the comparison is done. The comparator is triggered to operate on the rising edge of CMP_CLK. When the reset signal SAMP_B (inverse of the external clock signal, SAMPLE) is low, the control logic block will be reset and the input bootstrapped switches will track the input. When the tracking phase is about to be finished, SAMPLE goes down forcing CMP_CLK to transition from 0 to 1, thus triggering the first comparison after which CMP_RDY is generated. According to the outcome of the comparator, the first DFF of the DAC register generates the control signals (B_{1P} and B_{1N}). This complementary signal will control the connecting direction of the DAC capacitor. After that, CMP_CLK goes up again and the next comparison begins. The conversion sequence goes on until finally the LSB is determined. The asynchronous control logic helps the SAR ADC to operate efficiently in such a way that after each sampling, the ADC works with an internal timing sequence. Thus, the circuit does not have to wait for the synchronous clock to trigger each bit conversion. When the conversion cycle finishes, the whole circuit simply goes to sleep awaiting the next sample. The maximum delay of the SAR logic is formulated as:

$$T_{SAR\_logic} = T_{XOR} + 2T_{DFF} + T_{NAND} \tag{3}$$

where T_{XOR} is an XOR gate delay, T_{DFF} is a DFF delay of the shift and DAC registers, and T_{NAND} is a NAND gate (connected to CDAC switches in Fig. 6) delay. To reduce the SAR logic delay and, as a result, to increase the SAR speed, it is imperative to prioritize the designs of TSPC ("true single-phase clock") DFFs, customized XOR and NAND according to the required driving capacity.

C. DAC

A current-steering DAC is used to achieve lower thermal noise as compared to a resistor ladder DAC. It uses non-return-to-zero (NRZ) to have a better protection against clock jitter. However, matching of current sources is important for the linearity and, regardless of the resonator performance, can

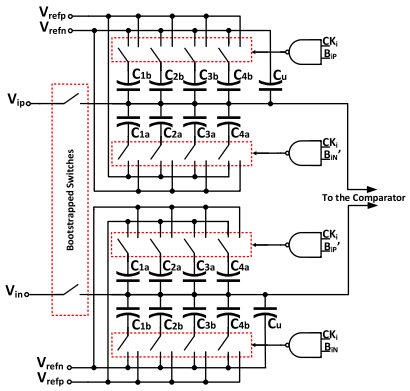

Fig. 6. Block diagram of a 5-bit capacitive DAC configuration of ASAR quantizer.

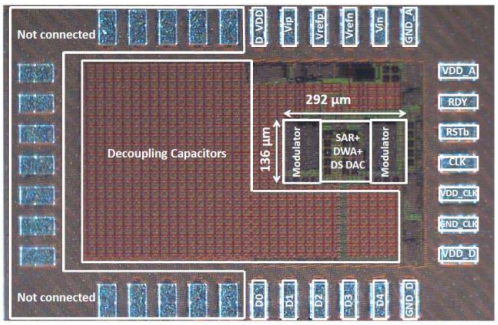

Fig. 7. Chip micrograph.

introduce nonlinearity into the system. Partial data-weighted-averaging (PDWA) is employed to reduce the non-linearity, albeit it increases the complexity and power consumption. The PDWA includes a binary-to-thermometer decoder, barrel shifter, binary decoder and register [18].

IV. Experimental Results

The 2nd-order CT-BP-ΔΣM ADC was fabricated in TSMC 28nm LP CMOS. Fig. 7 shows the chip micrograph. The core area, excluding the bonding pads, decoupling capacitors, and I/O drivers, is 0.04 mm^2. Decoupling capacitors fill the unused area to reduce noise between power supplies and ground. The power supply is 1 V. The chip has 19 pins and is mounted on a customized PCB board.

A. Measurement Setup

The input test signal is fed to the PCB through an SMA connector. It is then passed through a single-ended to differential balun. A single-pole RC filter is placed between the ADC driver outputs and the ADC inputs to reduce noise contribution due to the driving circuitry. A customized power board generates the required power supply and reference voltages for analog and digital parts and drives the on-chip voltage buffers. The measurement setup is shown in Fig. 8. A 400 MHz clock is generated by a data pattern generator. The digital output data streams and clock signal are captured by a logic analyzer. These streams are then exported into MATLAB and processed to compute the Fast Fourier Transform (FFT).

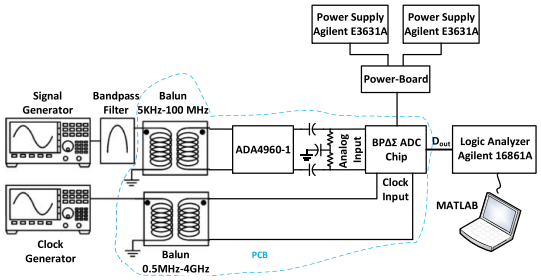

Fig. 8. Measurement setup.

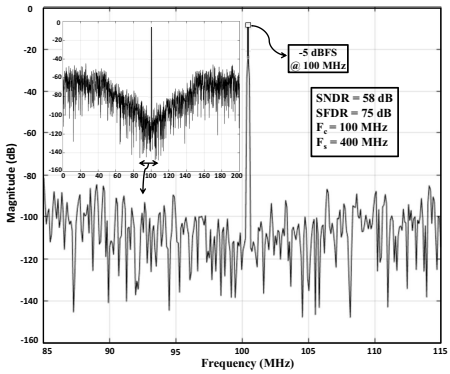

Fig. 9. Power spectral density for −5 dBFS input at 100 MHz.

B. Measurement Results

The measured output power spectrum density (PSD) for a −5 dBFS 100 MHz sinusoidal input is shown in Fig. 9 (top-left insert) from 0 to half of the sampling frequency. The main plot shows the in-band PSD over a 30 MHz bandwidth. From the plot, the spurious-free dynamic range (SFDR) is 75 dB. A two-tone test is performed with two sinusoids, 1 MHz apart, with amplitudes of −21 dBFS, as shown in Fig. 10. Fig. 11 shows the measured SNDR across the input signal amplitudes. The minimum detectable signal amplitude is −66 dBFS with a 100 MHz signal tone. Hence, a 61 dB dynamic range can be achieved, which is limited by the thermal noise from resonator and DAC. The total power consumption is 2.5 mW. The performance summary of the prototype ADC and comparison table to state-of-the-art in CT-BP-ΔΣM are provided in Table II. The measured Walden FoM is 38.6 fJ/conv.-step, which, to our knowledge, is the best among CT-BP-ΔΣM ADCs, specifically thanks to: 1) the single-stage pseudo-differential self-biased inverter instead of the conventional op-amp (or multiple amplifiers) in the loop-filter, 2) using positive feedback topology and merging with HPF, and 3) only one DAC per resonator.

The definition of Walden and Schreier figure-of-merits, $\mathrm{FoM_W}$ and $\mathrm{FoM_S}$, respectively, is as below.

$$\mathrm{FoM}_w = \frac{\mathrm{POWER}}{(2 \times \mathrm{BW} \times 2^{\frac{\mathrm{SNDR}-1.76}{6.02}})} \tag{4}$$

$$\mathrm{FoM}_s = \mathrm{DR} + 10\log_{10}\left(\frac{\mathrm{BW}}{\mathrm{POWER}}\right). \tag{5}$$

V. Conclusion

CMOS scaling has made the use of traditional op-amps increasingly difficult, especially in ADCs based on continuous-time (CT) bandpass (BP) delta-sigma modulators (ΔΣM). In

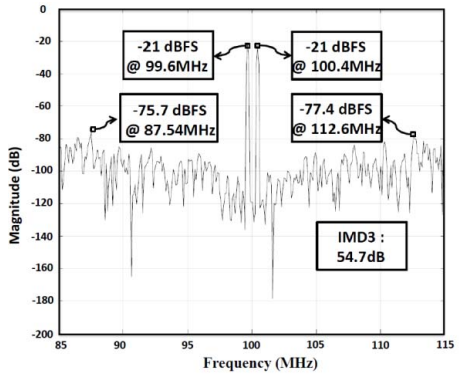

Fig. 10. Power spectral density for the two-tone test.

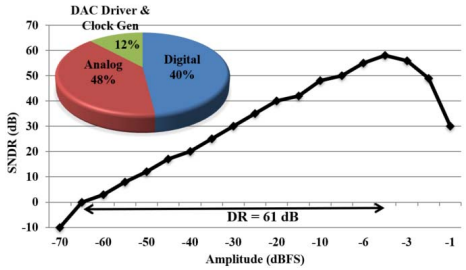

Fig. 11. Measured SNDR versus input amplitude, and power budget.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART IN CT-BP-ΔΣM

Ref.	[11]	[23]	[24]	[25]	**This work**
CMOS (nm)	65	250	180	65	**28**
F_s (MHz)	800	320	800	345	**400**
F_c (MHz)	200	10	200	2.4	**100**
BW (MHz)	24	20	10	10	**30**
DR (dB)	60	-	70	74.2	**61**
SNDR (dB)	58	53.5	68.4	64.1	**58**
Power (mW)	12	32	160	6.3	**2.5**
Area (mm^2)	0.2	1.3	2.5	0.385	**0.04**
FoM_w (fJ/Conv.)	380	2060	3720	240	**38.6**
FoM_s (dB)	153	-	147.96	166.2	**161.8**

this brief, we exploit self-biased pseudo-differential inverters as their replacements. The CT-BP-ΔΣM topology then gets re-architected such that the most critical block in the ADC, a resonator acting as a loop filter, can be of 2^{nd}-order and realized with the single pseudo-differential inverter which merges a positive feedback with high-pass filtering. This way, the count of passive components is minimized, thus leading to reduced power and area. The ΔΣM quantizer adopts a 5-bit asynchronous successive approximation register (ASAR) topology for high-speed operation.

The prototype modulator achieves a 61 dB dynamic range in a 30 MHz bandwidth by consuming only 2.5 mW at 1V supply. The resulting FoM of 38.6 fJ/conv.-step makes it the best among state-of-the-art designs.

REFERENCES

[1] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Dosho, and A. Matsuzawa, "A fifth-order continuous-time delta-sigma modulator with single-opamp resonator," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 697–706, Apr. 2010.

[2] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power optimized continuous-time ΔΣ ADC for audio applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 351–360, Feb. 2008.

[3] H.-C. Tsai, C.-L. Lo, C.-Y. Ho, and Y.-H. Lin, "A 64-fJ/Conv.-step continuous-time ΔΣ modulator in 40-nm CMOS using asynchronous SAR Quantizer and digital ΔΣ truncator," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2637–2648, Nov. 2013.

[4] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.

[5] P. L. Muntal and I. H. H. Jørgensen, "34.3 fJ/conv.-step 8-MHz bandwidth fourth-order pseudo-differential ring-amplifier-based continuous-time delta–Sigma ADC in 65 nm," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 10, pp. 198–201, Oct. 2018.

[6] E. Siragusa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.

[7] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658–2668, Dec. 2006.

[8] D. Vercaemer, J. Raman, and P. Rombouts, "Passive loop filter assistance for CTSDMs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 10, pp. 1157–1161, Oct. 2017.

[9] H. Mirzaie, H. Maghami, R. Zanbaghi, P. Payandehnia, K. Mayaram, and T. S. Fiez, "A 72.4-dB SNDR 92-dB SFDR blocker tolerant CT ΔΣ modulator with inherent DWA," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 3, pp. 347–351, Mar. 2019.

[10] H. Huang, S. Sarkar, B. Elies, and Y. Chiu, "28.4 a 12b 330MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving <1dB SNDR variation," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2017, pp. 472–473.

[11] H. Chae, J. Jeong, G. Manganaro, and M. P. Flynn, "A 12 mW low power continuous-time bandpass ΔΣ modulator with 58 dB SNDR and 24 MHz," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 405–415, Feb. 2014.

[12] S. Kim, C. Rhee, and S. Kim, "A wide dynamic range multi-mode bandpass continuous-time delta–sigma modulator employing single-opamp resonator with positive resistor-feedback," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 2, pp. 235–239, Feb. 2020.

[13] S. Zeller, C. Muenker, R. Weigel, and T. Ussmueller, "A 0.039mm^2 inverter-based 1.82mW 68.6dB-SNDR 10 MHz-BW CT- ΔΣ -ADC in 65 nm CMOS using power- and area-efficient design techniques," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1548–1560, Jul. 2014.

[14] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, Feb. 1992.

[15] M. Figueiredo, R. Santos-Tavares, E. Santin, J. Ferreira, G. Evans, and J. Goes, "A two-stage fully differential inverter-based self-biased CMOS amplifier with high efficiency," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 7, pp. 1591–1603, Jul. 2011.

[16] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE J. Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, Feb. 1991.

[17] J. R. Custodio, J. Goes, N. Paulino, J. P Oliveira, and E. Bruun, "A 1.2-V 165-μW 0.29-mm2 multibit sigma-delta ADC for hearing aids using nonlinear DACs and with over 91 dB dynamic-range," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 376–385, Jun. 2013.

[18] M. Ranjbar, A. Mehrabi, O. Oliaei, and F. Carrez, "A 3.1 mW continuous-time ΔΣ modulator with 5-bit successive approximation quantizer for WCDMA," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1479–1491, Aug. 2010.

[19] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[20] B. A. Chappell *et al.*, "Fast CMOS ECL receivers with 100-mV worst-case sensitivity," *IEEE J. Solid-State Circuits*, vol. 23, no. 1, pp. 59–67, Feb. 1988.

[21] H. J. Shin and D. A. Hodges, "A 250-Mbit/s CMOS crosspoint switch," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 478–486, Apr. 1989.

[22] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for medical implant devices," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.

[23] J. Arias *et al.*, "A 32-mW 320-MHz continuous-time complex delta-sigma ADC for multi-mode wireless-LAN receivers," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 339–351, Feb. 2006.

[24] C.-Y. Lu, J. F. Silva-Rivas, P. Kode, and J. Silva-Martinez, and S. Hoyos, "A sixth-order 200 MHz IF bandpass sigma-delta modulator with over 68 dB SNDR in 10 MHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1122–1136, Jun. 2010.

[25] Y. Xu, X. Zhang, Z. Wang, and B. Chi, "A flexible continuous-time ΔΣ ADC with programmable bandwidth supporting low-pass and complex bandpass architectures," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 3, pp. 872–880, Mar. 2017.