Oscillator Flicker Phase Noise: A Tutorial

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(Invited Paper)

***Abstract*—A deep understanding of how to reduce flicker phase noise (PN) in oscillators is critical in supporting ultra-low PN frequency generation for the advanced communications and other emerging high-speed applications. Unfortunately, the current literature is either full of conflicting theories and ambiguities or too complex in mathematics, hiding the physical insights. In this brief, we comprehensively review the evolution of flicker noise upconversion theories and clarify their controversial and confusing parts. Two classes of such upconversion mechanisms in voltage-biased *LC*-tank oscillators (nMOS-only and complementary) are specifically compared and numerically verified using a commercial simulation model of 28-nm CMOS. We identify that non-resistive terminations of both 2nd and 3rd harmonic currents contribute to oscillation waveform asymmetries that lead to the flicker noise upconversion. Further, we discuss three $1/f^3$ PN reduction mechanisms: waveform shaping, narrowing of conduction angle, and gate-drain phase shift.**

***Index Terms*—Flicker noise up-conversion, flicker phase noise reduction, impulse sensitivity function (ISF), cross-coupled oscillators, complementary oscillators, class-C, gate-drain phase shift.**

I. Introduction

As THE CMOS technology advances, the flicker ($1/f$) noise upconversion in oscillators has become a serious issue due to the increasingly worsening intrinsic $1/f$ noise in MOS transistors, especially in FinFETs [1] and FD-SOI [2]. At the same time, the emerging applications of 5G/6G wireless communications [3]–[13], high-speed wireline links [14], [15], and quantum computing [16]–[18] all rely on frequency sources of ultra-low phase noise (PN). Thus, a deep understanding of flicker noise upconversion and ensuing reduction mechanisms in oscillators is highly desired.

In contrast to thermal phase noise (PN), which has been well studied since 1966 [19]–[26], the flicker phase noise theory was not effectively developed [27] until the impulse sensitivity function (ISF) was introduced by Hajimiri and Lee in 1998 [28], [29]. The ISF theory suggests that a *symmetric* oscillating waveform would suppress any flicker noise from up-converting. As an example, by adding more delay stages to a ring oscillator, while maintaining its oscillating frequency, the intrinsic asymmetry in *RC*-induced rising and falling edges can be mitigated through sharpening of these edges, thus reducing the flicker, $1/f^3$, PN [30]–[32]. Nevertheless, the theory was silent on *how* to achieve that symmetric oscillation waveform in *LC*-tank oscillators. In a somewhat surprising twist, we demonstrate in this brief that the waveform symmetry is not the only way to suppress the flicker noise upconversion.

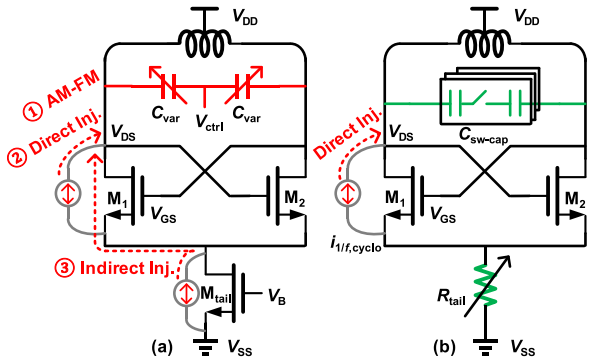

Fig. 1. Flicker noise upconversion mechanisms in (a) tail current-biased VCO and (b) voltage-biased DCO with digitally controlled tail-resistors.

The early study of $1/f$ noise upconversion in *LC*-tank oscillators was focused on current-biased VCOs [see Fig. 1(a)], in which the tail current source transistor, M_{tail}, is inserted to enhance the robustness against process, voltage and temperature (PVT) variations. Two types of $1/f^3$ PN mechanisms dominate: 1) frequency perturbation due to the large, thus sensitive, tuning-tank varators, C_{var}, and non-linear parasitic capacitance of connected devices (e.g., $M_{1/2}$); 2) instantaneous phase perturbation due to an injection of flicker current noise into the tank directly from the cross-coupled pair, $M_{1/2}$, or indirectly from the tail current source, M_{tail}, via $M_{1/2}$. The former mechanism of AM-FM by C_{var} was well explained in [33]–[35]: both differential-mode (DM) and common-mode (CM) oscillation waveform amplitudes depend on the tail-current and thus are slowly modulated by its $1/f$ current noise. As for the indirect injection of flicker noise from the tail current source, it was analyzed in [36], [37] by a theory based on "Groszkowski effect" [38] (different from the ISF theory). However, it fails to explain the $1/f$ noise upconversion from the cross-coupled pair, and thus may not contribute to a unified theory for all the flicker noise upconversion mechanisms in oscillators.

In recent years, it has become increasingly popular to replace the tail current source with digitally controlled tail-resistors [see Fig. 1(b)], thus removing the $1/f$ noise contribution by M_{tail} while ensuring the PVT robustness [39].

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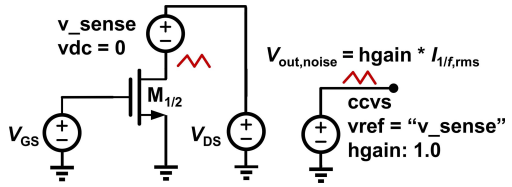

Fig. 2. Test-bench for $I_{1/f,\mathrm{rms}}(t)$ using dc/NOISE engines and a set of discrete waveform points of V_{GS} and V_{DS} within T_0 from PSS simulations.

This also enhances the I_{D}-vs.-V_{G} linearity of $\mathrm{M}_{1,2}$ [40], [41], resulting in lower unwanted harmonic currents (e.g., I_{H2}, I_{H3} may cause waveform asymmetries). This new class of voltage-biased oscillators can further promote a low-supply operation by removing the tail resistors [42]–[45]. Concurrently, the AM-FM mechanism has also been minimized with the scaling of CMOS technology and the introduction of switched-capacitors ($C_{\mathrm{sw\text{-}cap}}$) in both VCOs and digitally controlled oscillators (DCOs) [46], [47]. As a result, this leaves the cross-coupled pair as the only remaining source of the $1/f$ noise upconversion. In this brief, we discuss comprehensively the $1/f$ noise upconversion mechanisms from the cross-coupled pair as well as several $1/f^3$ PN reduction methods using a unified theory framework [47]–[51].

II. Flicker Noise Upconversion

A. Nature of Cyclostationary $1/f$ Current Noise

As discussed in [48], the flicker current noise $i_{1/f,\mathrm{cyclo}}(t)$ of a MOS transistor in a maintaining amplifier (e.g., cross-coupled pair $\mathrm{M}_{1/2}$ in Fig. 1(b)) is intrinsically at low frequencies $\Delta\omega$ (e.g., $2\pi\times 10\,\mathrm{kHz}$) but its amplitude is periodically changed (i.e., cyclostationary) within the oscillation waveforms of V_{GS} and V_{DS} with period of T_0 (i.e., $2\pi/\omega_0$, where ω_0 is the resonating frequency). Thus, for $\Delta\omega$,

$$i_{1/f,\mathrm{cyclo}}(t) = \sqrt{2} I_{1/f,\mathrm{rms}}(t)\cdot\cos(\Delta\omega t+\gamma) \tag{1}$$

where $I_{1/f,\mathrm{rms}}(t)$[1] is a periodically (T_0) modulated rms value of flicker current noise (unit: $\mathrm{A}/\sqrt{\mathrm{Hz}}$) and γ is an initial random phase. It is quite difficult to give an analytical expression of $I_{1/f,\mathrm{rms}}(t)$ in short-channel devices [1], [2], so it significantly limits quantitative analysis of flicker noise upconversion in advanced CMOS technology. As a remedy, we introduce a test-bench of $I_{1/f,\mathrm{rms}}(t)$ in Fig. 2 to capture its short-channel effects. The corresponding $I_{1/f,\mathrm{rms}}$ at $\Delta\omega$ (using dc/NOISE engines) for a set of waveform points of V_{GS} and V_{DS} within T_0 (from periodic steady-state (PSS) simulation) is sensed by a 0V dc voltage source (i.e., v_sense), transferred by a current-controlled voltage source (i.e., ccvs), and then "measured" through a voltage noise (i.e., $V_{\mathrm{out,noise}}$).

With the help of Fig. 3, let us now introduce a thought experiment on how $i_{1/f,\mathrm{cyclo}}(t)$ changes the phase of V_{DS} within T_0. We first decompose $i_{1/f,\mathrm{cyclo}}(t)$ into impulses as [52]

$$i_{1/f,\mathrm{cyclo}}(t) = \int_{-\infty}^{\infty} i_{1/f,\mathrm{cyclo}}(\tau)\cdot\delta(t-\tau)d\tau \tag{2}$$

where $\delta(t)$ is the Dirac delta function (i.e., unit impulse) and $i_{1/f,\mathrm{cyclo}}(\tau)$ represents the strength of the impulse, $i_{1/f,\mathrm{cyclo}}(\tau)\cdot\delta(t-\tau)$, at τ. Further, assume such an impulse at t_0 with a positive strength of $i_{1/f,\mathrm{cyclo}}(t_0)$ (i.e., $\sqrt{2}I_{1/f,\mathrm{rms}}(t_0)\cdot\cos(\Delta\omega t_0+\gamma)>0$) injecting into a falling slope of the oscillation waveform, see Fig. 3(a). It causes positive ΔV_{DS} due to the positive injected charge, and so the phase of V_{DS} is delayed (i.e., $\Delta\phi<0$). Since the phase of $i_{1/f,\mathrm{cyclo}}(\tau)$ (i.e., $\Delta\omega\tau+\gamma$) changes very slowly within T_0 (i.e., $\Delta\omega\cdot T_0\approx 0$), the polarity of the other following impulses within T_0 keeps positive. For example, the impulse at $t_0+T_0/2$ (i.e., $i_{1/f,\mathrm{cyclo}}(t_0+T_0/2)\cdot\delta(t-(t_0+T_0/2))$), still introduces positive ΔV_{DS} at the rising slope of V_{DS}, advancing its phase (i.e., $\Delta\phi>0$, see Fig. 3(c)). In addition, we observe no phase change for the impulse injection at the bottom (or peak) of V_{DS} (i.e., $\Delta\phi=0$), see Fig. 3(b). Obviously, the $1/f^3$ PN depends on the net phase change caused by $i_{1/f,\mathrm{cyclo}}(t)$ within the full T_0. Based on the above physical insights into flicker noise upconversion, the $1/f^3$ PN is derived as [28], [48]

$$\mathcal{L}_{1/f^3}(\Delta\omega) = \left(\frac{1}{2}\cdot\frac{\sqrt{2}}{\Delta\omega T_0}\int_0^{T_0} h_{\mathrm{DS}}(t)\cdot I_{1/f,\,\mathrm{rms}}(t)dt\right)^2 \tag{3}$$

where $h_{\mathrm{DS}}(t)$ is a non-normalized ISF[2] (unit: rad/C), describing the phase response of V_{DS} against current impulse perturbations. As per (36) in [28], $h_{\mathrm{DS}}(t)$ is approximately proportional to the derivative of V_{DS}, i.e., extreme during the mid-transitions of V_{DS} and null at its peak/bottom. Interestingly, it also suggests that "*waveforms with larger slope show a smaller peak in the ISF function*". In other words, sharper edges in V_{DS} are more robust to noise, while its less steep edges (also implying longer noise exposure time) are more vulnerable to noise. Thus, for asymmetric rising and falling edges of V_{DS}, $i_{1/f,\mathrm{cyclo}}(t)$ might cause smaller phase change during sharper transitions (i.e., net phase change $\neq 0$ in one period), leading to the flicker noise upconversion.

B. Origins of Waveform Asymmetries in Oscillators

Two pioneering but obviously conflicting theories about the $1/f$ noise upconversion in voltage-biased oscillators exist in literature. Bonfanti *et al.* [57] claimed that it is caused by a 3rd-harmonic current (i.e., I_{H3}) entering the capacitive path of the *LC*-tank. However, the effects of 2nd-harmonic current (i.e., I_{H2}) were neglected without further explanation. On the other hand, Shahmohammadi *et al.* [58] suggested the non-resistive terminations of I_{H2} cause waveform asymmetries, resulting in the $1/f$ noise upconversion, while the effects of I_{H3} should be regarded as benign (also claimed in [59]). In hindsight, the key difference appears that the former focused on complementary oscillators, while the latter on nMOS-only oscillators.

[1]This can be roughly modeled by periodically modulated transconductance G_{m} and drain current I_{D}; hence, it mainly depends on V_{GS} around the saturation region of MOS transistor [48].

[2]The positive sidebands of periodic transfer function (PXF) [53] provide a fast and accurate way to calculate $h_{\mathrm{DS}}(t)$ [49] (see also [54]–[56]).

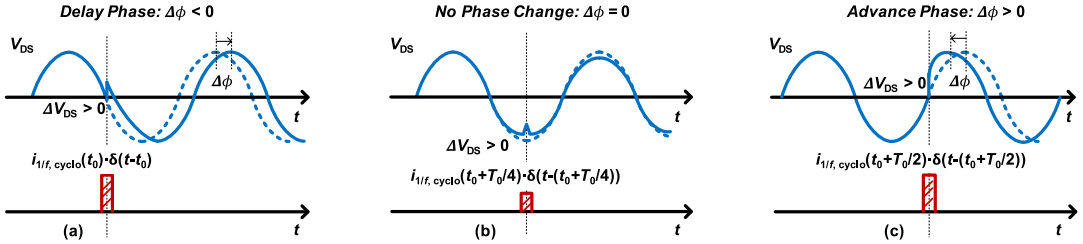

Fig. 3. Thought experiment: cyclostationary flicker current noise, $i_{1/f,\mathrm{cyclo}}(t)$, injecting into the tank at three representative instances: (a) falling slope, (b) bottom, and (c) rising slope of V_{DS}. Polarity of $i_{1/f,\mathrm{cyclo}}(t)$ stays positive but its magnitude is periodically modulated within T_0 (extreme at transition slopes).

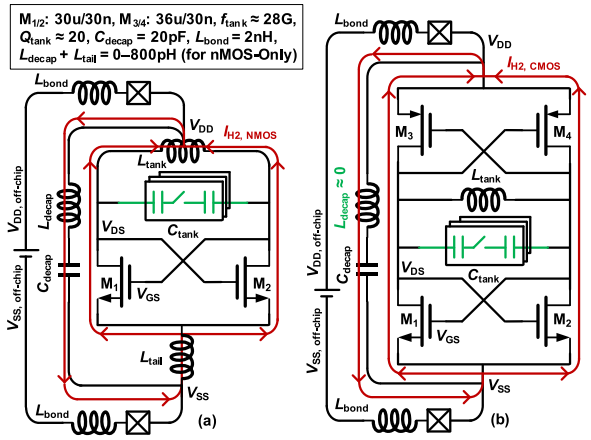

Fig. 4. CM return paths in (a) nMOS-only and (b) complementary oscillators.

TABLE I
SIMULATED AND CALCULATED PERFORMANCE OF VOLTAGE-BIASED OSCILLATORS IN NMOS-ONLY AND COMPLEMENTARY CONFIGURATIONS

	nMOS ($L_{\mathrm{decap}} = L_{\mathrm{tail}} = 0$)	Complementary
Technology	TSMC 28-nm LP CMOS	
Freq. (GHz)	28	
PN @10kHz (dBc/Hz) (Sim./Cal.)	-44.13/-44.3	-39.69/-40
PN @1MHz (dBc/Hz)	-102.3	-98.67
Power (mW)	5.27	
FoM @1MHz (dB)	-184.5	-180.5
$1/f^3$ PN Corner (kHz)	~3000	~3000
V_{DD} (V)	0.75	1.36
V_{H1} (mV)	792	736.1
$V_{\mathrm{H2}}/V_{\mathrm{H1}}$	8.11%	0.29%
$V_{\mathrm{H3}}/V_{\mathrm{H1}}$	1.30%	5.51%

To solve the conflicts and further gain comparative intuition, the nMOS-only and complementary oscillators are configured as in Fig. 4 with the same LC tank,[3] operating frequency, and power consumption. The local decoupling capacitor (modeled by C_{decap} and its parasitic inductance L_{decap}) provides a tight on-chip return path for the CM current (e.g., I_{H2}). As shown in Fig. 4(a) (assuming $L_{\mathrm{decap}} = L_{\mathrm{tail}} = 0$ for now), the CM current from $\mathrm{M}_{1/2}$ mainly enters the inductive path of the implicit CM inductance of L_{tank}. However, the CM return path in the complementary oscillator is entirely different. Firstly, there is no implicit CM inductance of L_{tank} in the CM return path. Besides, due to a short physical distance between the local V_{DD} and V_{SS}, the parasitic L_{decap} is nearly zero. By properly sizing the pMOS cross-coupled pair, the CM current generated by the nMOS cross-coupled pair is almost entirely absorbed by the pMOS pair, resulting in an ultra-low CM impedance and almost zero CM voltage.

Simulated performance of two unoptimized oscillators is summarized in Table I. Both suffer from severe $1/f$ noise upconversion ($1/f^3$ PN corner $>$ 3MHz). However, the 2nd-harmonic voltage (i.e., V_{H2}) in the complementary oscillator is an order-of-magnitude smaller than its 3rd harmonic voltage (i.e., V_{H3}), while V_{H2} in the nMOS-only oscillator dominates over V_{H3}. Hence, it is obvious that the harmonic compositions that degrade the waveform symmetry and $1/f^3$ PN differs.

[3]The center tap of L_{tank} in Fig. 4(b) is floating.

C. Harmonic Waveform Shaping Due to V_{H2} and V_{H3}

Waveform shaping of V_{DS} caused by I_{H2} (at $2\omega_0$) entering the inductive, resistive or capacitive nature of the CM tank (resonating at $\omega_{\mathrm{cm,tank}}$) is conceptually modeled by [50], [58]:

$$V_{\mathrm{DS}} \approx \begin{cases} |V_{\mathrm{H0}}| + |V_{\mathrm{H1}}|\cos\omega_0 t + |V_{\mathrm{H2}}|\cos(2\omega_0 t + \frac{\pi}{2}), & (L) \\ |V_{\mathrm{H0}}| + |V_{\mathrm{H1}}|\cos\omega_0 t + |V_{\mathrm{H2}}|\cos 2\omega_0 t, & (R) \\ |V_{\mathrm{H0}}| + |V_{\mathrm{H1}}|\cos\omega_0 t + |V_{\mathrm{H2}}|\cos(2\omega_0 t - \frac{\pi}{2}), & (C) \end{cases} \quad (4)$$

where $|V_{\mathrm{H0,1,2}}|$ are the magnitudes of dc, fundamental, and 2nd harmonic voltages, respectively. As shown in Fig. 5(a), the rising slope of V_{DS} (around $0.75T_0$) becomes steeper when I_{H2} sees an inductive nature of the CM tank (i.e., $\omega_{\mathrm{cm,tank}} \gg 2\omega_0$), while in Fig. 5(c) its falling slope (around $0.25T_0$) gets steeper when I_{H2} encounters a capacitive nature of the CM tank (i.e., $\omega_{\mathrm{cm,tank}} \ll 2\omega_0$). The V_{DS} becomes symmetric (with a flat bottom, see Fig. 5(b)[4]) when I_{H2} sees a resistive characteristic of the CM tank (i.e., $\omega_{\mathrm{cm,tank}} = 2\omega_0$). On the other hand, the V_{DS} waveform shaping introduced by I_{H3} entering the capacitive nature of the DM tank, or specifically, the resistive nature of the DM dual-tank (e.g., class-F oscillators [60]) is

$$V_{\mathrm{DS}} \approx \begin{cases} |V_{\mathrm{H0}}| + |V_{\mathrm{H1}}|\cos\omega_0 t + |V_{\mathrm{H3}}|\cos(3\omega_0 t + \pi), & (R) \\ |V_{\mathrm{H0}}| + |V_{\mathrm{H1}}|\cos\omega_0 t + |V_{\mathrm{H3}}|\cos(3\omega_0 t + \frac{\pi}{2}), & (C) \end{cases} \quad (5)$$

where $|V_{\mathrm{H3}}|$ is the magnitude of 3rd-harmonic voltage. As shown in Fig. 5(d), it is no longer straightforward to define the general level of steepness for the two transition slopes (i.e.,

[4]This is further supported by Fig. 9 in [65], where the voltage peaks at $\mathrm{M}_{1,2}$'s source node are aligned with zero-crossing points of their drain voltages (i.e., maximum CM current in zero-crossing points). This results in the bottom of DM drain voltage being aligned with the peak of CM voltage.

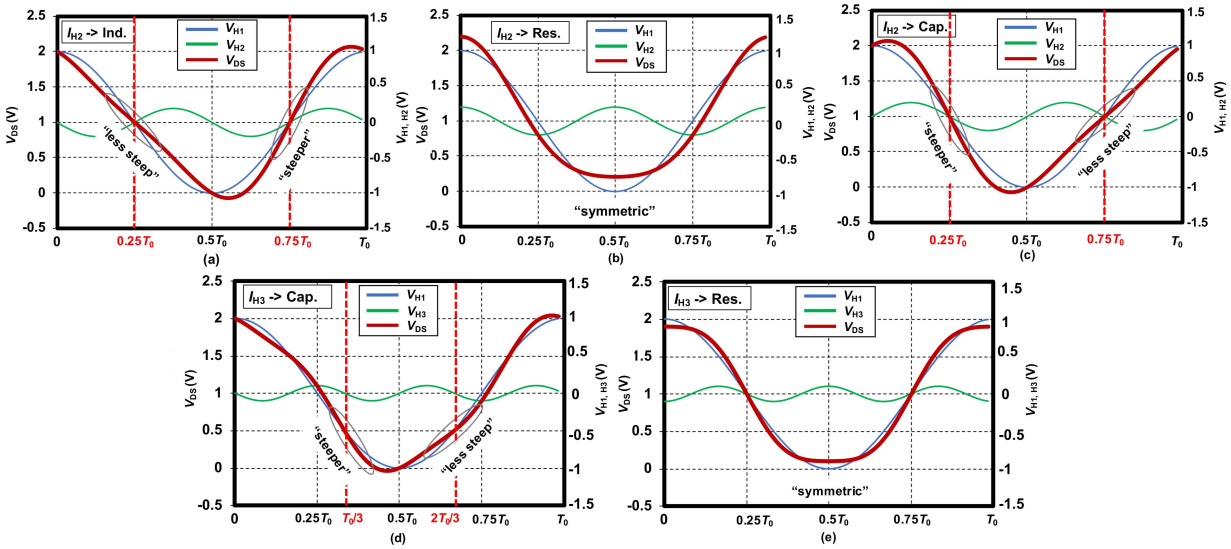

Fig. 5. Conceptual models of waveform-shaping of $V_{\rm DS}$ due to $I_{\rm H2}$ entering (a) inductive, (b) resistive, or (c) capacitive terminations at $2\omega_0$; and due to $I_{\rm H3}$ entering (d) capacitive or (e) resistive terminations at $3\omega_0$ (Conditions: $|V_{\rm H0}| = 1$ V, $|V_{\rm H1}| = 1$ V, $|V_{\rm H2}| = 0.2$ V, $|V_{\rm H3}| = 0.1$ V).

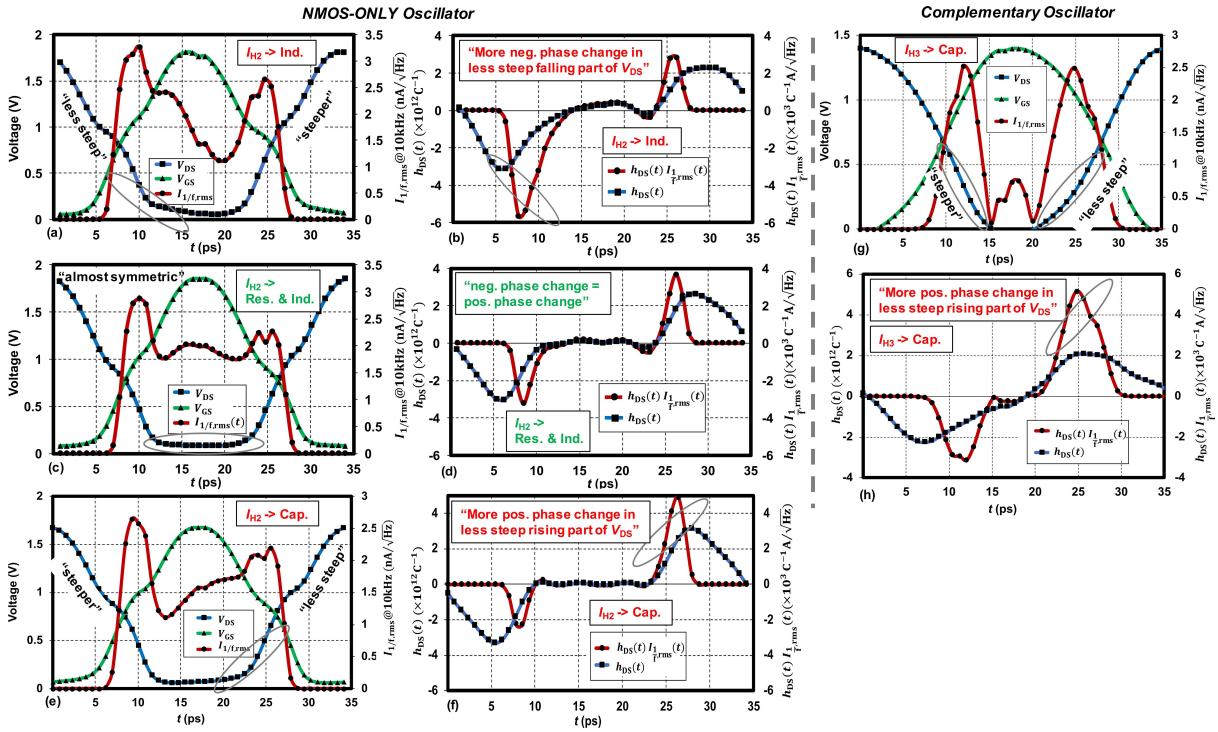

Fig. 6. Simulated waveform of $V_{\rm GS}$, $I_{1/f,\rm rms}$, $V_{\rm DS}$, $h_{\rm DS}$, and $h_{\rm DS} \cdot I_{1/f,\rm rms}$ when $I_{\rm H2}$ entering an inductive path (a), (b), resistive & inductive path (c), (d), and capacitive path (e), (f) in the nMOS-only oscillator, and when the $I_{\rm H3}$ entering a capacitive path (g), (h) in the complementary oscillator.

at around $0.25T_0$ and $0.75T_0$) due to the inflection caused by the peak/bottom of $V_{\rm H3}$ aligned with the falling/rising edges of $V_{\rm H1}$ [58]. However, the rising part of $V_{\rm DS}$ is still gentler around $2T_0/3$ as compared with the faster falling part around $T_0/3$, which was neglected in [58]. It becomes symmetric when $I_{\rm H3}$ entering a resistive path, see Fig. 5(e). We thus conclude that the capacitive terminations of $I_{\rm H2}$ and $I_{\rm H3}$ flatten the rising edges of $V_{\rm DS}$ while their inductive terminations flatten the falling edges in different time instances of $V_{\rm DS}$.

D. Numerical Verification

Fig. 6 shows the simulated plots of $V_{\rm GS}$, $I_{1/f,\rm rms}$ (obtained from Fig. 2), $V_{\rm DS}$, and $h_{\rm DS}$ (see [49]) of the nMOS-only [Fig. 4(a)] and complementary [Fig. 4(b)] oscillators under different terminations of harmonic currents. When $I_{\rm H2}$ enters the inductive path of the implicit CM inductance of $L_{\rm tank}$, it flattens the falling edge of $V_{\rm DS}$ (see Fig. 6(a) and compare it with the conceptual model in Fig. 5(a)), leading to a larger negative phase change (i.e., negative area of $h_{\rm DS} \cdot I_{1/f,\rm rms}$, shown in Fig. 6(b)) at the falling edge around $T_0/4$ (i.e., 8.75 ps). By

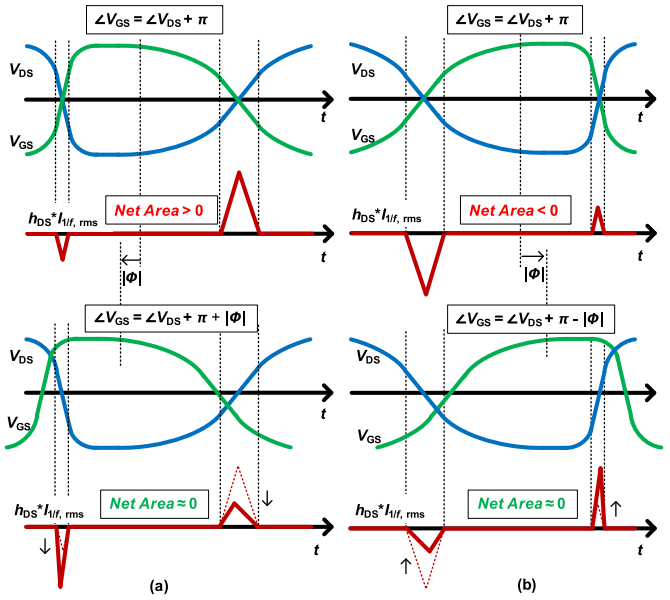

Fig. 7. Moving the peak of V_{GS} towards steeper edges of V_{DS} to suppress $1/f^3$ PN in an oscillator with steeper (a) falling or (b) rising edges of V_{DS}.

gradually increasing $L_{tail}+L_{decap}$, I_{H2} can see the resistive termination and then experience the capacitive termination due to the parasitic $C_{ds}+C_{gs}$ of nMOS pair [48], [50]. Figs. 6(e) and (f) show the more positive phase change caused by the $1/f$ noise in the flatter rising slopes of V_{DS} when I_{H2} enters the capacitive path. Interestingly, the weakest flicker noise upconversion does not happen when I_{H2} sees the purely resistive termination but rather at a partly inductive termination (e.g., $f_{cm,tank} = 59.64\ \text{GHz} > 2\times 28\ \text{GHz}$), as shown in Figs. 6(c) and (d). This is because in the nMOS-only oscillator, I_{H2} entering the slightly inductive termination will sharpen V_{DS}'s rising edges a little to compensate for the detrimental effects of the I_{H3} residue entering the capacitive termination. As for the complementary oscillator [see Figs. 6(g)-(h)], V_{H3} steepens the falling parts of V_{DS}, while flattening the rising parts, leading to a smaller negative area of $h_{DS}\cdot I_{1/f,rms}$ at around $T_0/3$ (i.e., 11.67 ps, see also Fig. 5(d)). Table I shows the tight agreement (<0.5 dB) between the theory and simulations of PN @10 kHz, thus demonstrating the effectiveness of the proposed numerical method.

III. Flicker Phase Noise Reduction Mechanisms

With the new understanding of waveform shaping caused by the two ill-behaved 2nd and 3rd harmonics, three $1/f^3$ PN reduction techniques can be analyzed.

A. Second Harmonic Resonance (or Not?)

An additional 2nd-harmonic resonance by means of a tail-tank was one of the earliest effective techniques to reduce both thermal PN and flicker PN in *LC* tank oscillators [61], [62]. The analysis in [63] demonstrated that the improvement in thermal PN relies only on high-impedance of the CM path to suppress the "loaded-*Q*" effects [64] (i.e., reducing $4kTg_{ds}$ noise). It can be also implemented by the high impedance of the inductive CM path, rather than only 2nd-harmonic resonance. Shahmohammadi *et al.* [58] pointed out the association of the 2nd harmonic resonance with the waveform slope symmetry to explain their $1/f^3$ PN reduction mechanism, and demonstrated its implementation by an implicit CM resonance (also see [65]). With a careful consideration of the CM return path [48], [66], this technique was first applied in a mm-wave class-F_{23} oscillator [8] featuring a record low $1/f^3$ PN corner of ~100 kHz (also see [67]–[70]).

A more general consideration should treat the termination of I_{H2} as a "knob" to tune the steepness of V_{DS}'s slopes. For example, in a complementary oscillator, I_{H3} might be entering the capacitive path of the DM tank and flattening the V_{DS}'s rising edges, causing the $1/f$ noise upconversion. However, adding a CM tank [65], [71] and forcing I_{H2} to enter high-impedance of the resistive/inductive CM path (also boosting V_{H2}) could sharpen these ill-behaved rising edges caused by V_{H3}, suppressing the $1/f^3$ PN.

B. Narrowing of Conduction Angle

Class-C oscillator was first introduced in [72] with a thorough analysis of its thermal PN mechanism. However, the theory explaining its excellent flicker PN (see [73]–[76] showing surprisingly good $1/f^3$ PN) was not revealed until [49]. In contrast to "symmetrising" the oscillating waveform by V_{H2} [48], narrowing of conduction angle could decrease the flicker current noise *exposure* to the asymmetric waveform caused by the 2nd (in nMOS-only class-C) or 3rd (in complementary class-C [77]) harmonic current entering the non-resistive terminations. In recent years, this technique attempted to add two "controlled switches" under the cross-coupled pair to decrease the conduction angle [78]–[80].

C. Phase Shift of V_{GS} Against V_{DS}

A positive phase shift of V_{GS} against V_{DS} (via an *RC* time-constant) was introduced [81], [82] in a complementary oscillator to reduce its $1/f^3$ PN. An intuitive understanding of this technique is portrayed in Fig. 7(a). As discussed in Section II, the 3rd-harmonic current entering the capacitive termination in a complementary oscillator, sharpens the falling edges of V_{DS} while leveling off its rising edges, thus leading to a smaller negative phase change caused by the $1/f$ noise at V_{DS}'s falling edges. However, if the peak of V_{GS} could move towards the steeper edge of V_{DS} (with shorter exposure time of $I_{1/f,rms}$) by some phase shift (i.e., $|\Phi|$), increasing the exposure magnitude of $I_{1/f,rms}$ for the limited exposure time, the net area of $h_{DS}\cdot I_{1/f,rms}$ in one period will be null, ultimately suppressing the $1/f^3$ PN. Recently, the gate-drain phase shift technique was implemented by a capacitance-ratio (better PVT robustness than with the absolute *RC* time-constant) in a transformer-based complementary oscillator, demonstrating low flicker PN with wide tuning range (39%) [51] (also see [83]–[85] for more details on phase shift in a transformer). Further, we could predict that a negative phase shift of V_{GS} against V_{DS} could suppress the $1/f^3$ PN in an oscillator with steeper rising edges of V_{DS} (e.g., I_{H2} entering the inductive termination), as shown in 7(b). We

believe the gate-drain phase shift could be another promising "knob" in other typologies of oscillators.

IV. Conclusion

In this brief, we survey the theoretical developments of the flicker noise upconversion and methods of mitigating it. To dispel some current misunderstandings, we clarify that it is *both* of the ill-behaved 2nd (dominating in nMOS-only oscillators) and 3rd (dominating in complementary oscillators) harmonics that cause asymmetries in the oscillating waveform, leading to the $1/f$ noise upconversion. An inductive termination of the 2nd or 3rd harmonic current could flatten the falling edges of $V_{\rm DS}$, while their capacitive path could flatten the rising edges. On the other hand, tuning the termination of the 2nd harmonic current, narrowing of conduction angle, and gate-drain phase shift are the three "knobs" to reduce the $1/f^3$ PN. The proposed simulation method of a periodically modulated rms value of flicker current noise (i.e., $I_{1/f,\rm rms}$) and non-normalized ISF (i.e., $h_{\rm DS}$) provide a powerful tool to study other low-flicker PN oscillator topologies in advanced CMOS.

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