A 0.2-V Three-Winding Transformer-Based DCO in 16-nm FinFET CMOS

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***Abstract*—In this brief, we introduce a 3.2–4 GHz three-winding transformer-based class-F digitally controlled oscillator (DCO) with a DC-DC booster for energy harvesting applications. A π-model is adopted for this multi-turn transformer to analyze its impedance transformation and overall loop gain. The trifilar coil generates large passive voltage loop gain, allowing the DCO supply voltage of 0.2 V to be even lower than the threshold voltage of transistors without any performance degradation. Due to the gate/drain isolation as well as smaller voltage-dependent capacitance in advanced FinFET technology, this brief achieves very low supply frequency pushing of 38 MHz/V. The switched capacitor placed at the tertiary winding can reach very fine resolution of 1.3 kHz due to the impedance transformations and source degeneration. The bias and control voltages of nearly zero power are generated with a switched-capacitor based DC-DC converter and a ring-based non-overlapped clock generator.**

***Index Terms*—Digitally controlled oscillator (DCO), energy harvesting, transformer, trifilar, FinFET, DC converter, voltage booster.**

I. Introduction

ENERGY harvesting (EH) is a topic of intensive research, promising battery-free operation of massive networks of wireless IoT devices [1]. To fulfill that goal, IC circuits featuring ultra-low power (ULP) consumption with ultra-low voltage (ULV) supply are desired. As an example, thermal electric, human vibration and photovoltaic EH, as shown in Fig. 1, produce ULV supplies (<0.3 V) that are well below the threshold voltage (V_{th}) of even the most recent FinFET CMOS transistors, thus making it extremely challenging for circuit designers. On the other hand, all-digital PLLs (ADPLL) are well known for their friendliness to low supply voltages and immunity from supply perturbations [2]. The major part of power consumption in the whole ADPLL lies in a digitally controlled oscillator (DCO) [2], [3]. Thus, new special circuit techniques are needed to make the IoT devices function properly with supplies below V_{th}.

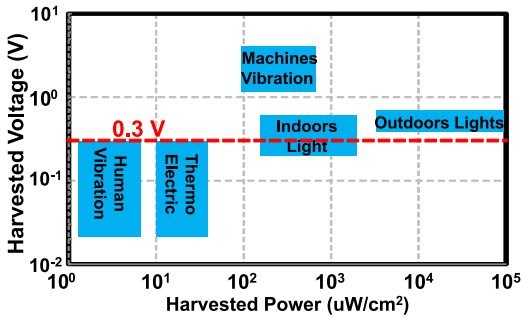

Fig. 1. Supply voltage from energy harvesters is typically low and highly dependent on the underlying energy activity.

A transformer feedback oscillator [4] is a promising topology for ULV operation due to its passive RF voltage gain. However, the gates and drains of the cross-coupled transistors there share the same dc voltage. This causes the resonating frequency, mainly due to its voltage-dependent gate capacitance C_g, to strongly track (i.e., be pushed by) the supply voltage, V_{DD}. For EH, the supply pushing must be very low due to the significant temporal variability of harvested voltage, as indicated in Fig. 1. The varying harvested voltage could be hundreds of mV, which is >10× larger than in conventional consumer IC designs.

A class-F oscillator [5] also provides a passive voltage gain, but the gates are electrically separated from the drains via the transformer, thus resulting in a low frequency pushing. However, its V_{DD} cannot readily go below V_{th} since the DCO tuning word voltage would not be able to reliably switch the capacitors at such low supply. In [6], a self voltage-boosting technique was proposed to provide a high-enough control voltage of VCO for the sufficient tuning range. A voltage booster using a GHz-level clock consumes excessive power and brings high frequency spurs, which must be then properly filtered.

This brief is an extension of our conference paper [7] in which a trifilar-coil oscillator topology providing large passive voltage gain was proposed to enable the sub-V_{th} operation. A π-model for a *three*-winding transformer is introduced to explain the resonant frequency and impedance transformation which helps to generate fine tune resolution. The source of the oscillator transistor is not tied to ground, hence the gate-source

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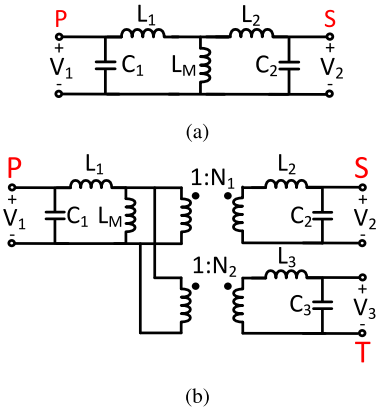

Fig. 2. (a) T-model for a 2-winding transformer-based resonator. (b) π-model for a 3-winding transformer-based resonator.

(V_{GS}) swing can be larger than in the conventional common-source cross-coupled pair topology. The 3rd-harmonic tone is coupled from the primary resonator to the source side, making a smaller effective ISF function. Due to the gate/drain isolation as well as smaller voltage dependent-capacitance in advanced FinFET technology, this brief achieves very low frequency pushing. To provide the bias and control voltages which are higher than V_{DD}, a switched-capacitor based DC-DC converter with a ring-based non-overlapped clock generator is proposed featuring a nearly zero power consumption.

II. Three-Winding Resonator Design

A conventional *two*-winding 1:2 transformer in a class-F oscillator can be thoroughly analyzed by a T-model of Fig. 2(a) [5]. However, if the number of windings is larger than 2, it is hard to adopt the T-model due to the duplicate mutual inductance effects. In [8], a π-model was adopted for a *multi*-winding transformer. In Fig. 2(b), V_1, V_2 and V_3 represent the primary, secondary and tertiary voltage sources. There are two ideal transformers in the middle with a perfect coupling coefficient $k = 1$. Capacitors C_1, C_2 and C_3 are digitally tunable to control the resonant characteristic of the network. The values of various inductances and turns ratios are captured in formulas (1)–(3) [8]:

$$N_1 = \frac{L_{M23}}{L_{M13}}, N_2 = \frac{L_{M23}}{L_{M12}} \tag{1}$$

$$L_M = \frac{L_{M12}L_{M13}}{L_{M23}}, L_1 = L_{11} - \frac{L_{M12}L_{M13}}{L_{M23}} \tag{2}$$

$$L_2 = L_{22} - \frac{L_{M12}L_{M23}}{L_{M13}}, L_3 = L_{33} - \frac{L_{M23}L_{M13}}{L_{M12}} \tag{3}$$

where L_{11}, L_{22} and L_{33} represent self-inductances of the primary, secondary and tertiary coils, respectively. Inductance L_1 equals L_{11} minus L_M, which is a mutual inductance part. Without the magnetic coupling, L_1 reduces to the self-inductance L_{11}. Terms L_{M12}, L_{M23} and L_{M13} represent mutual inductances between L_{11}, L_{22} and L_{33}, which could be obtained from electromagnetic (EM) simulations or measured with the other windings unloaded. From Fig. 2(b), the impedance transformation could be easily realized by the ideal transformers 1:N_1 and 1:N_2. To calculate the equivalent inductance (L_{eq}) seen from the primary coil, capacitors C_{1-3} are expediently removed. In this design, the secondary coil is connected to a high impedance (MOS gate), so the end-point of L_2 is considered open and its inductance could be ignored. Then, L_{eq} could be obtained as:

$$L_{eq} = \frac{N_2^2 L_1 L_M + L_1 L_3 + L_M L_3}{L_M N_2^2 + L_3} \tag{4}$$

The equivalent capacitance seen from the primary coil could be also derived from the impedance transformations:

$$C_{eq} = C_1 + N_1^2 C_2 + N_2^2 C_3 \tag{5}$$

In this design, N_1 and N_2 are equal to 1.87 and 0.37, respectively. Hence, N_2^2 is significantly smaller than 1 and so C_3 could be neglected in C_{eq}. Thus, the resonant frequency seen from the primary coil is derived as:

$$\omega_{osc} = \sqrt{\frac{1}{(C_1 + N_1^2 C_2)\frac{N_2^2 L_1 L_M + L_1 L_3 + L_M L_3}{L_M N_2^2 + L_3}}} \tag{6}$$

L_M, L_1, L_2 and L_3 are equal to 0.41, 0.15, 0.29 and 0.37 nH, respectively. C_1 and C_2 are set to 1 pF. The estimated resonant frequency is 3.34 GHz which is within a 3% error from EM simulations. Since the DCO requires a variable capacitance for frequency tuning, the DCO gain (K_{DCO}) could be derived as [2]:

$$K_{DCO}(f) = 2\pi^2 (L_{eq} \cdot \Delta C) f^3 \tag{7}$$

$K_{DCO}(f)$ is a frequency step in response to a small digitally induced ΔC step. If ΔC is placed at the tertiary coil, K_{DCO} could be re-written as:

$$K_{DCO,T}(f) = 2\pi^2 [L_{eq} \cdot \left(\frac{N_2^2}{1 + N_1^2 + N_2^2}\right) \cdot \Delta C_3] f^3 \tag{8}$$

$K_{DCO,T}$ represents the DCO gain contributed by the tertiary resonator. Eq. (8) shows that ΔC_3 will experience a 0.03× reduction. This helps with generating very fine tuning resolution (i.e., low K_{DCO}) by setting a small ratio of $N_2^2/(1 + N_1^2 + N_2^2)$. The very fine K_{DCO} helps with reducing the quantization noise of ADPLL in order to avoid a power hungry $\Sigma\Delta$ modulator [2], [9].

To leverage the advantage of class-F operation from a significant presence of the 3rd harmonic, the turns ratio of primary to secondary is set to 1:2 in this design. In Fig. 3, Z_{in} into the primary represents the input impedance seen from V_1 with a 3rd harmonic tone. By setting $C_1 = C_2 = C_3$, Z_{in} of the tertiary could also have a strong 3rd harmonic impedance peaking as shown by the blue curve. If the tertiary winding is adopted at the source side of MOS, V_{GS} could be reshaped to benefit from the lowered impulse sensitivity function (ISF).

III. Design of Trifilar DCO

The conventional class-F oscillator can provide a nearly 2× *passive* voltage gain due to the 1:2 turns-ratio transformer from the drain (D) to gate (G) of the MOS transistors. In the proposed trifilar oscillator, the passive voltage gain is *enhanced* by another winding located at the source (S) of the cross-coupled transistors, as shown in Fig. 4(a). The tertiary

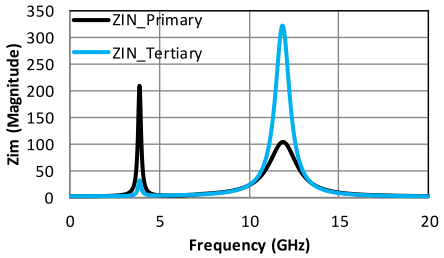

Fig. 3. Input impedances of three-winding transformer tank.

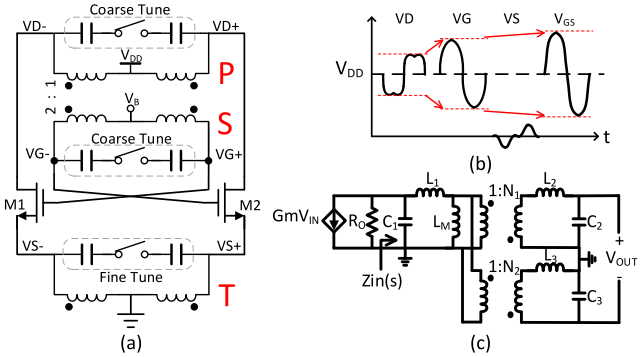

Fig. 4. Proposed trifilar oscillator: (a) schematic, (b) time-domain waveforms, (c) small signal π-model.

winding is coupled through a weak magnetic coupling 1:N_2 from the original primary winding. Consequently, the NMOS source signal (V_S) oscillates around the ground dc level and produces a voltage swing in the opposite direction to that of V_G, thus enhancing V_{GS}, as shown in Fig. 4(b). A higher effective V_{GS} is thus achieved.

Voltage V_B controls the gate bias of cross-coupled NMOS independently from $V_{\rm DD}$ due to the isolating effect of the transformer. The nonlinear capacitance C_G is typically 3× larger than C_D and so it would normally be the main contributor to the frequency pushing. Since V_B does not drain any current, it can undergo a heavy low-pass filtering to eliminate any of its transient effects on C_G.

The coarse bank with 23 MHz/bit is split between the transformer's primary and secondary windings to achieve the maximum Q enhancement [5]. The switched-capacitor at the source side can reach a very fine resolution of 1.3 kHz, as suggested by (8), which could help in eliminating the power-hungry $\Sigma\Delta$ modulator in an ADPLL.

The small-signal model of the trifilar oscillator is shown in Fig. 4(c). The primary side in Fig. 2(b) is equivalent to the drain side of cross-coupled MOS, and so on. The voltage loop gain could be derived by the formula for $V_{\rm out}/V_{\rm in}$:

$$\frac{V_{\rm out}}{V_{\rm in}} \simeq g_m(R_O||Z_{\rm in}(s))\frac{L_M}{L_{11}}(N_1+N_2) \tag{10}$$

$Z_{\rm in}(s)$ could be represented the long formula (9), as shown at the bottom of the page. From Eq. (10), the voltage loop gain

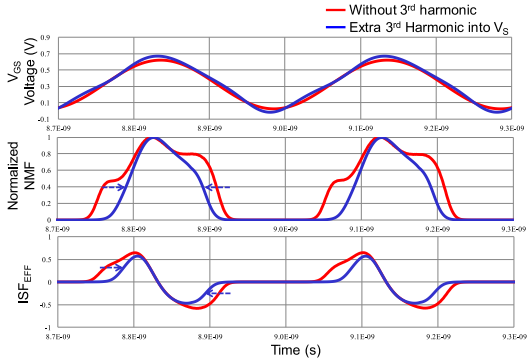

Fig. 5. ISF function benefiting from the 3rd harmonic injection.

could be enhanced by the term (N_1+N_2). For the same start-up condition, the device's required transconductance g_m could be reduced 55% at the sub-$V_{\rm th}$ bias while the passive voltage gain is already boosted up by 220% [2]. Thus, the supply voltage could be brought down to 0.2 V or lower, while still ensuring the reliable oscillation start-up. As shown in Eq. (10), higher N_1 and N_2 beneficially bring higher passive voltage gain. However, excessively large N_2 might bring strong source degeneration and degrade the MOS' g_m. In Fig. 4(c), $G_mV_{\rm in}$ and R_o bypass the tertiary winding for the sake of simplified derivation. The value of N_2 needs to be traded off between the active and passive voltage gains.

For the three-winding transformer, the effective quality factor could be calculated by $Q_{\rm tri} = \Im(Z_{\rm tot})/\Re(Z_{\rm tot})$. The total $Q_{\rm tri}$ will be a weighted combination of Q-factors of the three coils. Two thick metals and one ultra-thick metal are combined to achieve the lowest possible series resistance for the maximum Q-factor and minimum voltage drop in the supply path. $Q_{\rm tri}$ exceeds 11 within 3–4 GHz of the DCO tuning range (TR).

IV. Phase Noise (PN)

Figure 5 demonstrates the ISF function benefiting from the 3rd harmonic injection. At the top, the red curve is a waveform V_{GS} of the original class-F oscillator. The blue curves contain an additional 3rd harmonic injected into the source, thus achieving a higher amplitude by the tertiary feedback. At the zero-crossing points, the 3rd harmonic injection helps to narrow down the zero-crossing regions where the injected noise can severely degrade the phase noise. This effectively reduces the normalized noise modulating function (NMF) as indicated by the arrows at the middle of Fig. 5. Thus, a smaller effective ISF function and lower (∼2 dB) PN could be achieved.

V. DC-to-DC Converter

As mentioned above, if the available supply is below $V_{\rm th}$, then the sub-threshold control voltage of the switched-capacitor will lead to a very narrow tuning range. Furthermore, as this topology separates the drains and gates to enhance the overall g_m at low $V_{\rm DD}$, V_B bias higher than $V_{\rm DD}$ is needed

$$Z_{\rm in}(s) = \frac{s(N_2^2L_1L_M + L_1L_3 + L_ML_3)}{s^2(N_2^2L_1L_M + L_1L_3 + L_ML_3)(C_1 + N_1^2C_2) + L_MN_2^2 + L_3} \tag{9}$$

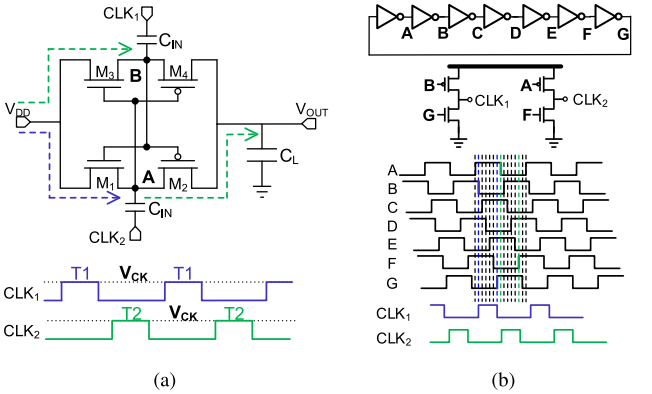

Fig. 6. (a) Voltage booster schematic. (b) Ring-based non-overlapped clock generator.

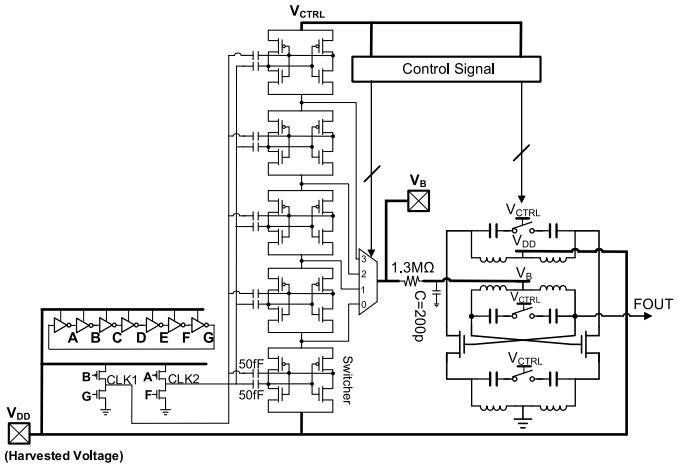

Fig. 7. Trifilar DCO with DC-DC converter.

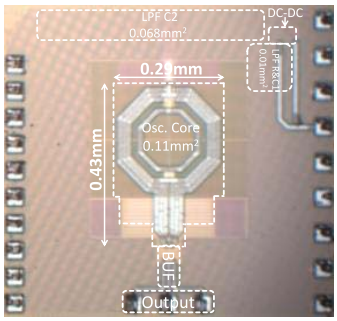

Fig. 8. Die micrograph.

in the sub-V_{th} operation. Consequently, a tiny DC-to-DC converter coupled to the harvested voltage is proposed to provide a nearly static control V_{ctrl} and bias V_B for the trifilar DCO. A cross-coupled voltage booster could help to generate V_{DD}+V_{CK} by the nonoverlapped clocks CLK_1 and CLK_2, as shown in Fig. 6(a). During T_1, point A is charged to near V_{DD}. In the next interval, T_2, CLK_2 changes from 0 V to V_{DD} and point B is charged to near V_{DD} and waiting for the next period for the boost-up. The important concern is for CLK_1 and CLK_2 to be non-overlapped; otherwise, M_1 and M_2 might be turned-on simultaneously and degrade the level of V_{OUT}. C_{IN} is designed to ensure the adequate current sinking from V_{OUT}. In this design, V_B drains no static current due to the gate load connection and static control. V_{ctrl} only consumes drain/source leakage of the buffer which drives the frequency tuning switched-capacitor. Thus, C_{IN} could be at the level of only tens of fF.

In conventional designs, a non-overlapped clock generator often comprises combinatorial logic to generate certain delays. A logic cell (e.g., NAND, NOR) usually requires at least three stacked MOS transistors, thus raising the minimum operational level of V_{DD}. Here, a non-overlapped clock generator is proposed using a simple ring oscillator (RO) with a clock gating technique, as shown in Fig. 6(b). A multi-phase single-ended 7-stage RO generates seven clock phases, from A to G. The switcher's inverters use a different gate control to generate the rising/falling edges of CLK_1 and CLK_2. Thus, the nonoverlapped period is defined as T_{RO}/N, where T_{RO} is the period of ring oscillator and $N = 7$ is the number of RO stages. The number of series-connected MOS in this circuit will not exceed two, which helps to operate at V_{DD} lower than 0.2 V. V_{in} provides the input to the voltage booster and directly controls the drain side of MOS. To save extra power from the RO, the oscillation frequency is set to tens of MHz by using small W/L-ratio inverters.

VI. Circuit Implementation

Figure 7 presents the overall view of this design. Five voltage booster stages driven by the non-overlapped clock generator provide a sufficiently high voltage to turn on the switched capacitors. This way, the full tuning range (i.e., <20%) can be recovered. A high-enough voltage for V_{ctrl} could also help to eliminate the frequency pushing effect from these switches. V_B uses a selected voltage booster output. Low-pass filter of 3 kHz corner is adopted to eliminate the ripple from voltage booster and to prevent the DCO PN degradation. Ripples of the lower frequency (i.e., <30 kHz) could be mitigated by the eventual ADPLL loop.

VII. Measurement

The proposed trifilar DCO is implemented in 16-nm FinFET CMOS, whose chip micrograph is shown in Fig. 8. Figure 9 shows on-wafer phase noise measurements. At the $V_{DD} = 0.4$ V setting, phase noise (PN) reaches −120 to −123 dBc/Hz and −143 to −145 dBc/Hz at 1 MHz and 10 MHz offsets, respectively. FOM is 188–191 dBc/Hz with a power consumption of 3.8 mW. In the $V_{DD} = 0.2$V mode, the PN worsens to −111∼ −113 dBc/Hz and −132 ∼ −135 dBc/Hz at 1 MHz and 10 MHz offsets, respectively, but the power consumption reduces to 0.6 mW, yielding FOM of 186–188 dB. The flicker PN corner is 40 kHz and 120 kHz at 0.2 V and 0.4 V, respectively. The frequency pushing in Fig. 10(a)(b) shows a small value of 3.627 MHz/V at 0.4 V and 12.6–38.2 MHz/V at 0.2 V. The coarse step size is 23 MHz/bit and the fine step is 1.3 kHz/bit. The DC-to-DC converter could operate at as low as 0.15 V, consuming only 0.2 uW at the 0.2 V input, as shown in Fig. 10(c). The proposed approach allows the DCO to ultimately operate at as low as 0.17 V of the harvested voltage.

To check for any spurs from the ring oscillator of non-overlapped clock generator, the measured phase noise with and without the DC-DC converter is shown in Fig. 10(d).

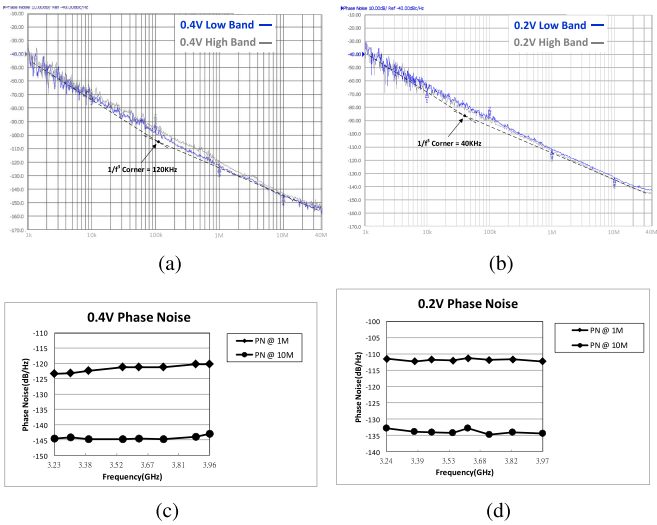

Fig. 9. Measured phase noise: (a) at 0.4 V; (b) at 0.2V; (c) at 0.4 V across tuning range; (d) at 0.2 V across tuning range.

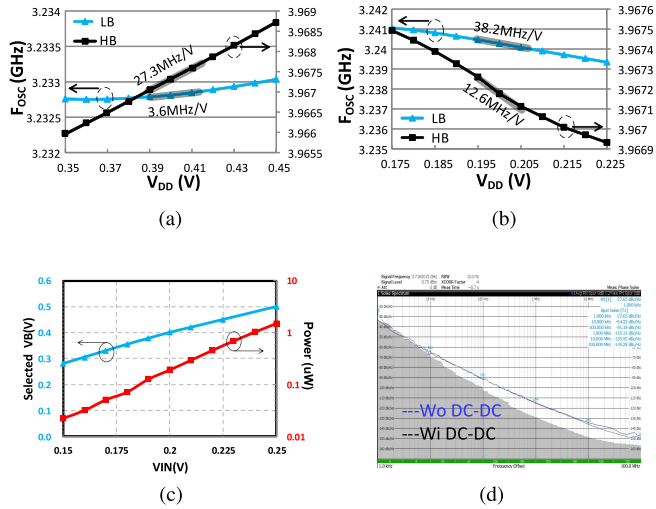

Fig. 10. Measurements of: (a) frequency pushing at 0.4 V; (b) frequency pushing at 0.2 V; (c) DC-DC converter; (d) phase noise spectrum wi/wo DC-DC converter.

TABLE I
COMPARISON WITH STATE-OF-THE-ART ULV OSCILLATORS

	This Work		[10]	[11]	[12]	[13]
Technology	16nm FinFET		65nm	40nm	28nm	28nm
VDD[V]	0.2	0.4	0.4	0.5	0.7	0.9
Tuning Range[GHz]	3.2-4.0 (22%)		2.5-3.3 (27%)	3.3-4.5 (31%)	4.7-5.4 (14%)	2.9-3.8 (27%)
Phase Noise [dBc/Hz] @ 10MHz	-134	-145	-147	-143	-138	-150
Power [mW]	0.6	3.8	6.8	4.1	0.5	6.8
FOM*	188	190	189	188	195	192
Frequency Pushing(MHz/V)	12.6-38.2	3.6-27.3	180*	46-60	NA	NA
1/f³ Corner(KHz)	40	120	2000	60	200	200
Core Area [mm²]	0.11		0.15	0.1	0.18	0.19

It exhibits no spurs, indicating the 3 kHz LPF is fulfilling its function. Table I shows comparison with state-of-the-art low-voltage LC-tank oscillators. Our V_{DD} is the lowest while delivering state-of-the-art performance. The area of 0.11 mm^2 is among the lowest. The frequency pushing and flicker noise corner frequency are both the lowest, mainly due to the trifilar topology and the use of FinFET devices.

VIII. CONCLUSION

This brief demonstrates a DCO for energy harvesting applications, which eliminates the intermediary power management system in conventional IoT solutions. By virtue of a trifilar-coil design, a passive voltage gain is boosted to overcome the start-up issues at a low supply voltage of 0.2 V. Separating the gate and drain voltages by the trifilar-coil transformer helps to bring the DCO supply below the threshold voltage. The variable capacitance from the gate side is separated from the main supply, thus eliminating the supply pushing effects by means of a low-pass filter. Fine tune resolution is achieved by means of impedance transformation from the tertiary coil. Class-F operation makes the waveform sharper for a better 1/f noise immunity and ISF. A tiny built-in DC-to-DC converter provides the gate biasing and control voltage for the switch capacitors with negligible power consumption. To operate at a low-supply voltage, a ring-based non-overlapped clock is generated by the gated inverters. Realized in TSMC 16-nm FinFET, it consumes sub-mW at 0.2 V, while achieving state-of-the-art performance. This brief shows a high potential for the solution of low-supply, low power consumption and low supply pushing in portable wireless applications.

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