A 33-GHz LNA for 5G Wireless Systems in 28-nm Bulk CMOS

Mahsa Keshavarz Hedayati, *Student Member, IEEE*, Abdolali Abdipour, *Senior Member, IEEE*, Reza Sarraf Shirazi, Cagri Cetintepe, *Member, IEEE*, and Robert Bogdan Staszewski, *Fellow, IEEE*

***Abstract*—This brief presents a design procedure of a compact 33-GHz low-noise amplifier (LNA) for fifth generation (5G) applications realized in 28-nm LP CMOS. Based on the unique set of challenges presented by advanced nanoscale CMOS, the emphasis is put here on the optimization of design and layout techniques for active and passive components in the presence of rigorous metal density rules and other back-end-of-the-line challenges. All passive components are designed and optimized with full-wave electromagnetic simulations for a high quality factor. In addition, layout techniques help to miniaturize the total area as the suggested 5G frequency band of 33 GHz is not high enough to provide a sufficiently compact chip size. The resulting increase in the concentration of required metal fills furthermore makes this optimization more challenging. The fabricated LNA consists of two cascode stages with a total core area of 0.68×0.34 mm^2. It exhibits 4.9-dB noise figure and 18.6-dB gain at 33 GHz while consuming only 9.7 mW from a 1.2-V power supply.**

***Index Terms*—Low-noise amplifier (LNA), 28-nm CMOS, millimeter-wave (mm-wave), metal density rules, electromagnetic (EM) modeling, 5G cellular, system-on-chip (SoC).**

I. Introduction

THE FIFTH Generation (5G) of mobile communications is shaping out as a flexible infrastructure capable of handling the ever-increasing demand for mobile data. While the 5G standard is yet to be finalized, mm-wave frequency bands appear as best candidates to satisfy the insatiable demand for bandwidth. Based on the recommended frequency spectra for 5G at mm-wave, the 33 GHz band is selected in this brief due to its minimum atmospheric absorption. While necessarily addressing the tough 5G performance requirements, the upcoming transceivers must simultaneously focus on low cost, low footprint and low power consumption [1]. A fully integrated SoC solution addresses these challenges through tight monolithic integration of RF, analog and digital circuitry. This drives the implementation towards the ever more advanced CMOS technology nodes in order to benefit from the Moore's law of scaling of area, power consumption and speed of digital logic. Recognizing these trends, this brief adopts an advanced 28-nm bulk CMOS technology in a quest to enable fully integrated mm-wave 5G SoC transceivers. In this brief, we take on (arguably) the most challenging building block, i.e., an LNA, and simultaneously focus on high-performance, low-area and low-power aspects, thus maximizing the relevant figure-of-merit (FoM), while solving numerous problems associated with this new technology adoption.

While certainly a boon for digital circuits, the 28 nm CMOS faces some new critical challenges in RF circuit design. Lower intrinsic gain of transistors translates into lower available LNA gain, although their gain efficiency g_m/I typically remains higher. Furthermore, closer proximity of the back end-of-line (BEOL) stack to the lossy substrate and lower overall metal stack thickness in comparison with the dedicated RF-CMOS technologies add more parasitic losses, which manifest in lower quality (Q)-factors for inductors and transmission lines [2]. The latter necessitates precise modeling of passive components in addition to the active ones, and renders EM full-wave simulations an integral part of the circuit design.

In addition, as pointed out in [3], complicated design rules, especially tough metal density rules, which are much stricter than previously, cause considerable degradation of passive components. In order to satisfy the required minimum metal density, one needs to populate all passive structures, such as inductors and transmission lines, with dummy metal fills on all metal layers. The effects of these dummy fills on Q-factor as well as self-resonance frequency (SRF) of passive devices are investigated in this brief. It has to be strongly pointed out that the 33 GHz band of 5G is not yet high enough to enjoy benefits of small enough passive devices of >60GHz designs that can be largely free of the dummy metal fills. The feature size of surrounding areas of 33 GHz inductors and transformers is still relatively large compared to the maximum metal-free area allowed by the technology. Consequently, the relatively higher concentration of metal-filled regions aggravates design of high-quality passive components. Model inaccuracies in mm-wave and wider process variations are further challenges.

The advanced CMOS technology, however, can inherently benefit some aspects of RF designs. Noise contribution of transistors decreases as CMOS scales. This trend helps with the reduction of noise figure (NF) and overall design of LNAs. Specifically, lower device parasitics and corresponding high f_t and f_{max} (410/230 GHz for core transistors) enable high-speed/frequency operation and extend it up to mm-wave [2], [4]. Associated reductions in power consumption and area result in denser, lower-cost and power-efficient circuits.

Manuscript received June 27, 2018; revised July 7, 2018; accepted July 9, 2018. Date of publication July 24, 2018; date of current version September 27, 2018. This work was supported by Science Foundation Ireland under Grant 14/RP/I2921. This brief was recommended by Associate Editor J. M. de la Rosa. *(Corresponding author: Abdolali Abdipour.)*

M. Keshavarz Hedayati is with the Department of Electrical Engineering, Amirkabir University of Technology, Tehran 159163-4311, Iran. During this work, she was with School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, D04 Ireland (e-mail: mahsa.hedayati@ucd.ie).

A. Abdipour and R. S. Shirazi are with the Department of Electrical Engineering, Amirkabir University of Technology, Tehran 159163-4311, Iran (e-mail: abdipour@aut.ac.ir).

C. Cetintepe and R. B. Staszewski are with the School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, D04 Ireland (e-mail: robert.staszewski@ucd.ie).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2018.2859187

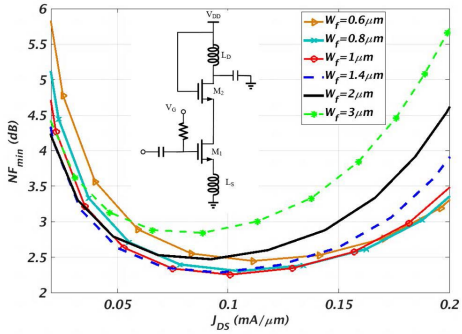


Fig. 1. Simulated NF_{min} as a function of drain current density for 28 nm cascode transistors with drain and source PDK inductors at 33 GHz ($N_f = 30$).

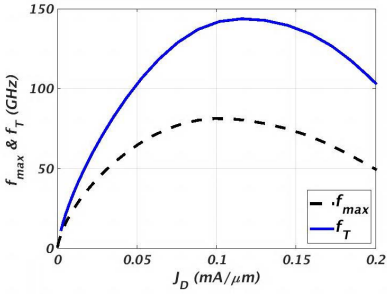


Fig. 2. Simulated f_{max} and f_T of 28 nm cascode transistors as a function of $J_D = I_D/W$ ($V_{DS} = 1.05$ V, $N_f = 30$, $W_f = 1$ μm).

This brief introduces a compact 33-GHz LNA with 18.6 dB gain and 4.9 dB NF implemented in TSMC 1P9M 28-nm LP bulk CMOS technology. Section II discusses the circuit design and highlights active and passive component design and optimization. Section III reports the simulation and measurement results.

II. MM-Wave LNA Design in 28-nm CMOS

A. Millimeter-Wave Transistor Design

In order to accurately design mm-wave circuits for high-performance in 28 nm CMOS, the transistor layout has to be carefully implemented for reduced interconnect parasitics and optimum device sizes. Toward the former goal, the transistors use a double-sided gate contact to minimize gate resistance,which otherwise might impact noise and gain performance of the LNA. In addition, wide and short interconnects contact the drain and source regions, which immediately connect to the ultra-thick M9 layer.

Proper selection of finger width and drain current density can maximize the mm-wave transistor performance. In particular, this brief optimizes the transistor size/bias combinations by taking into account the cascode nature of LNA stages. Common-source (CS) and common-gate (CG) transistors feature the same size for subsequent analyses, as their non-unity ratio was noted to yield only marginal performance changes. As Fig. 1 demonstrates, a current density of $J_D = I_D/W = 0.1\ mA/\mu m$ and finger width of $W_f = 1$ μm minimize NF_{min} of the cascode topology and hence its actual noise figure. Fig. 2 plots f_{max} and f_T as a function of current density and shows that $J_D \approx 0.1\ mA/\mu m$ maximizes these quantities, leading to a better mm-wave performance. Moreover, Fig. 3 presents f_{max} for different finger width (W_f) and finger number (N_f) combinations, and shows that ~1-μm-wide fingers help keep f_{max} sufficiently high for the considered transistor width range.

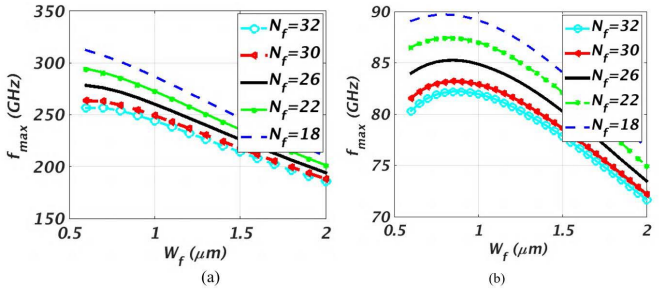


Fig. 3. Simulated f_{max} as a function of W_f in 28-nm: (a) Single transistor, (b) cascode structure.

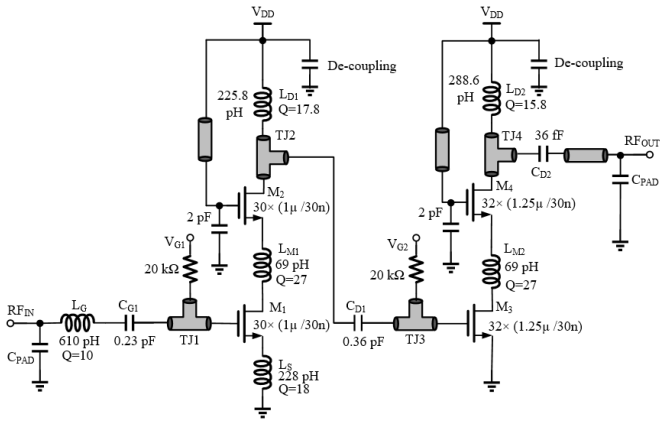
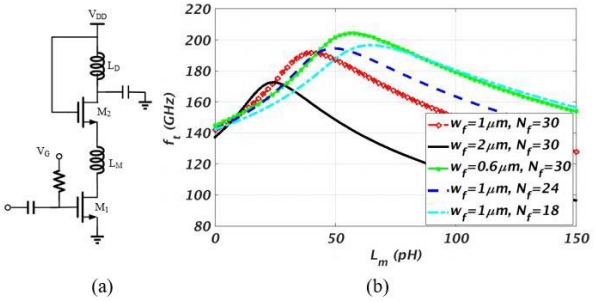


Fig. 4. Schematic of the 33-GHz LNA.

B. Circuit Design

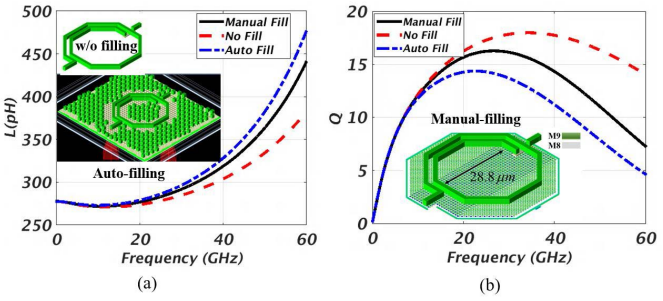
The presented LNA comprises two stages, as shown in Fig. 4. Each stage employs a cascode topology owing to its better reverse isolation, higher gain and improved stability at mm- wave frequencies [5]. The drain-source interconnection of CS and CG transistors feature a series 69 pH inductor (L_{m1}, L_{m2}) to tune out the parasitic capacitances at these nodes, and to boost the gain [5], [6]. In particular, Fig. 5 demonstrates a 21% improvement in f_T with the optimized L_m. The transistor bias sets the optimum NF_{min} current density of 0.1 $mA/\mu m$. Selected finger widths and number of fingers (1/1.25 μm, 30/32) minimize NF_{min}, maximize f_{max}, and set the trade-off between maximum available gain, minimum NF and power consumption of each stage, as Fig. 3 supports. The second stage is designed without source degeneration and slightly bigger than the first one for higher gain (by 2.9 dB + 1.1 dB) and slightly lower NF (by 0.1 dB). The intrastage inductors (L_{m1}, L_{m2}) and transistor sizes are adjusted to help transform the source impedance to the optimum noise impedance [5].

The input impedance Z_{in} matching employs inductive degeneration of the first CS stage: The 0.23 nH L_S degenerates the source of M_1 and sets the real part of Z_{in} to 50 Ω, while the 0.61 nH L_G, in series with the gate, approximately tunes out the imaginary part. Load inductors and MOM capacitors are optimized for interstage and output conjugate matching. The matching networks incorporate the effect of RF pads, which have reduced pad dimensions (55x55 μm^2) and employ $M9{+}AP$ layers to minimize their capacitance to the substrate ($C_{PAD} = 35\ fF$ according to full-wave simulations). A dense



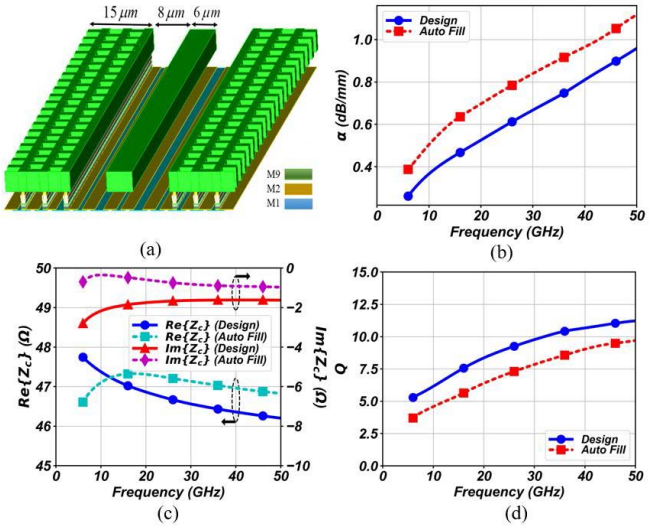
(a) (b)

Fig. 5. Simulated f_T of the cascode structure as a function of L_M: (a) Simulated schematic, (b) simulation results.



(a) (b)

Fig. 7. Full-wave simulated characteristics of L_{D2}: (a) Inductance, (b) Q.



(a) (b) (c) (d)

Fig. 6. Designed GCPW transmission line: (a) Line geometry, (b) simulated attenuation constant, (c) characteristic impedance, (d) quality factor.

grid of connected metal fills on M1 to M8 forms the strong chip ground plane and minimizes the parasitic impedances in the return path.

C. Design of Passive Components

Decreased BEOL thickness, closer proximity to the lossy Si substrate and highly restricted metal density rules of 28 nm CMOS make it all difficult to realize high-quality on-chip passive components, thus calling for their accurate design and optimization. Moreover, unsupported frequency range of PDK passive component models (qualified up to 20 GHz) and customized passive layouts make EM simulations an inherent part of the design.

The interconnects between the active and lumped passive components of the LNA employ a grounded coplanar waveguide (GCPW) topology, as illustrated in Fig. 6(a). These GCPW transmission lines use M9 for the signal trace and side ground planes. At the substrate interface, partially overlapping M1 and M2 strips act as a shield to avoid leakage of the EM fields into the lossy silicon substrate, thereby improving the Q-factor [7]. The side ground planes connect to the lowest metal layer through stacked vias from M1 to M9. M1 and M2 strips underneath the signal trace are left floating to prevent these highly resistive traces from acting as a current return path. Hence, the return current flows through the thick metal stack and cause negligible loss. The foundry rules necessitate a few modifications to the traditional GCPW structure: (i) side ground planes exhibit a slotted pattern, and (ii) connected fills from M1 to M8 increase the metal density while maximizing their distance to the signal trace as much as possible [7].

Passive components need to be modeled accurately at mm-wave to properly evaluate their parasitics and loss contributions, both of which have a pronounced impact on the circuit performance. In line with this goal, GCPW transmission lines, T-junctions, inductors and MOM capacitors are characterized with full-wave EM simulations, and are then optimized for maximum Q. Figs. 6(b)-(d) show simulated characteristics of the GCPW transmission line adopted in our design: The transmission line has a Q factor of 10.1, with an associated 0.74 dB/mm loss at 33 GHz. The same figure also compares these values to that of a traditional CPW: The lack of a shield and a metal stack arrangement, and random placement of automatically generated metal fills yield a worse Q of 8.2 at the same frequency, an observation justifying our modifications.

Accurate design of T-junctions is essential for low-loss connection of transmission line segments. Therefore, an optimized unit GCPW T-junction layout was designed to minimize the insertion and return losses. GCPW T-junctions TJ_2 and TJ_4 at the drain connections of M_2 and M_4 have considerable effect on the overall gain. The optimized T_{J2} and T_{J4} junctions present insertion losses of 0.3 dB and 0.2 dB, respectively, compared to ideal wire connections. It should be noted that TJ_2 and TJ_4 also contribute to the drain inductance of M_2 and M_4, and these contributions are accounted for during the design of L_{D1} and L_{D2}.

Since this technology PDK does not have any high-Q Metal-Insulator-Metal (MIM) capacitors, MOM capacitors which are optimized for maximum Q are employed instead. A large number of parallel short fingers as well as parallel metal layers maximize the capacitance density and help reduce the parasitic series resistance. Q factor of C_{D1} is 12.2 at 33 GHz.

Fig. 7 shows the geometry and simulated characteristics of a typical inductor (L_{D2}) employed in the LNA design for different fill scenarios. As the inset of Fig. 7(b) illustrates, the manually filled inductor employs the ultra-thick M9 layer for the coil and a guard ring on M1 similar to the PDK-supplied one. It features a dense arrangement of manually generated metal fills (over M1 to M7 inside the coil, and M1 to M9 outside) to avoid DRC errors. Fig. 7(a) depicts the same inductor without any filling (w/o fill) and with automatically generated top-level filling (auto-fill). Full-wave simulations show a Q of 18.0 at 33 GHz for the coil itself without any fills. Manual metal fills decrease Q to 15.8, whereas automatically generated dummy fills reduce this further down to 13.0 at 33 GHz. EM-aware placement of manual fills helps to mitigate Q factor degradation compared to the quasi-random placement of auto-fill generator which furthermore aims a more aggressive metal density in general. The remaining inductors of the LNA are

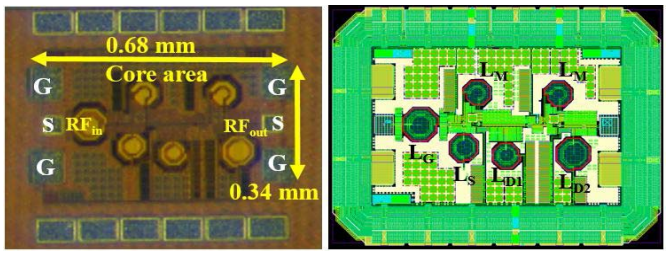


Fig. 8. Chip micrograph and layout of the fabricated LNA.

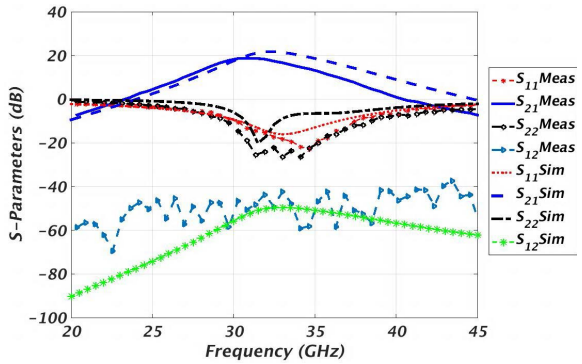
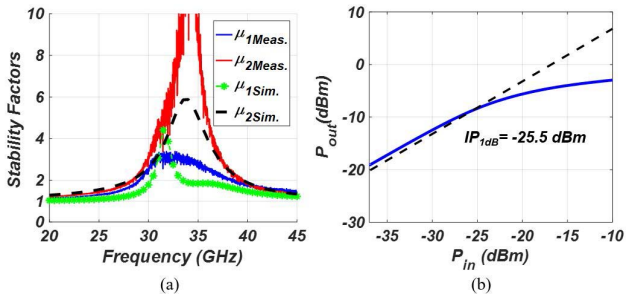
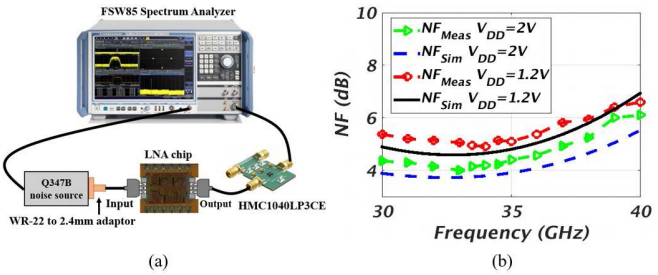


Fig. 9. Measured vs. simulated S-parameters of the 33-GHz LNA.



(a) (b)

Fig. 10. Measured LNA stability and linearity: (a) Stability factors, (b) compression characteristics at 33 GHz.



(a) (b)

Fig. 11. (a) NF measurement setup, (b) simulated and measured NF.

similarly optimized with EM simulations, and their quality factors are reported in Fig. 4. The spacing between inductors and proximity to nearby devices are also investigated to allow for a compact and DRC-compliant layout with negligible mutual coupling effects.

In order to suppress the parasitic inductance and resistance of the interconnects leading to V_{DD} I/O pads of both LNA stages, a proper combination of de-coupling capacitors is employed. Since SRF of MOM capacitors decreases for high capacitance values, a parallel combination of low-capacitance MOM capacitor units is used instead for a de-coupling capacitance of 10-20 pF with a high SRF to mitigate wirebond parasitics of dc I/O pads.

III. LNA Simulation and Measurement Results

The LNA circuit design is finalized following the integration of full-wave characterized passives and subsequent tuning. Simulated S-parameters of the complete LNA are shown in Fig. 9. The gain plot reveals a peak of 21.1 dB at 33 GHz, and a 3-dB bandwidth of 4.4 GHz. Return losses are better than 10 dB in the same band. Figs. 10(a) and 11 plot the simulated μ stability factors and NF. The LNA is stable up to 45 GHz, and simulated NF is 4.58 dB at 33 GHz. This simulated NF is higher than NF_{min} ~2.4 dB reported in Fig. 1, due to addition of bias resistances (contributing 0.2 dB), GCPW transmission lines (0.4 dB), post-layout parasitics of PDK transistors and inductors (0.2 dB), the matching inductor L_G (0.6 dB) and the second LNA stage (0.7 dB). L_G dominates this NF increase next to the second stage because of its high inductance and associated relatively poor Q, the latter of which trades-off with area through coil width (0.35 dB improvement leads to 40% area increase). Linearity simulations show an IP_{1dB} of −25 dBm at 33 GHz.

The LNA is fabricated in TSMC 1P9M 28 nm LP bulk CMOS. Fig. 8 shows a micrograph of the assembled chip, which occupies a core area of $0.68\times0.34\text{mm}^2$. The dc and ground pads are connected to the PCB with wirebonds to enable transistor biasing, whereas the mm-wave input and output pads are probed. S-parameters of the LNA chip are measured with Picoprobe 67A-GSG-100 CPW probes interfaced with Agilent E8361A PNA. Prior to the measurements, reference planes are set at probe tips through an off-chip SOLT calibration. RF pad capacitances are not de-embedded from the measurement results, as these were absorbed into the matching network. Fig. 9 presents the measured S-parameters of the LNA: $|S_{21}|$ shows a peak of 18.6 dB at 33 GHz, and the 3-dB bandwidth reads 4.7 GHz (14%). $|S_{11}|$ and $|S_{22}|$ are below −10 dB over 30-37 GHz and 29.0-38.5 GHz, respectively, amounting to a matching bandwidth of 21.2%. Reverse isolation of the LNA is better than 45 dB. The LNA remains stable as evidenced by the stability factors μ_1 and μ_2 in Fig. 10(a). During these measurements, first and second cascode stages draw 3.5 mA and 4.6 mA, respectively, from a 1.2 V supply.

Linearity measurements are conducted with the power sweep function of E8361A PNA. Fig. 10(b) reproduces compression measurements at 33 GHz, and demonstrates that measured IP_{1dB} of −25.5 dBm is in agreement with simulations.

The noise figure is measured with the Y-factor method using R&S FSW85 spectrum analyzer and Keysight Q347B noise source in a Faraday cage. An external LNA (HMC1040LP3CE) is used as a pre-amplifier right before FSW85 to reduce measurement uncertainty. The NF measurement setup is illustrated in Fig. 11(a). Measured noise figure is 4.90±0.22 dB at 34 GHz as plotted in Fig. 11(b).

Table I summarizes the performance of the implemented LNA, and compares it with state-of-the-art mm-wave CMOS designs. We use the following FOM expressions to weigh different aspects of these designs:

$$FOM_1(conv.) = \frac{Gain[abs]\times 1000}{(F-1)[abs]\times P_{DC}[mW]}((Watt)^{-1}) \quad (1)$$

$$FOM_2 = \frac{FOM(conv.)\times(BW/f_0)}{(CoreArea[mm^2]\times f_{\max}[GHz])}\left(\left(Watt\times mm^2\times GHz\right)^{-1}\right) \quad (2)$$

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

Ref.	Tech.	Freq. (GHz)	Max Gain (dB)	NF(dB)	P_{DC} (mW)	Area* (mm^2)	Topology	FOM_1 $(W)^{-1}$	FOM_2 $(W\times mm^2 \times GHz)^{-1}$	FOM_3 $(W\times mm^2 \times GHz)^{-1}$
[8]	0.18 μm	14.3-29.3	9.9	4.3-5.8	13.9	0.54	CG-2CS	133	5.8	8.4
[9]	65 nm	7.6-29.0	10.7	4.5-5.6	12.1	0.23	Cascaded CG & CS	157	27	23
[10]	65 nm	15.8-30.3	10.2	3.3-5.7	12.4	0.18	Cascode	242	28	44
[13]	65 nm	35-43	14.3	3.8	28.8	0.252	1 triple-cascode	129	2	11.9
[11]	65 nm	54.4-90.0	17.7	5.4-7.4	19.0	0.28	4 stage CS	164	3.2	6.5
[6]	28 nm	91.0	32.0	5.3	36.0	0.21	6 Cascode stages	462	2.7	24
[12]	28 nm	68.1-96.4	29.6	6.4-8.2	31.3	0.25	4 CS stages	271	3.8	11
This work**	28 nm LP	33	18.6 | 24.5	4.9 | 4.0	9.7 | 27.6	0.23	2 Cascode stages	433|414	8.1 | 7.8	57 | 54

*Core area includes RF GSG pad area but without the DC pads. ** Reported values are for 1.2 V and 2.0 V supply voltage, respectively.

$$FOM_3 = \frac{FOM(conv.)}{(CoreArea[mm^2] \times f_{\max}[GHz])}\left(\left(Watt \times mm^2 \times GHz\right)^{-1}\right) \quad (3)$$

where $F = 10^{NF/10}$ represents the noise factor. FOM_1 stands for the conventional FOM definition, while FOM_2 and FOM_3 extend the former with normalized silicon area to better reflect the occupied area, and thus cost, for fully integrated 5G systems. As we are not aware of similar designs for the targeted carrier frequency and similar technology node, we compare the performance of our LNA with state-of-the-art reported for different mm-wave bands and/or at other CMOS nodes. When compared to the other 28-nm solutions but at the higher frequency band, this 5G band starts disadvantaged due to a relatively larger area footprint for the passive components and faces the adverse effects of relatively higher concentration of metal fills. Moreover, Q-factor of GCPW interconnects stays relatively low compared to those works, as the latter scales roughly with the square root of carrier frequency, as shown in Fig. 6(d). However, even though the reported LNAs for older technology nodes feature better gain and NF, this brief ends up in a compact design with less power consumption and competitive mm-wave performance thanks to the optimized layout practices. Consequently, FOM_1 is one of the highest, falling slightly short of [6]. The reached FOM_2 is the best, except for [9] and [10], which target ultra-wideband applications hence their excessive (as for our 5G applications) bandwidth disproportionately contributes to FOM_2. As the proposed 5G systems are typically narrowband with their fractional bandwidth not exceeding 5-10%, FOM_3 removes the emphasis on bandwidth in an effort to obtain a more accurate metric for 5G applications. An inspection of Table I reveals that this brief presents the highest FOM_3 and satisfies the stated goals for the targeted application, making it a good candidate for a 5G SoC implementation.

IV. CONCLUSION

This brief is the first report of a 33-GHz LNA fabricated in the advanced but challenging 28-nm CMOS. All passive components of transmission lines, inductors and pads are designed and optimized with full wave simulations to cope with the strict metal density rules and other mentioned BEOL challenges of the technology for a satisfactory mm-wave performance. The fabricated LNA demonstrates high FOM while consuming less power and area compared to state-of-the-art, which makes it more applicable for 5G communications.

ACKNOWLEDGMENT

The authors thank Iran National Science Foundation (INSF) for scholarship, MCCI and Analog Devices for indirect support, EMX for software license, TSMC for University Shuttle chip fabrication, and Hsieh-Hung Hsieh for discussions.

REFERENCES

[1] S. Onoe, "Evolution of 5G mobile technology toward 2020 and beyond," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2016, pp. 23–28.

[2] E. Adabi, B. Heydari, M. Bohsali, and A. M. Niknejad, "30 GHz CMOS low noise amplifier," in *Proc. Symp. IEEE Radio Freq. Integr. Circuits (RFIC)*, Honolulu, HI, USA, 2007, pp. 625–628.

[3] F.-W. Kuo *et al.*, "A 12mW all-digital PLL based on class-F DCO for 4G phones in 28nm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, USA, 2014, pp. 1–2.

[4] M. A. T. Sanduleanu, G. Zhang, and J. R. Long, "31–34GHz low noise amplifier with on-chip microstrip lines and inter-stage matching in 90-nm baseline CMOS," in *Proc. Symp. IEEE Radio Freq. Integr. Circuits (RFIC)*, San Francisco, CA, USA, 2006, p. 4.

[5] T. Yao *et al.*, "Algorithmic design of CMOS LNAs and PAs for 60-GHz radio," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1044–1057, May 2007.

[6] D. Pepe and D. Zito, "32 dB gain 28 nm bulk CMOS W-band LNA," *IEEE Microw. Compon. Lett.*, vol. 25, no. 1, pp. 55–57, Jan. 2015.

[7] F. Vecchi, M. Repossi, W. Eyssa, P. Arcioni, and F. Svelto, "Design of low-loss transmission lines in scaled CMOS by accurate electromagnetic simulations," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2605–2615, Sep. 2009.

[8] Y.-T. Lo and J.-F. Kiang, "Design of wideband LNAs using parallel-to-series resonant matching network between common-gate and common-source stages," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 9, pp. 2285–2294, Sep. 2011.

[9] P. Qin and Q. Xue, "Design of wideband LNA employing cascaded complimentary common gate and common source stages," *IEEE Microw. Compon. Lett.*, vol. 27, no. 6, pp. 587–589, Jun. 2017.

[10] P. Qin and Q. Xue, "Compact wideband LNA with gain and input matching bandwidth extensions by transformer," *IEEE Microw. Compon. Lett.*, vol. 27, no. 7, pp. 657–659, Jul. 2017.

[11] Y. Yu, H. Liu, Y. Wu, and K. Kang, "A 54.4–90 GHz low-noise amplifier in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2892–2904, Nov. 2017.

[12] M. Vigilante and P. Reynaert, "A 68.1-to-96.4GHz variable-gain low-noise amplifier in 28nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2016, pp. 360–362.

[13] B.-J. Huang, K.-Y. Lin, and H. Wang, "Millimeter-wave low power and miniature CMOS multicascode low-noise amplifiers with noise reduction topology," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 12, pp. 3049–3059, Dec. 2009.