A Low-Power Continuous-Time Delta–Sigma Modulator Using a Resonant Single Op-Amp Third-Order Loop Filter

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***Abstract*—A third-order loop filter (LF) using a single op-amp resonator is presented for continuous-time delta–sigma modulators. The proposed technique improves both the power and area efficiencies by reducing the number of active components and simplifying the modulator topology. It also enhances the controllability of the transfer function and resonating condition of the single op-amp LF by using positive feedback. A more power-efficient implementation is obtained with an autonomous common-mode dynamic comparator. Fabricated in a 180-nm CMOS technology, the modulator occupies an active area of 0.14 mm^2 and consumes 37.4-μW power from a 1.8-V supply. It achieves a dynamic range of 72.5 dB and a peak signal-to-noise and distortion ratio of 67.3 dB in a 150-kHz signal bandwidth when clocked at 12 MHz. The Walden figure-of-merit of the modulator is 65.9 fJ/conv.-step.**

***Index Terms*—Continuous-time, delta–sigma modulator, third-order, single op-amp resonator, loop filter, dynamic comparator.**

I. Introduction

DELTA–SIGMA modulators (DSMs) with continuous-time (CT) loop filters (LFs) have gained popularity in battery powered applications due to their potential for low power consumption and low-voltage operation [1]. CT modulators provide an inherent anti-aliasing function and have a relaxed speed requirement on the active elements compared to their discrete-time counterpart. In particular, CT DSM architectures are good choices for applications with high resolutions and low bandwidths [2]–[4].

Recently, low power design has become an more important area of research. To achieve low-power dissipation, op-amp reduction techniques that merge multiple active-RC integrators into a single op-amp while still providing the same dynamic characteristics as conventional architectures have been proposed [5]–[10]. It is possible to diminish the power consumption by using a number of op-amps lower than the order of the modulator, because the quality of the notch can be maintained by an RC network with a single op-amp LF [11].

Second-order DSMs are presented in [5]–[7] based on a single op-amp LF in which resonance is realized by positive feedback. The positive feedback constitutes a notch filter and preserves the desired resonant behavior, resulting in reduced area and power consumption. References [9] and [10] describe a third-order DSM realized in a single op-amp. Although the resulting circuits achieve state-of-the-art performances, third-order single op-amp LFs have drawbacks that must be addressed. The non-resonant LF in [9] is unable to optimize the noise transfer function (NTF) zeros for the maximum signal-to-noise ratio (SNR). Meanwhile, the resonant LF in [10] has difficulty controlling both the transfer function (TF) and resonating condition because of its complex RC network. In addition, the resonance in [10] is generated by feedback cancellation. Therefore, a sufficient loop gain is required at the resonance frequency. Furthermore, these third-order LFs not only degrade the loop stability, but they are more difficult to implement than second-order LFs.

In this brief, a resonant single op-amp third-order LF is presented for continuous-time DSMs. An RC network proposed for the LF improves power and area efficiency and enhances the controllability as well. The modulator employs an autonomous common-mode dynamic comparator, which helps save power. The remainder of this brief is organized as follows. Section II introduces the proposed DSM architecture, Section III describes the circuit implementation, Section IV presents the measurement results, and Section V provides conclusions.

II. Proposed DSM Architecture

Fig. 1 depicts a block diagram for third-order DSMs. In general, the number of op-amps in active-RC-based DSMs is equal to the LF order [1], [12]. The conventional third-order LF (Fig. 1(a)) has three active integrators (i.e., three op-amps), two feedforward branches (c_1, c_2), and one feedback branch (d). Unlike the conventional LF, the proposed third-order structure uses a single op-amp resonator (SOR) to improve power and area efficiency, as shown in Fig. 1(b). This is achieved by an appropriate RC network design that needs to be consistent with the third-order TF of H(s). An explanation of the

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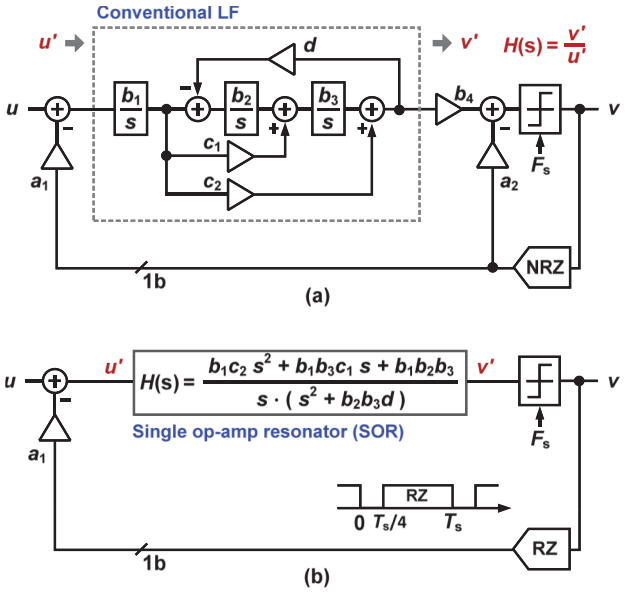

Fig. 1. Block diagram of third-order DSMs. (a) Conventional DSM. (b) Proposed DSM.

TABLE I
COEFFICIENTS OF THE THIRD-ORDER SINGLE OP-AMP RESONATOR

a_1	b_1	b_2	b_3	c_1	c_2	d
2	0.0234	0.4396	1	2.5	7.2735	0.0084

proposed approach is provided, along with a detailed circuit diagram, in Section III. Table I shows all of the LF coefficients of the modulator proposed for optimum gain scaling. A single-bit quantizer is realized using an autonomous common-mode dynamic comparator to have a more power-efficient implementation and reduce the quantization error. A return-to-zero digital-to-analog converter (DAC) using a switched resistor scheme with a 75% duty cycle is chosen for removing the components related to excess-loop delay [6]. The simplicity of the proposed structure—specifically, the active components consisting of just one third-order SOR, one comparator, and one DAC—is apparent.

III. CIRCUIT IMPLEMENTATIONS

A. Third-Order Single Op-Amp Resonator

The proposed SOR is shown in Fig. 2. The third-order TF is realized using a single op-amp with an input resistor (R_1), three series-connected capacitors (C_1, C_2, C_3), and two twin-T resistors placed at nodes V_X and V_Y. The input signal and the output signal are applied to R_6 and R_5, respectively, through the inverting op-amp with a DC gain of –1. The inverting op-amp is easily implemented using the cross-coupled connection of the differential signal. The TF of this LF is given by:

$$\mathrm{TF} = \frac{v'}{u'}. \tag{1}$$

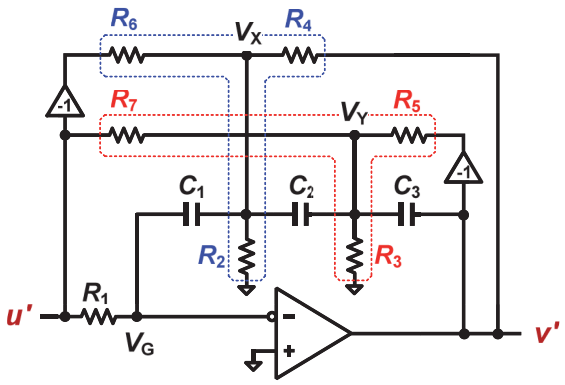

Fig. 2. Proposed third-order single op-amp resonator.

Then, the numerator (v') and denominator (u') are calculated through:

$$v' = \mathrm{s}^2 \cdot \frac{1}{C}\left(\frac{4}{R_1} + \frac{1}{R_7} - \frac{3}{R_6}\right) + \mathrm{s} \cdot \frac{1}{C^2}\left[\frac{3}{R_1}\left(\frac{1}{R_X} + \frac{1}{R_Y}\right) - \frac{2}{R_6 R_Y}\right] + \frac{2}{C^3 R_1}\left(\frac{1}{R_X} \cdot \frac{1}{R_Y}\right). \tag{2}$$

$$u' = \mathrm{s} \cdot \left[\mathrm{s}^2 + \frac{2}{3C^2 R_5 R_Y}\right] \tag{3}$$

where $R_X = R_2 \| R_4 \| R_6$ and $R_Y = R_3 \| R_5 \| R_7$ denote the equivalent resistances of the parallel-connected resistors at nodes V_X and V_Y, respectively, and $C = C_1 = 2 \cdot C_2 = C_3$ is the typical capacitance of the series-connected capacitors. The TF is expressed in the same form as $H(\mathrm{s})$ in Fig. 1 and does not include a second-order Laplace term in its denominator. The positive feedback path produced by R_5 eliminates this second-order term when:

$$R_4 = 3 \cdot R_5. \tag{4}$$

Thus, the proposed RC network has a resonating TF, which is used to implement a zero-optimized NTF. The resonance in (4), which is realized by positive feedback, relies on matching the resistors ratio rather than the absolute values, thereby improving immunity to process and temperature variations. The proposed resonator is implemented with a similar number of passive components, but it has two fewer amplifiers than conventional active-RC resonators [1], [12].

Moreover, it is possible to simplify the circuit, thereby reducing the power consumed, because the resonance is achieved by positive feedback. Because the resonances in [8] and [10] are determined by feedback cancellation, a sufficient loop gain is needed at the resonance frequency to maintain the notch quality. However, since the resonance of the proposed SOR is generated by positive feedback, the desired resonant behavior is preserved even when the loop gain degrades. This is because positive feedback enhances the quality factor of the notch [11]. Therefore, although the unity-gain bandwidth (UGBW) of the op-amp is reduced, the signal-to-noise and distortion ratio (SNDR) of the modulator does not deteriorate significantly. The simulated SNDR distribution versus the

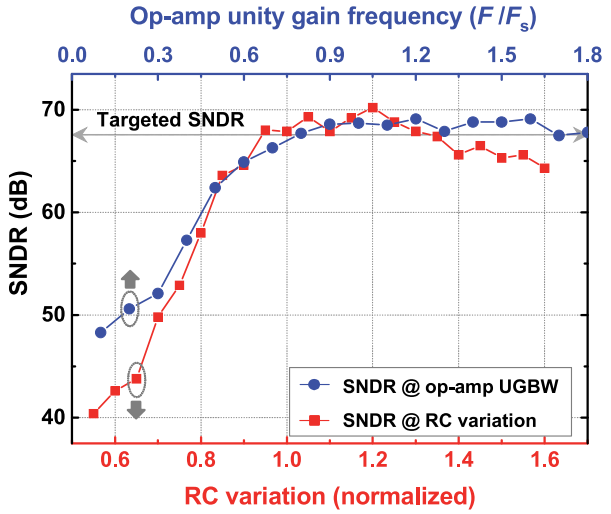

Fig. 3. SNDR versus op-amp unity-gain frequency and normalized RC product.

finite unity-gain frequency is shown in Fig. 3. The proposed modulator retains the targeted SNDR, even with a low UGBW of $0.8{\cdot}F_s$. The measurements reveal that the amplifier requires a UGBW of $1.15{\cdot}F_s$ to tackle the linearity issue. To satisfy the gain-bandwidth requirement, the op-amp employs a two-stage topology with feedforward compensation [6].

Fig. 3 also shows the SNDR versus the normalized RC product. An RC time-constant variation moves the notch position and changes the NTF shape slightly, causing SNDR deterioration. The modulator can achieve the targeted SNDR for time constants in the range of 0.95–1.35. Although the third-order LF is implemented with SOR, the modulator tolerates large time constant variations and thus providing highly sustainable loop stability. To extend the tolerable RC time-constant variation, the capacitors comprise a 3-bit binary-weighted tunable capacitor bank.

In addition to the advantage mentioned above, the proposed structure provides independent control of both poles and zeros, which enhances TF controllability. The input resistor (R_1) is chosen to be 500 kΩ to comply with the thermal noise requirement. The capacitance of the corresponding nominal integration capacitor (C) is then 4 pF. The numerator coefficients (zeros) are controlled independently by different resistors. Resistors R_7 and R_6 adjust the numerator's second-order term. The first-order term is modified by both R_X and R_6, and the zeroth-order term is controlled by R_X and R_Y. Because the equivalent resistance is less than the smallest resistance in the parallel network, R_X and R_Y are dominantly affected by R_2 and R_7, respectively, in this design. Thus, resistor pairs R_7 and R_6, R_6 and R_2, and R_2 and R_7 can adjust the respective second-, first-, and zeroth-order terms of the numerator. Resistor R_5 determines the denominator coefficients (poles) of the resonating TF. Consequently, it is easy to calibrate the TF of the proposed third-order LF.

B. Autonomous Common-Mode Dynamic Comparator

The quantizer is constructed based on a dynamic comparator using a sample-and-hold scheme to avoid slew-dependent

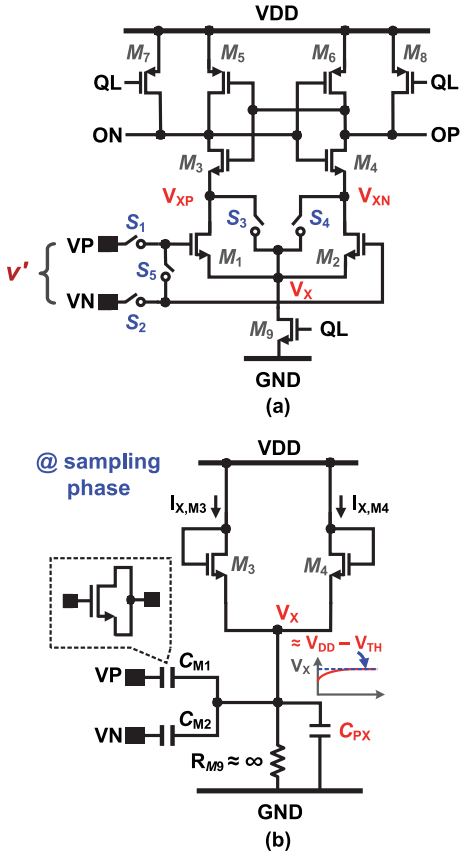

Fig. 4. Autonomous common-mode dynamic comparator based on sample-and-hold scheme. (a) Schematic diagram of proposed comparator. (b) Operation at sampling phase.

errors. As shown in Fig. 4(a), the proposed comparator eliminates both sampling capacitors and common-mode voltage from the conventional comparator [6], reducing the active area and power consumption. The operation is divided into four phases: the sampling, hold, latch, and reset phases. In the sampling phase, the latching clock signal (QL) is low and the switches S_1–S_4 are turned on. Then, M_7 and M_8 are turned on, M_3 and M_4 are operated in the linear region, and V_{XP}, V_{XN}, and V_X are shorted together, as shown in Fig. 4(b). Since node V_X is biased with the diode-connected transistors of M_3 and M_4, the parasitic capacitor of node V_X (C_{PX}) is charged by the subthreshold currents $I_{X,M3}$ and $I_{X,M4}$. When V_X reaches VDD-V_{TH}, M_3 and M_4 are cut off, where VDD and V_{TH} are a supply voltage and the transistor threshold voltage, respectively. The bottom plates of the gate capacitor are then tied to the fixed voltage of V_X and the input voltages are sampled across C_{M1} and C_{M2}. C_{M1} and C_{M2} replace the conventional sampling capacitors and V_{mX} replaces the common-mode voltage. The current efficiency of I_X can be improved by reducing the off-state leakage current of M_9. In the next phase, S_3–S_4 and S_1–S_2 are switched off sequentially. When QL increases to a high level, M_9 is turned on, and the differential pair starts to regenerate. The latch duration is asynchronously controlled to reduce the dynamic power further [13]. After latching, OP and ON are connected to VDD and the inputs are shorted together for the reset operation.

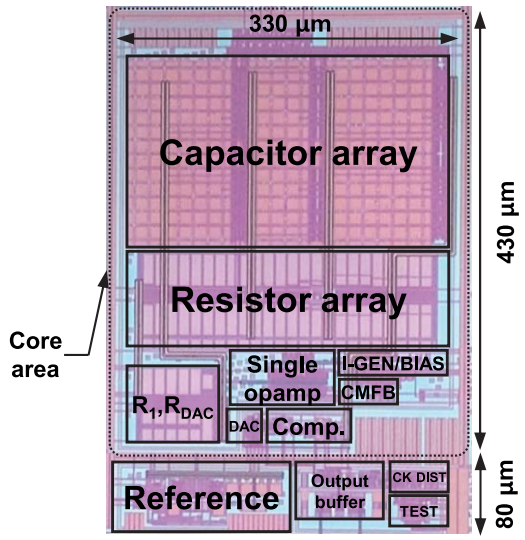

Fig. 5. Chip micrograph.

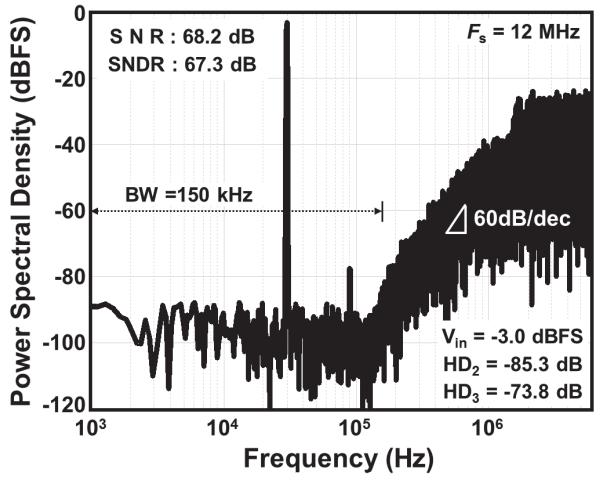

Fig. 6. Measured 65,536-point output spectrum with F_{IN} = 29.5 kHz.

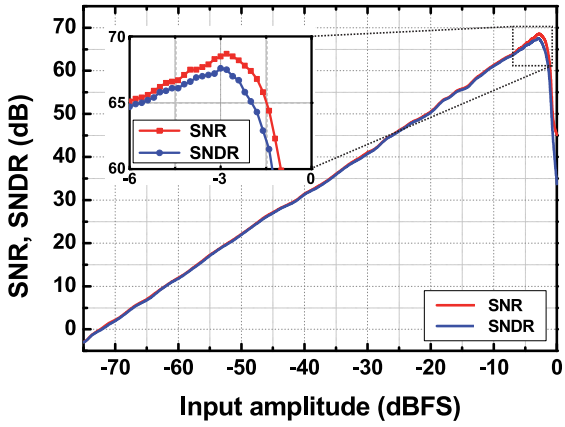

Fig. 7. Measured SNR and SNDR versus input amplitude.

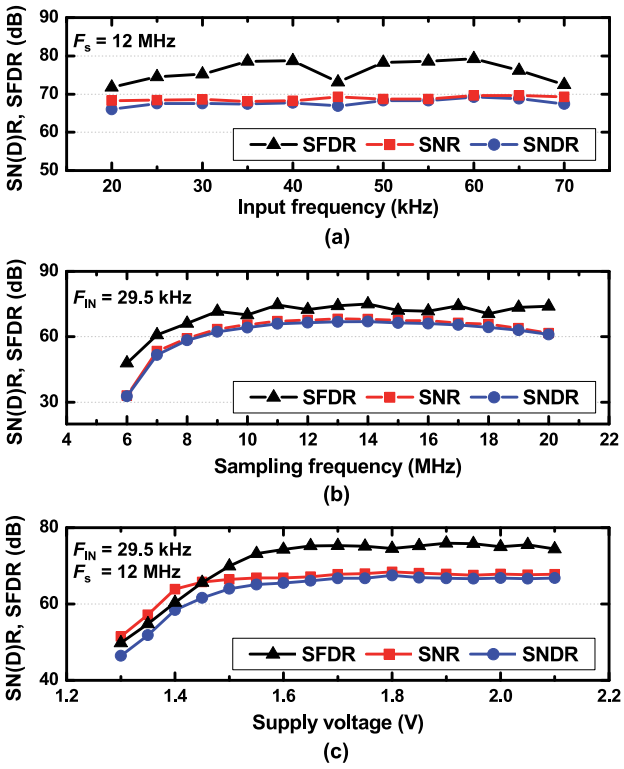

Fig. 8. Measured dynamic performances versus (a) Input frequency, (b) Sampling frequency, and (c) Supply voltage.

IV. Measurement Results

A DSM using a third-order SOR was implemented in a 180-nm CMOS. The chip micrograph is shown in Fig. 5. The active area of the modulator is only 0.14 mm^2. The capacitor and resistor arrays occupy over 80% of the active area. At a 12-MHz sampling rate, the modulator consumes 37.4 µW, of which 20.5 µW is consumed by the analog blocks (SOR and bias) and 16.9 µW by the digital blocks (DAC and comparator) from a 1.8-V supply. Fig. 6 shows the measured 65,536-point output spectrum of the DSM with an input of –3.0 dBFS at 29.5 kHz. The modulator demonstrates a third-order noise-shaping characteristic due to its implementation of the proposed resonator. The measured peak SNDR over a 150-kHz signal bandwidth is 67.3 dB. The third-order harmonic distortion (HD_3) is 73.8 dB below the signal tone, which illustrates the high linearities of both the LF and DAC.

The measured SNR and SNDR are plotted for different input powers for a 29.5-kHz input signal in Fig. 7. The peak SNR of 68.5 dB is achieved at an input of –2.8 dBFS, and a dynamic range (DR) of 72.5 dB is obtained for a 150-kHz bandwidth. The full-scale input signal amplitude (0 dBFS) is set to a 1-V_{p-p} differential. The overall dynamic performance is summarized in Fig. 8. The SNR, SNDR, and spurious-free dynamic range (SFDR) do not deteriorate when the signal frequency is increased up to the Nyquist input bandwidth (Fig. 8(a)). An SNR of 60 dB is maintained over a sampling frequency range from 8 MHz to 20 MHz without any reconfiguration of the prototype (Fig. 8(b)). The modulator remains stable for a wide F_s range, demonstrating its potential for multi-rate operation in CT DSMs. The modulator works well down to a VDD of 1.5 V, but further reduction of the supply voltage gradually degrades its performance (Fig. 8(c)).

TABLE II
PERFORMANCE COMPARISON TO PRIOR WORK: [7]–[10] ARE SINGLE OP-AMP LF ARCHITECTURES; [2]–[4] ARE DSMS WITH A SIMILAR TECHNOLOGY

Reference	This work	[7]	[8]	[9]	[10]	[2]	[3]	[4]
Process (nm)	180	130	90	65	65	180	160	130
VDD (V)	1.8	1.2/1.4	1.2/1.4	-	1.1	1.8	1.8	1.4
F_s (MHz)	12	185	300	186	650	6.144	11.29	256
BW (MHz)	0.15	7.2	8.5	3	10	0.024	0.02	2
OSR	40.0	12.8	17.6	31.0	32.5	128.0	282.3	64.0
DR (dB)	72.5	80	73	69.3	71.2	103.6	107.5	82
Peak SNR (dB)	68.5	78.2	69.3	69.3	69.3	99.3	104.4	80.5
Peak SNDR (dB)	67.3	76.9	67.2	68.8	68.6	98.5	98.3	74.4
Power (mW)	0.0374	13.7	4.3	1.36	1.82	0.28	1.65	5
Area (mm^2)	0.14	1.3	0.12	0.06	0.039	1.334	0.16	0.33
FoMs (dB)*	163.3	164.1	160.2	162.2	166.0	177.8	169.1	160.4
FoMw (fJ/step)**	65.9	166.3	135.1	100.7	41.4	84.8	613.7	291.4

*FoMs=SNDR+10·log(BW/Power), **FoMw=Power/(2·BW·$2^{(SNDR-1.76)/6.02}$)

Table II compares the DSM's performance with those of state-of-the art modulators with similar architectures [7]–[10] and technologies [2]–[4]. The prototype exhibits one of the lowest Walden figures-of-merit (FoMw) [14] (65.9 fJ/conv.-step) and smallest active areas (0.14 mm^2) among the DSMs using 180-nm CMOS technology. Even if extended to 130 nm [4], [6], [7], [15], the proposed DSM continues to demonstrate a competitive FoMw. In addition, the Schreier FoM (FoMs) [15] of 163.3 dB is successfully achieved.

V. CONCLUSION

A power- and area-efficient single-bit CT DSM was proposed. A resonant single op-amp third-order LF that was achieved by positive feedback reduced the number of active components and simplified the hardware complexity. In addition, an autonomous common-mode dynamic comparator eliminates the sampling capacitor and common-mode voltage. The measurement results indicated that these techniques enable power-efficient operation while allowing for both a compact area and a flexible design. Consequently, the DSM exhibits a competitive FoMw of 65.9 fJ/conv.-step and an active area of 0.14 mm^2. The proposed DSM is expected to be a potential solution to problems in several applications, including sensor interfaces, power management integrated circuits, and wireless systems.

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