Self-Biased Differential Rectifier With Enhanced Dynamic Range for Wireless Powering

Mahmoud H. Ouda, *Student Member, IEEE*, Waleed Khalil, *Senior Member, IEEE*, and Khaled N. Salama, *Senior Member, IEEE*

***Abstract*—A self-biased cross-coupled differential rectifier is proposed with enhanced power-conversion efficiency (PCE) over an extended range of input power. A prototype is designed for ultrahigh-frequency (UHF) 433-MHz radio-frequency power-harvesting applications and is implemented using a 0.18-μm CMOS technology. The proposed rectifier architecture is compared with the conventional cross-coupled rectifier. It demonstrates an improvement of more than 40% in the rectifier PCE and an input power range extension of more than 50% relative to the conventional cross-coupled rectifier. A sensitivity of −15.2-dBm (30-μW) input power for 1-V output voltage and a peak PCE of 65% are achieved for a 50-kΩ load.**

***Index Terms*—AC-to-DC power converter, adaptive, energy harvesting, radio-frequency identification (RFID), rectifier, self-biased, wireless powering.**

I. Introduction

WIRELESS power transfer (WPT) applications range from powering batteryless wireless sensors [1], radio–frequency (RF) identification (RFID) [2], and implantable devices [3]–[5], to the higher scale of space-based solar cells and wirelessly charged electric vehicles. It utilizes various frequency bands starting from low megahertz for low-power implants [4], [5] to ultrahigh-frequency (UHF) RFID tags [2], including a 433-MHz industrial, scientific, and medical (ISM) band [6] that is used for license-free communication, underwater wireless-sensor networks [7], and automotive applications such as batteryless tire-pressure monitoring systems [8]. Among this myriad of batteryless devices, the wireless power receiver is considered the linchpin for any given WPT system.

As shown in Fig. 1, the RF-to-dc power converter is the core of any wireless power receiver that supplies usable dc power out of the incoming RF power to the antenna. Recently, an RF-to-dc power converter has been used for recycling wasted RF power in hybrid duplexers and enhancing the power amplifier efficiency [9]. The RF-to-dc power converter performance is evaluated in terms of two main parameters: 1) sensitivity, which defines the minimum input RF power required to generate a specific dc output voltage, and 2) power-conversion efficiency

Manuscript received May 7, 2016; revised July 11, 2016; accepted July 12, 2016. Date of publication August 29, 2016; date of current version April 28, 2017. This brief was recommended by Associate Editor S. C. Wong.

M. H. Ouda and K. N. Salama are with King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia (e-mail: mahmoud.ouda@kaust.edu.sa; khaled.salama@kaust.edu.sa).

W. Khalil is with the Electro Science Laboratory, The Ohio State University, Columbus, OH 43212 USA (e-mail: khalil@ece.osu.edu).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2016.2591263

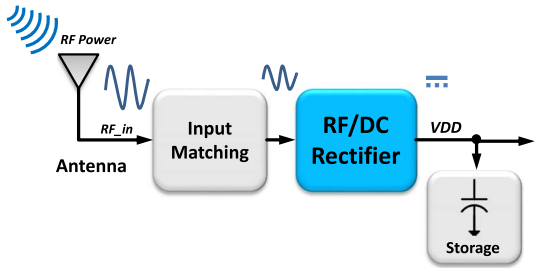

Fig. 1. Block diagram of the wireless power receiver.

(PCE), which is the ratio of the usable output dc power P_o to the input RF power P_i and can be expressed by

$$\text{PCE} = \frac{P_o}{P_i} = \frac{P_o}{P_o + P_{\text{diss}} + P_{\text{rvs}}} \tag{1}$$

where the input power P_i is equal to the summation of the output dc power P_o, the dissipated power in rectifying devices P_{diss} and the reverse leakage power P_{rvs}, which is caused by the nonidealities in the reverse characteristic of the rectifying device.

Traditionally, ac–dc power converters have been realized using diode-based architectures, such as the Greinacher cell, the Dickson multiplier [10], or a full-wave bridge rectifier [11]. Diode-based rectifiers have simply been realized in CMOS technology using diode-connected transistors, such as the Dickson rectifier shown in Fig. 2(a). However, they suffer from poor sensitivity at low input power and from high dropout voltage that degrades their PCE at mid-high input power. Enhanced sensitivity can be achieved either by using Schottky diodes that require additional fabrication steps and, hence, are seldom offered in conventional CMOS processes or by using an integrated step-up transformer occupying a large area [12]. On the other hand, the differential fully cross-coupled (FX) rectifier [2], as shown in Fig. 2(b), is widely used in RFID applications, due to its improved sensitivity and high peak efficiency. However, this improvement is gained at the expense of the reverse characteristic of the rectifying devices because the rectifying cross-coupled transistor is still a bidirectional device, unlike diodes or diode-connected transistors. Hence, it conducts in a reverse direction once the instantaneous value of the RF signal V_{RF} becomes lower than the output dc voltage V_{DD} in every RF cycle, as shown in Fig. 3(a). This periodic reverse leakage is exacerbated as the RF power level grows, degrading the rectifier conversion efficiency at high input power, as shown in Fig. 3(b). Consequently, the rectifier operates efficiently within a limited range of input power. To evaluate different rectifier

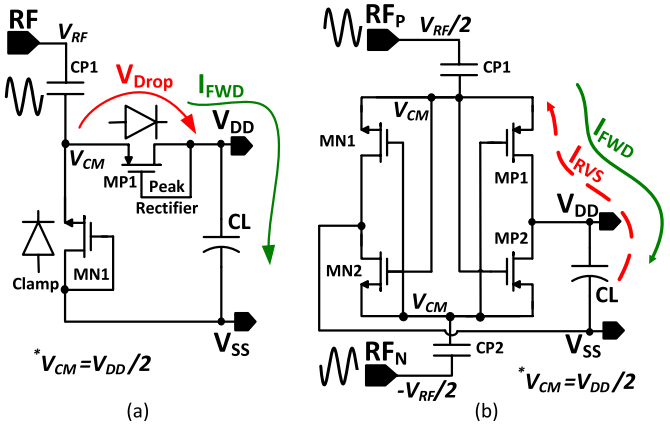

Fig. 2. Schematic of (a) the Dickson rectifier and (b) the conventional FX rectifier.

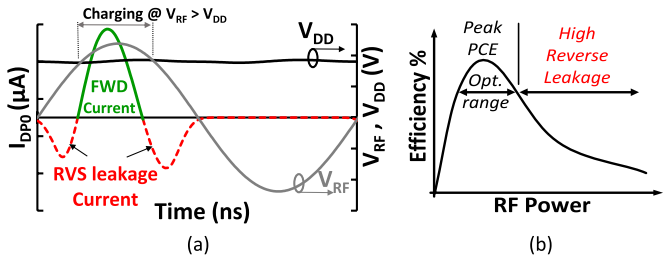

Fig. 3. (a) Conventional FX rectifier efficiency versus RF power and (b) its alternating current, output dc voltage, and RF voltage.

architectures, a dynamic range is defined as the input power range at which the rectifier maintains a PCE higher than 80% of its peak efficiency [13].

In [4] and [5], a low-megahertz adaptive architecture reconfigures the rectifier stage as a diode-connected voltage doubler or as a half cross-coupled rectifier based on the input power level. However, it requires active diodes driven by fast comparators that are not power efficient at high RF frequencies, such as UHF 433 MHz or higher. A multistage configuration is presented in [13] and [14] to enhance the efficiency of the cross-coupled rectifier by rewiring stages as a series or parallel multistage rectifier. Although this technique extends the efficiency of the cross-coupled rectifier over a wide range of input power, it requires multiple stages with high input capacitance and low input resistance, thus complicating the matching network design. In [15], an adaptive offset calibration technique is presented to compensate the threshold voltage $V_{\rm th}$ in diode-based rectifiers to improve their sensitivity. However, it requires two more auxiliary multistage rectifiers to compensate the $V_{\rm th}$ of the main rectifier, thus occupying a large area, adding more losses and degrading the PCE.

In this brief, we propose and experimentally validate a self-biased cross-coupled differential CMOS rectifier with enhanced efficiency over a wider input range than both diode-connected and cross-coupled rectifiers. This facilitates reliable and efficient RF-to-dc power conversion at varying RF power levels, and it adds more spatial freedom between the wireless power transmitter and receiver. The proposed architecture is illustrated along with its operational concept in Section II, whereas the

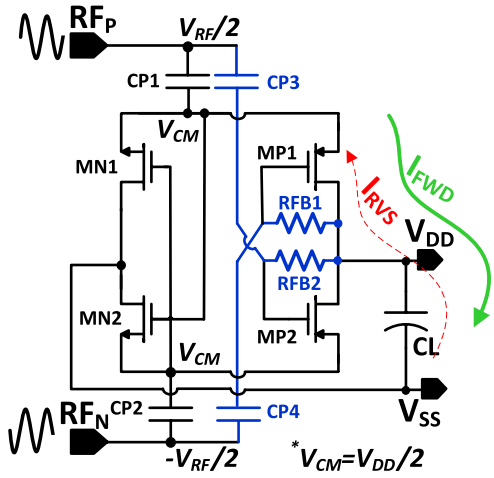

Fig. 4. Schematic of the proposed self-biased cross-coupled rectifier.

experimental results are discussed and compared with measurements of a fabricated conventional FX rectifier in Section III. Finally, the conclusion is drawn in Section IV.

II. Proposed RF-to-DC Power Converter

A. Proposed Architecture

A schematic of the proposed self-biased cross-coupled rectifier is shown in Fig. 4. The rectifier utilizes the cross-coupled configuration with the differential-drive capability, to maintain good sensitivity at low input power, by operating in the linear region and holding low dropout voltage. Moreover, a self-biasing mechanism is added to limit the reverse leakage at the sense of high input power. The proposed self-biasing mechanism controls the conduction of the rectifying devices by raising their effective turn-on voltage at high RF power levels. A simple implementation of this mechanism is achieved by applying the output dc voltage directly to the controlling gates of the rectifying transistors (MP1,2) without disturbing the RF signal at the differential inputs. This is achieved by decoupling the dc voltage of the rectifying pMOS MP1,2 gates from their corresponding nMOS MN1,2 using (CP3,4) and then applying the dc self-bias using an RF choke (RFC) coil that is a dc short circuit and an ac open circuit. It is worth noting that the self-biasing branch is connected to a MOSFET gate; hence, no dc current passes through it, whereas the self-biasing RFC branches can be simply replaced by high feedback resistors (RFB1, RFB2 $\simeq$ 100 kΩ) without loading the RF inputs, as shown in Fig. 4.

B. Operational Concept

The operating point of the proposed self-biased cross-coupled rectifying device is compared with the conventional cross-coupled and diode-connected rectifying devices in Fig. 5. Each rectifying device connects the ac-coupled RF node (RF superimposed on a common mode $V_{\rm CM} = V_{\rm DD}/2$) at its input terminal to the output $V_{\rm DD}$ point. As shown in Fig. 5(a), the gate and drain of the diode-connected device are tied to the output $V_{\rm DD}$ to act as a two-terminal diode. In the case of the conventional cross-coupled device, the gate is attached to the $\rm RF_N$ node ($= -V_{\rm RF}/2$ superimposed on $V_{\rm DD}/2$), as shown

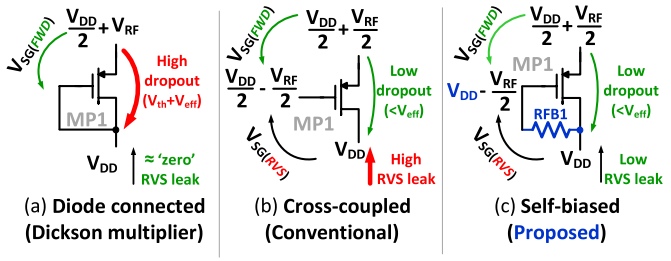

Fig. 5. Operating point of the rectifying device (MP1) configured (a) as a diode-connected transistor (Dickson rectifier), (b) as a cross-coupled transistor, and (c) as a self-biased transistor (proposed rectifier).

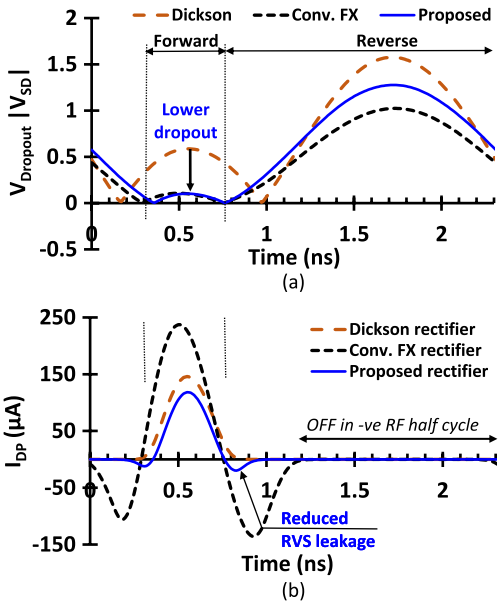

Fig. 6. Simulation of (a) dropout voltage $V_{\rm SD}$ and (b) drain current $I_{\rm DP}$ in the rectifying pMOS devices of the Dickson, conventional FX, and proposed rectifiers at 37-μW input power level.

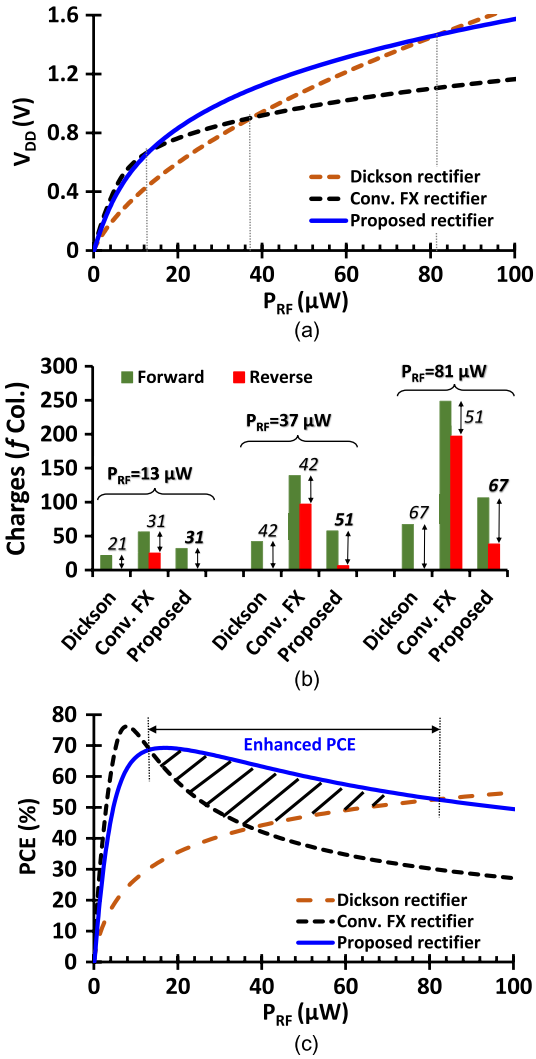

Fig. 7. (a) Simulated output voltage, (b) alternating charges flowing in MP1 per RF cycle (Qp), and (c) PCE for the Dickson, conventional FX, and proposed rectifiers versus RF input power.

in Fig. 5(b). However, in the proposed self-biased cross-coupled device, the gate RF_N signal is superimposed on $V_{\rm DD}$, as shown in Fig. 5(c). Note that both the proposed self-biased cross-coupled device and the diode-connected device need minimum turn-on RF voltage $V_{\rm RF\,min}$ equal to threshold voltage $V_{\rm th}$ plus $V_{\rm DD}/2$. This is unlike the conventional cross-coupled device, which requires $V_{\rm th}$ only. Moreover, the proposed device conducts in the linear region and holds a dropout voltage of less than or equal to its overdrive voltage $V_{\rm eff}$, passing higher output voltage than the diode-connected device, which requires a dropout of $V_{\rm th}+V_{\rm eff}$. As a result, the proposed self-biased cross-coupled device retains moderate sensitivity (i.e., it generates higher output voltage at the same RF input power) compared with the diode-connected device. This is derived from the operating points shown in Fig. 5 and it matches the simulated dropout voltages of the three rectifiers at the same input power, as shown in Fig. 6(a).

During the periodic RF signal transitions, the reverse leakage of the diode-connected device is negligible, whereas the conventional cross-coupled device is strongly biased by $V_{\rm SG(RVS)}=V_{\rm RF}/2+V_{\rm DD}/2$ in the reverse direction, as derived in Fig. 5. Accordingly, the reverse current lobes increase, as shown in Fig. 6(b). On the other hand, as shown in Fig. 5, the proposed device is biased only at $V_{\rm SG(RVS)}=V_{\rm RF}/2$, leading to reduced reverse current lobes, as shown in Fig. 6(b). It is worth noting that, during the negative RF half-cycle, the gate

TABLE I
COMPARISON OF RECTIFYING DEVICES

Rectifier	Dickson	Conv. FX	Proposed
Device	D-connected	X-coupled	**Self-biased**
Turn–on[1] (V_{RFmin})	High (=$V_{DD}/2+V_{th}$)	Low (=V_{th})	**High (=$V_{DD}/2+V_{th}$)**
Dropout[2] (V_{drop})	High (Sat.) (=$V_{th}+V_{eff}$)	Low (Linear) (=V_{eff})	**Low (Linear) (=V_{eff})**
Sensitivity[3]	Poor	Good	**Moderate**
RVS leak	Negligible	High, $I_{d\ MOS}$	**Low**
RVS Leakage Range[4]	Negligible leak $V_{RF}>V_{breakdown}$	Wide leak $2V_{th}-V_{DD}<V_{RF}<V_{RF}<V_{DD}$	**Low leak $2V_{th}<V_{RF}$ $V_{RF}<V_{DD}$**
Efficiency (PCE)	Low peak	High peak	**Good peak**
	Moderate-range	Narrow-range	**Wide-range**

[1] *Turn-on at $V_{SG} > V_{th}$.*
[2] *Dropout* affects sensitivity, output voltage and efficiency.
[3] *Sensitivity: turn on at low V_{RF} & with low dropout voltage.*
[4] *Reverse leakage if ($V_{SG\,(RVS)} > V_{th}$) & ($V_{SD\,(RVS)} > 0$).*

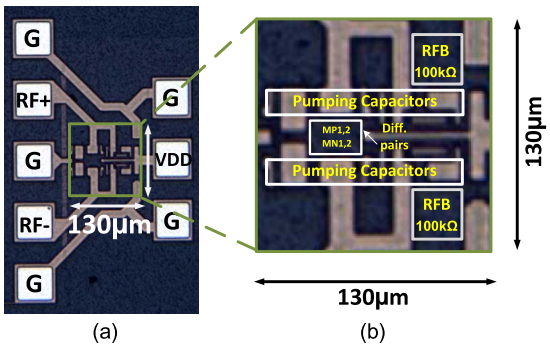

Fig. 8. Die microphotograph of (a) the proposed self-biased rectifier and (b) enlarged view of active area with the feedback resistors are highlighted.

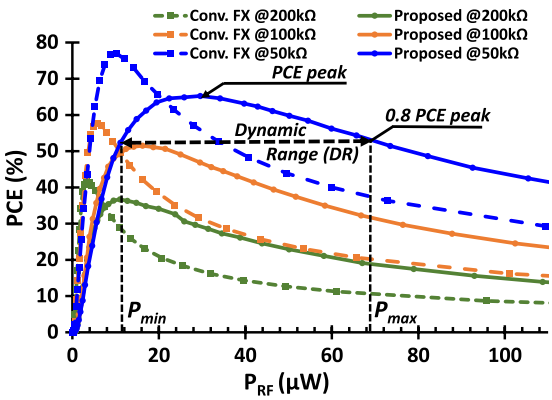

Fig. 9. Measured PCE of the proposed (solid) and conventional FX (dash) rectifiers versus input power, for three loads.

of the MP1 in the conventional FX and proposed rectifiers is positively biased, shutting down its current completely, similar to the reverse-biased diode-connected device.

Fig. 7(a) shows the simulation of the output voltage versus the input power, for all three rectifiers, for a load of 50 kΩ. At low RF power, the proposed rectifier outperforms the Dickson rectifier, whereas it outperforms the FX rectifier at high RF power. This can be explained by plotting both the forward harvested charges and the reverse leakage charges at three distinct RF power levels, as shown in Fig. 7(b). The simulated PCE of the three rectifiers versus input power is plotted in Fig. 7(c). As shown in Fig. 7, the conventional FX rectifier has a peak PCE at low RF power, but it falls off rapidly due to its high reverse leakage current, which is shown in Fig. 6(b). On the other hand, the Dickson (diode-based) rectifier displays a moderate PCE at the high RF power levels but suffers from poor efficiency at low input power due to its high dropout voltage, as shown in Fig. 6(a). Conversely, the proposed rectifier achieves a wider dynamic range with a slight decrease in its peak PCE relative to the conventional FX rectifier.

A comparison of the three rectifying devices is summarized in Table I, where the proposed self-biased rectifying device shows competitive advantages of low dropout voltage, as shown in Fig. 6(a), and hence low dissipation loss and better sensitivity than the diode-connected device. At the same time, the proposed rectifying device shows lower reverse leakage and wider input range than the conventional cross-coupled device, as shown in Figs. 6(b) and 7(c), respectively.

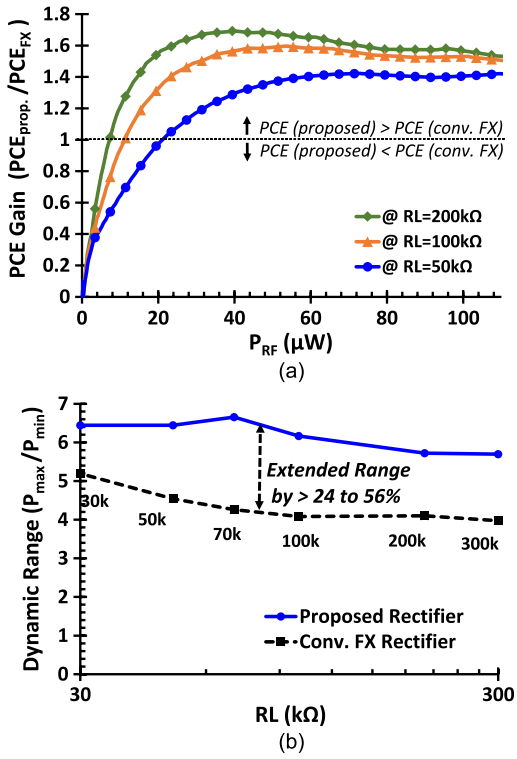

Fig. 10. (a) Measured ratio of the proposed rectifier PCE relative to the conventional FX rectifier PCE for three different loads. (b) Measured dynamic range of the proposed and conventional rectifiers.

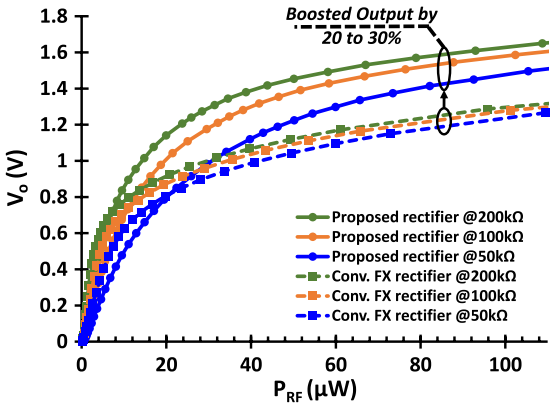

Fig. 11. Measured output dc voltage of the proposed and conventional FX rectifiers at 433 MHz versus RF input power for various loads.

III. Results and Discussion

The proposed rectifier is implemented in a 0.18-μm CMOS process technology and occupies a 130 μm $\times$ 130 μm active area. The die microphotograph is shown in Fig. 8. A conventional FX rectifier is implemented on the same die for a fair comparison with the proposed rectifier, using identical test setup and conditions. The RF measurement setup includes an Agilent vector network analyzer (N5225A) and a digital multimeter (34420A). The rectifier's PCE is measured with a single-tone 433-MHz signal at different input power levels, and the output dc voltage is recorded. After deembedding the reflection and transmission losses, the net input power is calculated and the PCE for the proposed and conventional rectifiers is plotted in Fig. 9 versus the input power at different loads. Although the proposed rectifier has lower peak PCE

TABLE II
PERFORMANCE COMPARISON

Ref	CMOS Process	Architecture	# stages	Chip Area (mm^2)	Frequency	Sensitivity P_{RF}@V_o=1V	Load (R_L)	Peak PCE	Dynamic Range[a] P_{max}/P_{min}
This Work	**0.18 μm**	**Adaptive self-biased cross-connected rectifier (Proposed)**	**1-stage**	**0.017**	**433 MHz**	**-15.2 dBm**	**50 $k\Omega$**	**65.3 %**	**6.5**
						-17 dBm	**100 $k\Omega$**	**51.5 %**	**6.2**
This Work	0.18 μm	Fully cross-coupled (FX) rectifier (Conventional)	1-stage	0.005	433 MHz	-13.6 dBm	50 $k\Omega$	77 %	4.5
						-14.5 dBm	100 $k\Omega$	57.5 %	4.1
[6]	0.18 μm	Fully cross-coupled with inter-stage RF injection	3-stage	0.088	433 MHz	-7.8 dBm	30 $k\Omega$	13.2 %	3.2
						-4.1 dBm	100 $k\Omega$	10 %	3
[15]	0.18 μm	Dickson rectifier with multiple-V_{th} offset cancellation.	4-stage	0.15	433 MHz	-11.2 dBm	50 $k\Omega$	32 %	4.2
						-14 dBm	100 $k\Omega$	34 %	4.7
[16]	0.18 μm	Hybrid V_{th} cancellation using RF input & DC output voltage	1-stage	NA	433 MHz	$>$ 0 dBm[b]	30 $k\Omega$	12.5 %	3.3
						$>$ 0 dBm[b]	100 $k\Omega$	4.6 %	3.6

[a] Input power range of PCE$\geqslant$0.8 Peak PCE.
[b] $0\,dBm$ for $Vo = 0.78V$.

($\simeq$65%) than the conventional rectifier, whose peak PCE is $\simeq$75%, the proposed architecture maintains its PCE over a broader dynamic range of input power. Thus, the proposed rectifier can operate efficiently at different RF power levels, enabling robust wireless powering from varying transmission distances or within unstable environments.

To elucidate the relative PCE enhancement of the proposed rectifier, the ratio of the proposed rectifier PCE over the conventional FX rectifier PCE is plotted in Fig. 10(a), for variable loads $R_L = 50$, 100, and 200 kΩ. An approximately 40%–70% efficiency improvement is achieved in the proposed rectifier at mid-high input power (> 30 μW) relative to the conventional FX rectifier, as shown in Fig. 10(a). Moreover, the proposed rectifier maintains the achieved improvement in PCE over a wide input range at different loading conditions, as shown in Figs. 9 and 10(a). To further illustrate this point, the dynamic range of input power [$P_{\min}$ to $P_{\max}$] at which the rectifier maintains 80% of its peak efficiency is represented as the ratio of $P_{\max}$ over $P_{\min}$ and is compared in Fig. 10(b), for the proposed and conventional FX rectifiers, versus different loading conditions. Evidently, the proposed rectifier achieves a higher dynamic range across a wide range of loading conditions (from 30 to 300 kΩ). Fig. 11 shows the measured output dc voltage versus input power level for the proposed and conventional FX rectifiers equally loaded by 50, 100, and 200 kΩ. At the same input power, the proposed self-biased rectifier delivers higher dc output voltage than the conventional FX rectifier by 20%–30%.

A performance comparison of the proposed rectifier versus the recent ISM 433-MHz rectifiers is summarized in Table II. The proposed rectifier shows 2$\times$ improvement in dynamic range and 5$\times$ enhancement in efficiency relative to the architecture in [6]. More than 50% wider dynamic range and doubled efficiency is achieved, as compared with the architecture in [15], with 9$\times$ chip area saving.

IV. CONCLUSION

In this brief, we have proposed a self-biased cross-coupled differential rectifier with 50% enhanced PCE over a wide range of input power levels and under different loading conditions. A sensitivity of $P_{\rm RF} = 30$ μW at $V_o = 1$ V and peak PCE $= 65.3\%$ are achieved for a 50-kΩ load. The architecture of the proposed rectifier is presented and its performance is compared with the conventional cross-coupled rectifier.

REFERENCES

[1] Y.-J. Kim, H. S. Bhamra, J. Joseph, and P. P. Irazoqui, "An ultra-low-power RF energy-harvesting transceiver for multiple-node sensor application," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 11, pp. 1028–1032, Nov. 2015.

[2] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009.

[3] M. H. Ouda, M. Arsalan, L. Marnat, A. Shamim, and K. N. Salama, "5.2-GHz RF power harvesting module in 0.18 μm CMOS for biomedical implantable sensors," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 5, pp. 1–8, May 2013.

[4] X. Li, C. Ying Tsui, and W.-H. Ki, "Power management analysis of inductively-powered implants with 1X/2X reconfigurable rectifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 3, pp. 617–624, Mar. 2015.

[5] H.-M. Lee and M. Ghovanloo, "An adaptive reconfigurable active voltage doubler/rectifier for extended-range inductive power transmission," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 8, pp. 481–485, Aug. 2012.

[6] S. S. Chouhan and K. Halonen, "A novel cascading scheme to improve the performance of voltage multiplier circuits," *Analog Integr. Circ. Sig. Process*, vol. 84, no. 3, pp. 373–381, 2015.

[7] A. A. Abdou *et al.*, "A matched Bow-tie antenna at 433 MHz for use in underwater wireless sensor networks," *J. Phys., Conf. Ser.*, vol. 450, no. 1, 2013, Art. no. 012048.

[8] J. Zhu, L. Wu, X. Zhang, C. Jia, and C. Zhang, "A low-power 433 MHz transmitter for battery-less tire pressure monitoring system," in *Proc. IEEE 9th Int. Conf. ASICON*, Oct. 2011, pp. 184–187.

[9] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "An RF–DC converter with wide-dynamic-range input matching for power recovery applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 6, pp. 336–340, Jun. 2013.

[10] J. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976.

[11] S. Dwari, R. Dayal, L. Parsa, and K. N. Salama, "Efficient direct ac-to-dc converters for vibration-based low voltage energy harvesting," in *Proc. IEEE 34th IECON*, Nov. 2008, pp. 2320–2325.

[12] H. Goncalves, M. Martins, and J. Fernandes, "Fully integrated energy harvesting circuit with $-$25-dBm sensitivity using transformer matching," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 5, pp. 446–450, May 2015.

[13] C.-J. Li and T.-C. Lee, "2.4-GHz high-efficiency adaptive power harvester," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 434–438, Feb. 2014.

[14] L. B. A. Scorcioni and S. Larcher, "A reconfigurable differential CMOS RF energy scavenger with 60% peak efficiency and $-$21 dBm sensitivity," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 3, pp. 155–157, Mar. 2013.

[15] K. Gharehbaghi, O. Zorlu, F. Kocer, and H. Kulah, "Auto-calibrating threshold compensation technique for RF energy harvesters," in *Proc. IEEE RFIC Symp.*, May 2015, pp. 179–182.

[16] S. S. Chouhan and K. Halonen, "Threshold voltage compensation scheme for RF-to-DC converter used in RFID applications," *Electron. Lett.*, vol. 51, no. 12, pp. 892–894, 2015.