32 dBm IP1dB / 46 dBm IIP3 GaN Phase-Amplitude Setting Circuit at Ku-band

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***Abstract*—Design and characterization of a 6-bit Phase and Amplitude Setting circuit realized in Gallium Nitride MMIC technology operating in Ku-band are reported in this brief. An analysis of transistor periphery selection is provided in order to fulfil linearity parameters concurrently targeting other design constraints such as switch isolation and size. It is shown that a trade-off between the contrasting goals of switch power handling (expressed in terms of 1dB compression point) and switch isolation should be addressed. The proposed linear versus nonlinear performance analysis is uncommon in the open literature since high power analysis is seldom treated in multi-bit phase and amplitude control circuits and even more valuable considering the relatively higher targeted operating bandwidth than previously published material. A useful insight into some design trade-offs required when synthesizing this class of circuits at Ku-band or above are here provided. State-of-the-art +32 dBm Input power at 1 dB compression point and + 46 dBm Input referred Third Order Intercept Point at Ku-band (13 - 17 GHz) are verified outclassing other technologies such as Gallium Arsenide or Silicon Germanium by a factor of 10 - 20 dB. The MMIC is an initial demonstrator targeting highly integrated circuits such as Gallium Nitride core-chips.**

***Index Terms*—Attenuators, Gallium Nitride, K-band, MMICs, Phase shifters.**

I. Introduction

GALLIUM Nitride (GaN) has become in the last 10 to 15 years the reference semiconductor for microwave and millimetre wave circuits in front-end electronic systems for telecommunications back-haul or high-end applications such as aerospace and defence [1], [2]. GaN's high breakdown voltage allows operating it at drain voltages that are far greater than the corresponding Gallium Arsenide (GaAs) value leading to power densities which are 3 to 5 times higher than GaAs. However, less material has been analyzed and proposed regarding the application of GaN technology - at microwave and millimetre wave frequencies - for signal conditioning, shaping and generation circuits, such as mixers [3], phase shifter (PS) [4], attenuators (ATT) and Voltage Controlled Oscillators (VCO) [5]. Focusing the attention on PS and ATT functionalities, most circuits reported in the open literature are realized either in Silicon Germanium (SiGe) or in GaAs [6]. These technologies are more mature with respect to GaN and often offer Enhancement/Depletion (E/D) mode transistors so it is possible to integrate digital functionalities . SiGe is a low-cost technology well employed in commercial oriented applications [7]. GaAs, on the other hand, features better electrical performance in terms of linearity and noise [8]. However, GaAs power levels remain far below the power handling capability of GaN circuits, making GaN attractive when signal shaping functionalities in high linearity T/R modules is required [9]. Moreover, recent advancements in Enhancement mode (E-mode) GaN transistor technology [10] are paving the way to circuit concepts new for GaN such as core-chips [11] or even fully integrated GaN front ends. Consequently, these circuits may be composed of amplifying cells interconnected with phase shifting or attenuating cells to improve integration and overall RF performance.

In this brief, a demonstrator MMIC is presented developed in a commercially available GaN 150-nm gate length technology provided by WIN. The goal of the MMIC is to demonstrate high linearity in conjunction with practical insertion loss at Ku-band providing 6-bit Phase and Amplitude Setting (PAS) functionality. The brief is organized as follows: a useful insight into some design trade-offs required when synthesizing this class of GaN circuits at Ku-band or above is provided in Section II, where an in depth analysis of transistor geometry selection is discussed in Section II-C. The latter provides useful design guidelines targeting the trade-off between the contrasting goals of switch isolation and IP1dB (Input referred 1 dB compression point). Finally, MMIC characterization and a benchmark table are provided in Section III demonstrating state-of-the-art results at Ku-band.

II. Design Solutions

The demonstrator MMIC is designed to fulfill the following target requirements: 6-bit PAS circuit (3 bits for phase setting and 3 bits for amplitude setting), 12 dB insertion loss (i.e. 2 dB/bit), more than +30 dBm IP1dB and +40 dBm IIP3 (Input Third Order Intercept Point), 5° and 0.5 dB respectively phase and amplitude RMS error in the 13 to 17 GHz bandwidth considering 50 Ω termination impedance. Phase shift steps are selected so as to provide a reasonable constellation of values covering the entire 0-360° range, while the attenuation values are selected to provide a dynamic range greater than 10 dB. The selected technology is WIN semiconductor's NP15-00. The process is a high power 150-nm gate GaN technology manufactured on 0.1 mm Silicon Carbide substrates. The key

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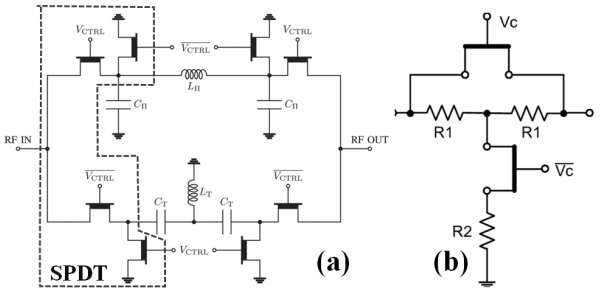

Fig. 1. Schematic diagram of the implemented phase shifter cells (a) and 2 dB attenuation cell (b).

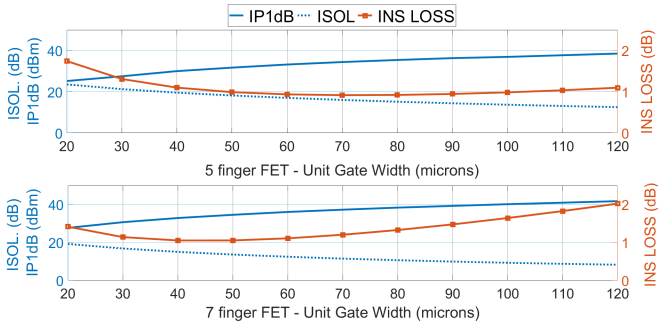

Fig. 2. SPDT insertion Loss, isolation and IP1dB as a function of gate width when employing a 5-finger or 7-finger series FET switch, evaluated at 17 GHz.

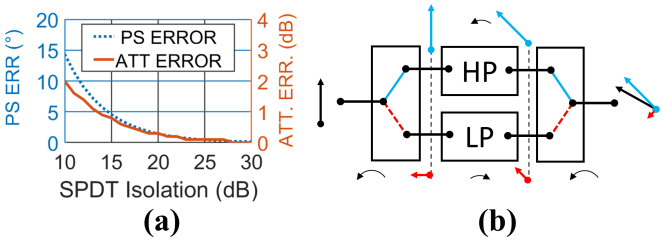

Fig. 3. Left (a): 90° PS cell error 8 dB cell error as a function of SPDT isolation. Right (b): Desired and leaked signals phase relationship at various 90° PS cell sections in the HP 'ON' case. Light blue vectors represent the desired signal while red vectors the unwanted (leaked) signal. Overall input and output signals are depicted in black. Circular arrows indicate phase rotation between the terminals of each section.

figures-of-merit analyzed for high power handling switching applications are: +80 V Gate-to-Drain Breakdown voltage, 2.1 Ω · mm transistor ON-state resistance (R_{ON}) and 0.13 pF/mm transistor OFF-state capacitance (C_{OFF}), yielding 0.3 ps $R_{ON} \times C_{OFF}$ time constant figure-of-merit for the technology when used in switching applications [12].

A. Phase Shifter Design

The three phase shift bits are obtained by switching the path of the RF signal from a phase anticipating cell, implemented in a high-pass 'T' topology (HP-T) , to a phase lagging cell, implemented in a low-pass 'Π' topology (LP-Π), as schematically depicted in Fig. 1 (a). The basic switching element is a single-pole double-throw (SPDT) circuit, whose simplified electrical schematic is also depicted in Fig. 1 (a) inside the dashed line. The synthesized component values, appearing in Fig. 1 (a), are provided in Table I and are obtained using equations reported in [13] and imposing 50 Ω termination condition.

TABLE I
PHASE SHIFTER AND ATTENUATOR CELLS COMPONENT VALUES

cell	L_Π (nH)	C_Π (pF)	L_T (nH)	C_T (pF)		cell	R_1 (Ω)	R_2 (Ω)
45°	0.38	0.09	∞ (open)	∞ (short)		2 dB	25	180
90°	0.38	0.09	0.75	0.51		4 dB	25	220
180°	0.53	0.21	0.53	0.21		8 dB	53	112

B. Attenuator Design

The 3-bit attenuator is designed to exhibit 0-14 dB dynamic by 2 dB steps. The 8 dB and 4 dB cells are synthesized by switching the path of the RF signal from a reference (ideally lossless) path to an attenuating path synthesized through a 'Π' topology resistive network, similar to the (LP-Π) in Fig. 1 (a), obtained by substituting R_1 with L_Π and R_2 with C_Π. The values of the resistors are function of attenuation while imposing the 50 Ω termination condition. In the 2 dB cell, one switch transistor directly connects input to output while another switch transistor connects one port of the resistive 'T' network to ground, as seen in Fig. 1 (b). The two FETs are controlled by a pair of opposite voltages. The resistive component values appearing in Fig. 1 (a) and (b) are provided in Tab. I.

C. Switch Design

Given the high linearity target, a fundamental design step consists in appropriately sizing the periphery of the series and shunt FETs appearing in the various schematics depicted in Fig. 1. At first, the negative (OFF-state) gate control voltage is set to -35 V, just below half the gate-to-drain breakdown voltage, while the positive (ON-state) gate control voltage is set to +0 V. This choice helps to improve dynamic swing when the FET is subject to high input power [14], [15]. Series and shunt FET geometries in the SPDT are chosen to achieve 1 dB insertion loss and +35 dBm input power at 1 dB compression point while guaranteeing adequate isolation. The importance of the latter parameter is treated later on in this section. Regarding IIP3, it is initially assumed to be approximately 10-15 dB higher than IP1dB [4], [16], and subsequently verified by analysis.

The shunt FET size is minimized since it is used to improve isolation, and its geometry is set to 1×40 µm. A study is performed to identify the optimum geometry of the series FET by analyzing data reported in Fig. 2. Here, three key SPDT figures-of-merit of are reported: insertion loss, isolation and IP1dB at the maximum design frequency, 17 GHz. Data are provided for 5-finger and 7-finger series FET switch, while sweeping the Unit Gate Width (UGW) of the transistor from 20 to 120 µm. The overall analysis space corresponds to FET total gate width ranging from 100 to 840 µm. The rationale for total gate width lower and upper limit is: smaller series FET geometries would lead to poorer insertion loss while larger

geometries to unpractical isolation values. As expected, the 7-finger demonstrates better power handling capability (IP1dB) about 2 dB higher than the 5-finger counterpart. However its isolation and insertion loss are slightly worse, especially as UGW increases.

An important aspect in switch design for phase shifters and attenuators is isolation and its impact on phase shift and attenuation [17]. Fig. 3 (a) shows the phase and amplitude error (meaning deviation from the ideal "high isolation" case) of the 90° PS and 8 dB ATT cells when the SPDT isolation is swept from 10 to 30 dB. In practice, as isolation worsens, the contribution of the signal leaked through the isolated path is no longer negligible and will produce some effect at the cell's output. This simplified vector sum effect between wanted and unwanted (leaked) signal is visible in Fig. 3 (b), where the HP 'ON' case is considered. In this simplified approach, the SPDT thru path is modelled as purely resisitive (i.e no insertion phase change is applied), while the SPDT isolated path as purely capacitive, and therefore the signal is simultaneously attenuated and rotated counter-clockwise by a quarter turn. The vector sum effect at the output is shown, and the error increases as the leaked signal's magnitude becomes larger due to worse SPDT isolation. In principle such effect can be compensated by tuning the resistive and inductive elements values appearing in the schematics. However, it could be inadvisable to do so, since exact tuning heavily depends on the actual SPDT isolation value that can be correctly determined only if a reliable small signal equivalent circuit model of the cold-FET (i.e at V_{DS} = 0 V) is available for the designer. If this is not the case, then at least 18-20 dB isolation should be implemented at SPDT level. Consequently, if such design constraint is applied, SPDT IP1dB cannot be better than +34 dBm as seen in Fig. 2 for the 5-finger transistor case. Since this IP1dB value is rather close to the target value, a 7×40 µm device is selected for the series FET in the SPDT of the 180° cell, that is the first block of the RF chain (IP1dB bottleneck) while accepting worse isolation, and select 5×40 µm devices in all other SPDT circuits. The geometry of the two transistors shown in the 2 dB cell (Fig. 1 (b) is determined applying a method similar to the SPDT: the series FET is determined to be 3×50 µm while the shunt FET geometry is set to 1×50 µm. Finally, a resistor (not appearing the various schematics depicted in Fig. 1) is inserted between each FET's gate terminal and the corresponding control voltage. Its role is to isolate the RF path from DC. Larger values would lead to higher switching-time. A trade-off between the latter parameter and power handling is performed showing that values in the region of 3 to 6 kΩ provide acceptable switching-time, in the order of a few nanoseconds, and power-handling trade-off. The switching time here provided does not take into account trapping effects that occasionally occur in GaN technology. Anyhow, the PAS switching speed will not be the system's bottleneck that is usually limited by the HPA turn-on time or T/R switch setting time [18].

D. PAS functionality integration

PAS functionality is fulfilled by cascading the six cells in this order: 180°, 90°, 8 dB, 45°, 4 dB, and 2 dB. Cell order is selected by imposing a minimization of cascade RMS error [19] and to maximize IP1dB as discussed in the previous section. IIP3 is also simulated and verified to be typically 10-12 dB higher than input referred 1 dB compression point. Design phase shift is practically ideal at centre frequency and the parasitic phase change due to attenuator switching is contained in ± 2° at mid-band and ± 4° at band edges. Likewise, design attenuation is practically ideal at centre frequency and the parasitic gain change due to phase cells switching is contained in ± 0.15 dB. The circuit is designed in Cadence's AWR v16 environment running EM analysis with AXIEM solver. Finally, chip micro-photograph is shown in Fig. 4 and cell position inside the circuit is also provided.

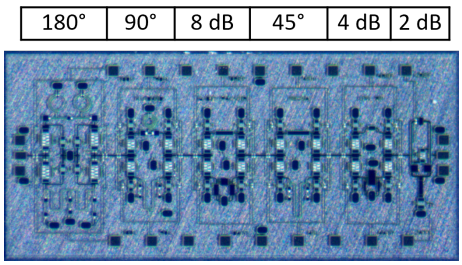

Fig. 4. 6-bit PAS GaN MMIC micro-photograph. Chip size is 3.7 mm × 2.1 mm.

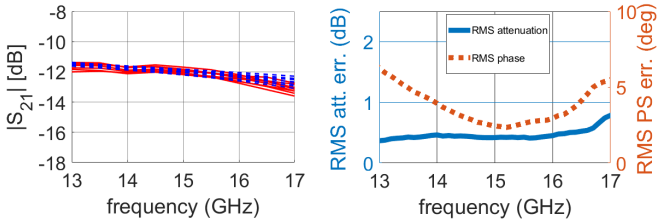

Fig. 5. Left: Insertion loss at minimum attenuation while varying the phase states. Blue dashed lines are simulations while red solid lines are measurements. Right: Measured phase (dashed orange line, right axis) and amplitude (blue solid line, left axis) RMS setting error versus frequency for all 64 states.

III. Characterization

The MMIC is tested on wafer at the operating frequency to verify its electrical performance. Linear and nonlinear measurements are acquired and compared to simulated values.

A. Linear characterization

The first analysis consists in evaluating the MMIC's insertion loss at minimum attenuation setting while varying the phase shifter states. Measured insertion loss spread is slightly higher than expected when changing phase state and the average insertion loss is 0.7 dB higher than simulations. The latter effect is likely due to an underestimation of substrate losses used in EM stack-up and the transistor's ON-state resistance (R_{ON}). Return loss at I/O ports is typically better than 14 dB over the operating bandwidth (Fig. 6). $|s_{11}|$ dispersion is affected by the 180° cell reactive behaviour over frequency.

Phase shift and attenuation states are plotted simultaneously in the constellation shown in Fig. 7, containing data at 1

TABLE II
SOA TABLE OF GAN PHASE AND/OR AMPLITUDE SETTING CIRCUITS

REF	TECH.	BW (GHz)	P.S. (# bits)	ATT. (# bits)	I.L. (dB)	I.L. per bit (dB/bit)	RMS PS/ATT (° / dB)	IP1dB (dBm)	IIP3 (dBm)	Area (mm^2)
[9]	GaN-SiC 150 nm	6-12	analog	0	7	N/A	N/A	25	N/R	2.5
[20]	GaN-Si 800 nm	8-12	1	0	2	2	3 / 0.2	38	46	10
[21]	GaN-Si 250 nm	8-12	5	0	14	2.8	6.4 / 0.8	34.8	N/R	23.5
[22]	GaN-Si 100 nm	30-40	6	5	18	1.7	8 / 1	28	N/R	4.2
[23]	GaN-SiC 250 nm	8-12	5	0	13	2.6	4.0 / 0.5	29	N/R	6
[24]	InGaAs 150 nm	31-40	5	0	8.8	1.8	4.7 / 0.6	16	N/R	3.3
[25]	CMOS 40 nm	24-34	3	0	6	2	13 / 1	9	N/R	3.4
T.W.	GaN-SiC 150 nm	13-17	3	3	12	2	3.5 / 0.5	32.5	46	7.8

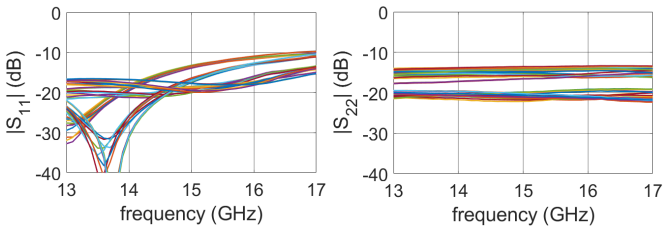

Fig. 6. Measured I/O return loss vs. frequency, all states. (Left) the port connected to 180° cell, (right) the port connected to 2 dB cell.

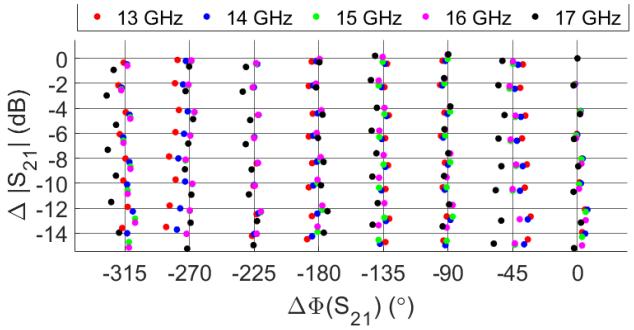

Fig. 7. Measured rectangular phase/amplitude points. All states are normalized with respect to state '000000' (top-right corner state). Data are provided from 13 to 17 GHz at 1 GHz step.

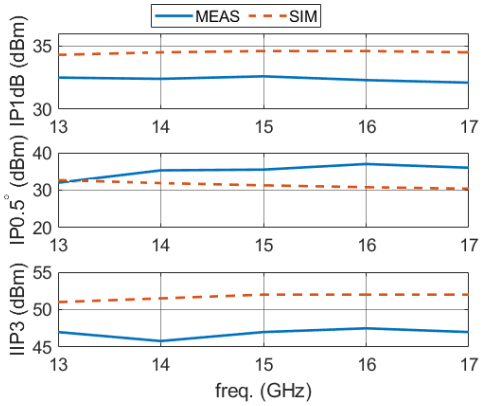

Fig. 8. Measured and simulated input power levels at notable nonlinear conditions from 13 to 17 GHz at state '000000'.

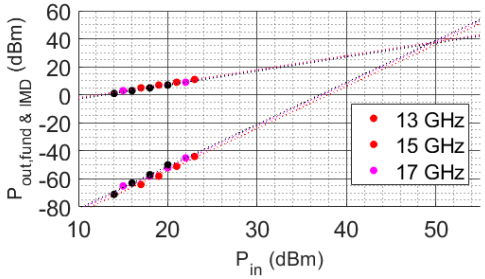

Fig. 9. Measured output power at fundamental frequency and third order inter-modulation distortion (IMD) at 13, 15, and 17 GHz at state '000000'.

GHz step from 13 to 17 GHz. All constellation points are normalized, at each frequency, respect to s_{21} of state '000000'. Therefore, the states in the top right corner are identically 0 phase shift and 0 attenauation. Some attenuation spread versus frequency at higher attenuation settings is visible in this graph. RMS phase and amplitude errors, plotted in Fig. 5 (right). Data are obtained always considering all 64 states. Therefore the parasitic phase change of the attenuator is considered in the RMS phase error and the parasitic insertion loss change of the phase shifter is considered when calculating the RMS amplitude error. The RMS phase error is better than 5° from 13.4 to 16.7 GHz and has a minimum value at 15 GHz that is the design frequency. Practically, the entire RMS phase error at 15 GHz is due to the parasitic phase change of the attenuator block since the PS behaviour at 15 GHz is nearly ideal. RMS amplitude error is constant over frequency since no reactive (frequency resonating) cells are embedded in the attenuator. Once again, most of the RMS ATT error is due to the parasitic insertion loss change of the phase shifter rather than setting errors in the attenuator itself.

B. Nonlinear characterization

Simulations versus measurement comparison is depicted in Fig. 8 for state '000000'. Input referred power levels at three noteworthy nonlinear conditions are provided: 1 dB gain compression point (IP1dB), the power level for which 0.5° AM/PM conversion is observed (IP0.5°), and third order intermodulation intercept point (IIP3). In general, there is good agreement between measured and simulated data. Simulations are better than measurements for IP1dB and IIP3, while the 0.5° AM/PM conversion is higher for the measured value. In

detail, IP1dB is greater than 32.3 dBm, while input power at 0.5° AM/PM distortion is typically better than +35 dBm. Measured IIP3 is around +46 dBm. Fig. 9 reports the output power components, fundamental tone (fund) and intermodulation distortion (IMD) tone, of the two-tone test spaced by 100 MHz. Dashed lines are provided to identify the input and output third order intermodulation points.

C. Benchmarking

Tab. II reports the electrical performance of phase and phase-amplitude shifting circuits operating at or above 10 GHz. The MMIC here presented is one of the few GaN examples containing both phase and amplitude setting functionalities. Moreover, to the best of the Authors' knowledge, it demonstrates the highest measured IP1dB and IIP3 at Ku-band for multi-bit circuits. The insertion loss may appear high, but it is influenced by the higher operating frequency and number of bits with respect to most other references, in particular [20]. The measured circuit I.L. per bit (2 dB/bit) compares very well with other references often targeting lower operating frequencies. Also, the apparently lower IP1dB is justified once again by the higher operating frequency, and most of all from the design constraints (switch isolation versus IP1dB trade-off) expressed in II-C.

IV. Conclusion

Design solutions and characterization of a 6-bit Phase and Amplitude Setting circuit realized in GaN technology operating at Ku-band is reported in this brief. An analysis of isolation versus IP1dB trade-off at SPDT switch level is provided. Such analysis is unusual in the open literature since high power applications are uncommon in phase and amplitude control circuits. More than +32.5 dBm IP1dB and + 46 dBm IIP3 are demonstrated outclassing other technologies such as GaAs or SiGe by a factor of 10-20 dB. To the best of the Authors' knowledge this is the highest power levels reported for GaN phase and amplitude setting circuits operating in Ku-band. The MMIC is an initial demonstrator targeting highly integrated circuits such as GaN core-chips.

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