A Compact DC-110GHz SPST Switch in 22nm FDSOI CMOS

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***Abstract*—This brief reports a compact DC-110GHz single-pole single-throw (SPST) switch in 22nm FDSOI CMOS technology. The switch adopts solely three n-MOSFETs, two of them with a special device option to reduce the substrate parasitic effects, and a third n-MOSFET in parallel to the gate resistance of the series n-MOSFET to improve isolation. Unlike prior wideband mm-wave switches, it does not make use of any large passive components, such as spiral inductors, transformers and transmission lines, which are prone to large parasitic effects, including losses, and require large area on silicon. Altogether, the novel switch circuit allows a very compact design, low losses and high isolation performance. The switch exhibits an insertion loss lower than 3.1 dB, an isolation better than 22 dB, and a return loss better than 12 dB, over the entire frequency range from DC to 110 GHz. The area on die amounts to 160 μm^2, that is up two or more orders of magnitude smaller than prior wideband mm-wave SPST switches.**

***Index Terms*—22nm FDSOI, mm-wave, single-pole single-throw (SPST), switch, wideband.**

I. Introduction

SWITCHES are among the most widely used components in RF and mm-wave systems. In the recent years, some wideband switches were introduced and they adopt inductors/transformers and transmission lines in order to achieve good performance over frequency [1], [2], [3], [4], [5], but with a negative impact as for the area on chip. Fully-depleted silicon-on-insulator (FDSOI) with ultra-thin body and buried-oxide layer allows taking most of the advantage of SOI technology [5] and has been used to implement prior-art switches [1], [3], [4], [6], [7], [8].

In this brief, we report a compact wideband single-pole single-throw (SPST) consisting solely of three n-type metal-oxide-semiconductor field-effect transistors (n-MOSFETs) in 22nm FDSOI complementary metal-oxide-semiconductor (CMOS), two of them with a special device option to reduce the substrate effects, a third n-MOSFET in parallel to the gate resistance of the series n-MOSFET in order to improve isolation, and it does not make any use of spiral inductors, transformers and transmission lines, allowing altogether a very compact design, low losses and high isolation performance from DC to 110 GHz. In [9] we have addressed the cryogenic characterization at 2K of the proposed compact switch as a key circuit, i.e., a "qubit size" switch, toward the implementation of monolithic quantum processors. In this brief we present all the features of the proposed compact switch and its complete experimental characterization at room temperature (300 K) for more general purposes in microwave and mm-wave communication and sensing applications [10], [11], such as radars [12], [13], radiometers [14] and 5G/6G mobile broadband phased-array transceivers [15], [16]. This brief is organized as follows. Section II presents the compact low-loss high-isolation wideband switch. Section III reports the implementation and measurements. Finally, Section IV draws the conclusions.

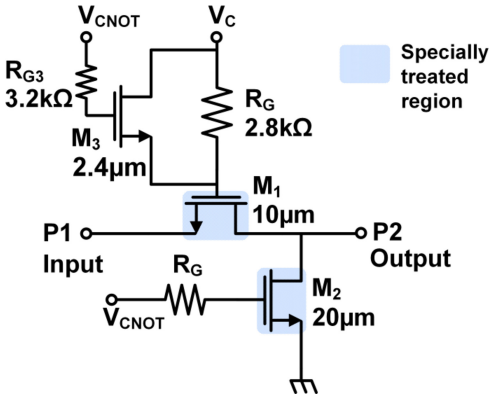

Fig. 1. Schematic of the SPST switch. M_1 and M_2 are n-MOSFETs with a specially treated region for lower losses and higher isolation. The DC control voltages V_C and V_{CNOT} allow switching the device in ON and OFF modes.

II. Low-Loss and High-Isolation Switch

Insertion loss (IL) and isolation (ISO) are key features of a SPST switch, as they are measures of the power difference between the input power and the output power when switch is in the ON and OFF state, respectively.

Fig. 1 shows the novel compact and wideband SPST switch based on a series-shunt topology with the aforementioned distinctive elements, which will be discussed in detail hereinafter. In a first instance, it is worth noticing that it consists solely

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of three n-MOSFETs and does not require spiral inductors/transformers and transmission lines, which would have required connecting the transistors to the top metal layers all through the back-end-of-line (BEOL) and then introduced substantial losses. Such a solution leads to very compact design with reduced parasitics and good wideband performance, as these are not reduced by lossy interconnects, whose effects are predominant at high frequencies.

The design was carried out in order to achieve a low insertion loss, while maintaining an isolation of 25 dB at 60 GHz, i.e., the central frequency of the mm-wave frequency band of interest. N-MOSFET devices with a nominal gate length of 20 nm were used for the implementation.

The switch is controlled by means of two DC control voltages, V_C and V_{CNOT}. When the switch is in the ON mode ($V_C = 0.8$ V, $V_{CNOT} = 0$ V).

To derive an expression of the insertion loss, let us assume that the n-MOSFET working in active and cutoff regions can be conveniently reduced to R_{on} and C_{off}, respectively. In the ON mode, the ABCD matrix of the small-signal equivalent circuit between Port 1 (i.e., P1) and Port 2 (i.e., P2) is given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & R_{on} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ j\omega C_{off} & 1 \end{bmatrix} = \begin{bmatrix} 1 + R_{on} j\omega C_{off} & R_{on} \\ j\omega C_{off} & 1 \end{bmatrix} \quad (1)$$

The insertion loss of the switch can be expressed as:

$$IL = -20\log|S_{21}| = -20\log\left|\frac{2}{A + B/Z_0 + CZ_0 + D}\right| \quad (2)$$

Then, the insertion loss is given by:

$$IL = 10\log\left\{\left(1 + \frac{R_{on}}{2Z_0}\right)^2 + \left[\pi f C_{off}(R_{on} + Z_0)\right]^2\right\} \quad (3)$$

where R_{on} is the channel resistance of the series transistor M_1 (active) and C_{off} is the capacitance of the parallel transistor M_2 (cutoff). From (3), the insertion loss at lower frequencies is mostly sensitive to the R_{on} [7], whereas C_{off} affects the insertion loss roll-off at higher frequency. For completeness, the channel resistance R_{on} of the n-MOSFET can be expressed as:

$$R_{on} = \frac{1}{\mu C_{ox} W/L(V_{GS} - V_T)} \quad (4)$$

where μ is the carrier mobility in the channel; W and L are channel width and length respectively; and V_{GS} and V_T are gate source bias and threshold voltage, respectively.

In 22nm FDSOI CMOS, super-low-V_T (SLVT) n-MOSFETs are preferred to regular V_T (RVT) n-MOSFETs to operate with a low threshold voltage (V_T), which has impact on lowering R_{on} and then the insertion loss. The threshold voltage can be further lowered by increasing the back-gate potential. However, for a wideband switch, the roll-off of the insertion loss over frequencies, which is affected by C_{off}, has to be minimized to reduce the insertion loss at high frequency. Both intrinsic capacitances of the transistor and extrinsic capacitances of the interconnects contribute to the total C_{off}.

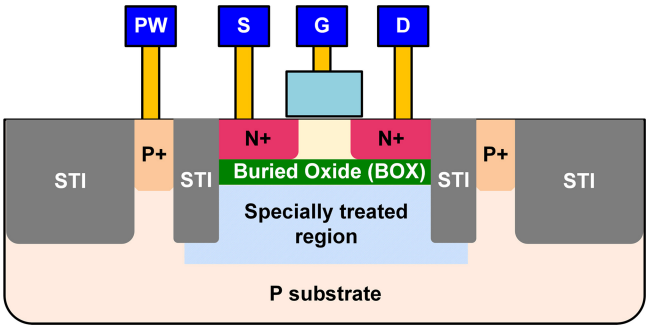

Fig. 2. Cross-section of the n-MOSFET with specially treated region.

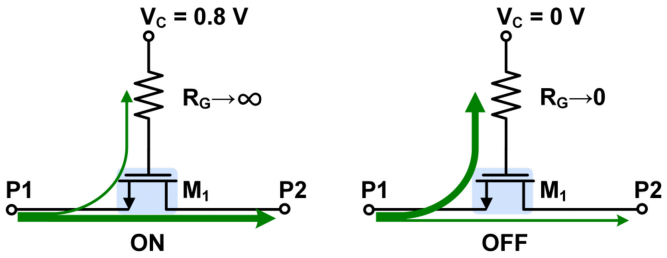

Fig. 3. Series n-MOSFET in the ON and OFF modes. The arrows illustrate the main (thick line) and residual (thin line) flow of the signal power.

The 22nm FDSOI CMOS technology by GlobalFoundries (22FDX) provides n-MOSFET device option with a specially treated region (BFMOAT) in order to reduce the parasitic effects in the substrate network [6]. Supported by the conclusion in [7], the BFMOAT n-MOSFET can be a valid option with respect to the common SLVT or RVT n-MOSFETs for mm-wave switches.

Fig. 2 shows the cross-sectional view of BFMOAT n-MOSFET in 22FDX technology. The thick specially-treated region is implemented below the BOX layer to further reduce the source/drain to substrate capacitances.

To further improve the isolation, the effect of the gate resistance R_G should be considered. From Fig. 3, when the switch is ON, the large gate resistance, R_G, is desired to direct most of the signal power toward the load for low insertion loss. On the other hand, a small gate resistance is desirable to bypass the signal toward ground when the switch is OFF, so to improve the isolation [8]. In order to accomplish these two desirable requirements, in our switch we have introduced the n-MOSFET, M_3, in parallel with R_G of series n-MOSFET. This additional transistor M_3 is active when the switch is OFF. As a consequence of its introduction in the switch circuit, the small channel resistance of M_3 bypasses the signal to ground and so it improves the isolation. With the adoption of M_3 in parallel with the gate resistance R_G of M_1, the post-layout simulation (PLS) results show that the isolation of SPST switch improves by about 3 dB at 60 GHz, with respect to the case without M_3, as reported in Fig. 4.

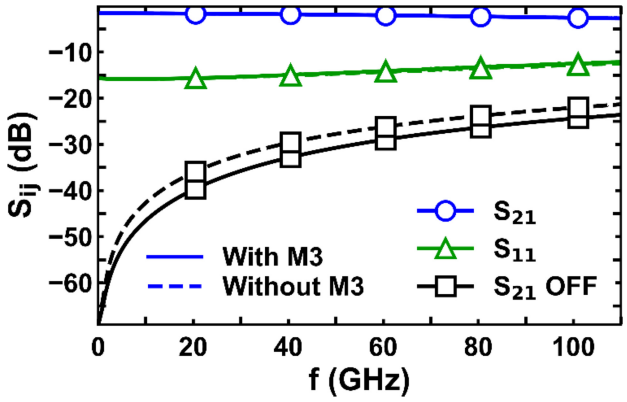

Fig. 4. S-parameters from simulation results of the SPST switch with and without M_3.

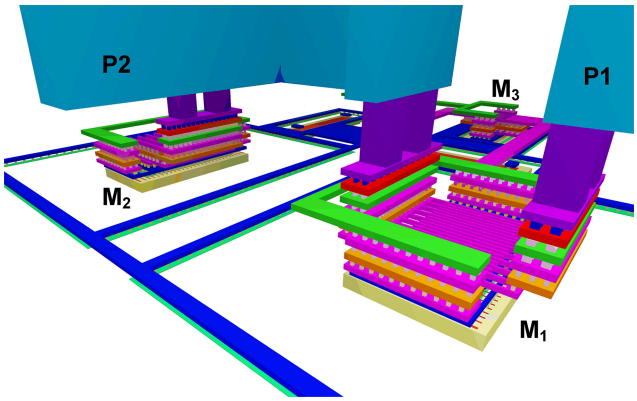

Fig. 5. Illustration of the layout in 3-D view.

III. Implementation and Measurements

A. Implementation

In order to achieve the desired performance, the gate width of the BFMOAT n-MOSFETs M_1 and M_2 have been sized to 10 μm and 20 µm, respectively. This sizing allows reaching a satisfactory tradeoff between low channel resistance and low C_{off} with the nominal control voltages, as captured by the equations (2) and (3). The bias resistors at the gate terminals are sized to 2.8 kΩ in order to secure an adequate AC series block impedance for the signal at the gate of the M_1 and M_2, and also have a compact size for reduced parasitic capacitances (i.e., higher overall impedance offered at the gate of the connected MOSFET) and a very compact layout. The width of SLVT n-MOSFET M_3 is 2.4 µm in order to provide a shunting path to ground for the unwanted residual signal at gate of M_1 while it is operating in the cutoff region.

The three-dimensional (3-D) view of the switch layout is illustrated in Fig. 5. The chip microphotograph is reported in Fig. 6.

B. Measurements

The switch has been measured on die with the Keysight Microwave Network Analyzer PNA-X N5245A and characterized over three frequency bands: DC-to-50 GHz, V (50-75 GHz) and W (75-110 GHz) bands. Power calibrations

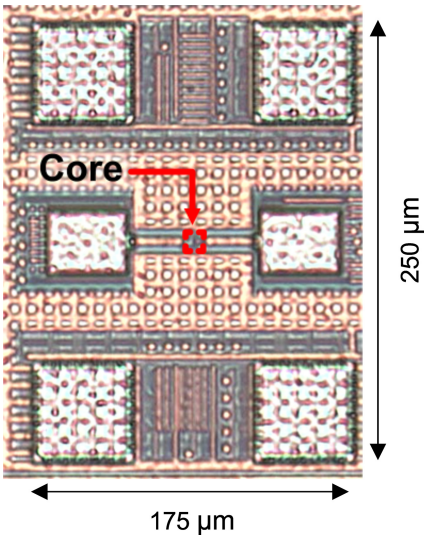

Fig. 6. Chip microphotograph of SPST switch with GSG pads (G: 50 × 50 µm^2; S: 45 × 35 µm^2). The core area (dashed box) amounts to 12.6 × 13 µm^2. The center-to-center pad spacing for signal pads with facing probes amounts to 120 µm. The control voltages generated externally are provided on chip through the DC pads and then distributed through a dense grid of metal layers. Bypass capacitors are placed in the area between and in proximity with the DC pads.

were carried out with the power meter N1914A, 50MHz-50GHz power sensor N8487A, the V-band V8486A and W- band W8486A power sensors by Keysight Technologies. Fig. 7 shows the measurement setups for all frequency bands.

The measurement setup below 50 GHz includes two FormFactor™ Infinity probes GSG i40 with 100 µm pitch, two 2.92mm coaxial cables and two 2.92-to-2.4 adapters to probe the input and output pads of the switch to the PNA-X. respectively.

The switch was probed by Formfactor GSG Infinity i110 probes (with 100µm pitch) and connected to the extender modules through 1-mm coaxial cables and WR-to-coaxial adapters. The measurement setup above 50 GHz includes a two-port Keysight Millimeter-Wave Controller (N5261A), two frequency extension modules (OMLINC) for each band.

The V15VNA2 T/R and W10VNA2 T/R extension modules were used to measure the S-parameters in V and W bands, The calibration was carried out up to the tips of probes with short-open-load-thru (SOLT) method using impedance standard substrate (ISS). Stand-alone GSG RF pads with thru feedlines were fabricated and measured for de-embedding purposes [9], [17], and their effects de-embedded from the S-parameter measurements of the switch together with the GSG pads with feedlines. The measurement results are reported in Fig. 8.

In the ON mode, the switch exhibits S_{21} of 1.6 dB at 1 GHz, increases gradually and amounts to 2.65 dB at 60 GHz, and 3.1 dB at 110 GHz. The switch exhibits S_{11} lower than 12.1 dB, i.e., the value at 110 GHz, all over the DC-to-110 GHz frequency range.

In the OFF mode (V_C = 0 V, V_{CNOT} = 0.8 V), S_{21} amounts to –60 dB, −26.4 dB and –22.8 dB at 1 GHz, 60 GHz, and 110 GHz, respectively. The comparison between

TABLE I
PERFORMANCE AND COMPARISON WITH PRIOR-ART SWITCHES

Ref.	**This work**	[1]	[2]	[3]	[4]	[18]
Type	**SPST**	SPST	SPST	SPST	SPST	SPDT
Tech.	**CMOS** [b]	CMOS [c]	SiGe [d]	CMOS [b]	CMOS [b]	SiGe [e]
Freq (GHz)	**DC-110**	DC-220	DC-125	10-110	DC-220	DC-110
IL (dB)	**< 3.1**	≤ 1.5	< 3.6	< 1.8	< 3.1	≤ 3.0
ISO (dB)	**>22.8**	>16	>22	>23	> 37	>20 [f]
RL (dB)	**>12**	> 10	≥ 10	>10	> 12	> 10.9
P_{1dB} (dBm)	**10.8 @50GHz**	7@50GHz	23@2GHz	7@24GHz	-	17@60GHz
Area [a] (mm^2)	**0.00016**	0.16	0.021 [g]	0.018	0.026	0.098

[a] Core [b] 22nm FDSOI [c] 45nm FDSOI [d] 90nm BiCMOS [e] 130nm HBT [f] Extrapolated from graph. [g] Extrapolated from figure.

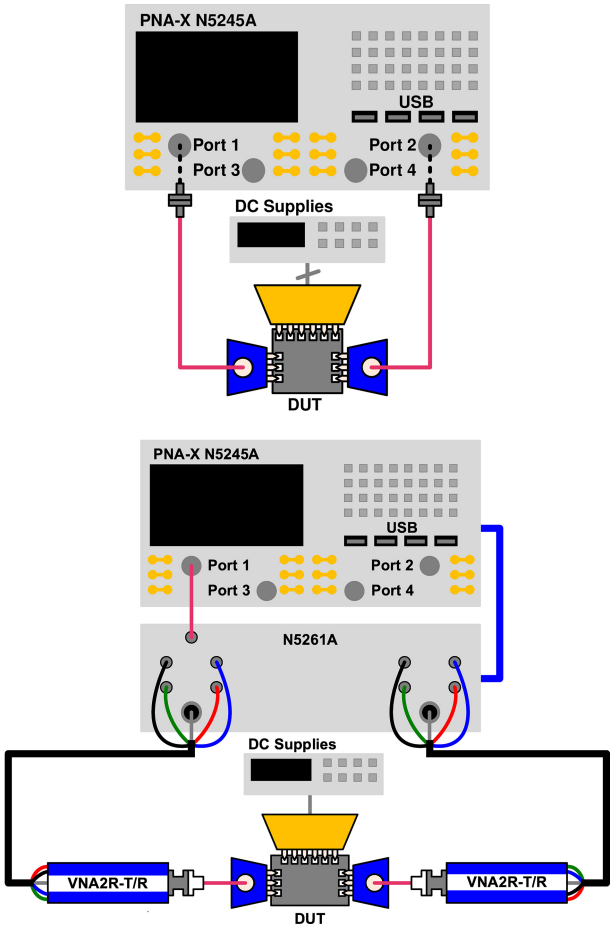

Fig. 7. On-chip measurement setup: DC-to-50 GHz (top); and V-band, W-band (bottom). These include multi-contact DC for bias voltages and GSG RF probes for input and output test signals.

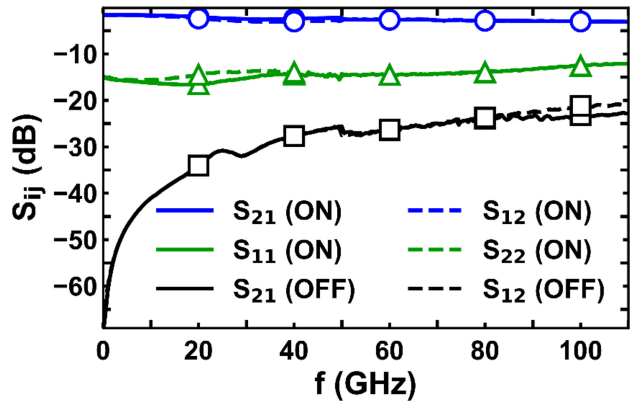

Fig. 8. Measured S-parameters of the SPST switch.

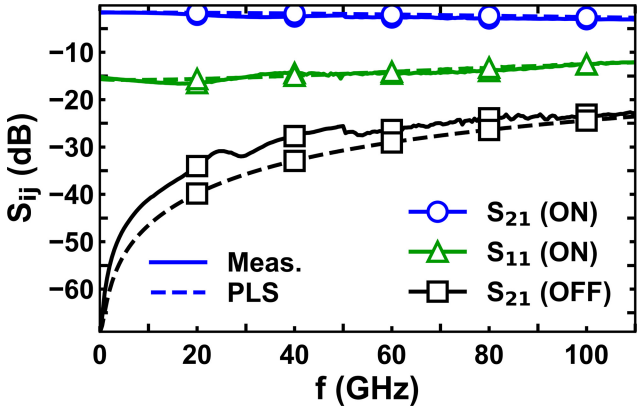

Fig. 9. Measured versus simulated relevant S-parameters of the switch.

the measured and simulated results of the relevant S-Parameters of the switch is reported in Fig. 9.

The measured input-referred 1dB compression point (iP_{1dB}) for input tones from 0.5 to 50 GHz is reported in Fig. 10. The comparison between the measured and simulated results is reported in Fig. 11. The iP_{1dB} amounts to about –1.8 dBm, 9.9 dBm and 10.8 dBm for input tones of 0.5 GHz, 35 GHz and 50 GHz, respectively. The higher iP_{1dB} at higher frequency can be explained to a large extent with the increase of the feedthrough component of the input signal, i.e., the signal component flowing through the overall parasitic capacitance across the source and drain terminals of the series transistor (M_1). As the impedance of such a parasitic capacitance reduces with frequency, the increase of the feedthrough signal component drained from the overall input signal at the source node leads to a higher iP_{1dB} at higher frequency.

Table I summarizes the performances of the SPST switch and reports the comparison with the prior art. The switch achieves a record area occupancy, while exhibits a low IL and high ISO and return loss (RL) comparable with the prior works.

IV. CONCLUSION

A novel and compact wideband (DC to 110 GHz) SPST switch has been designed and fabricated in 22nm FDSOI

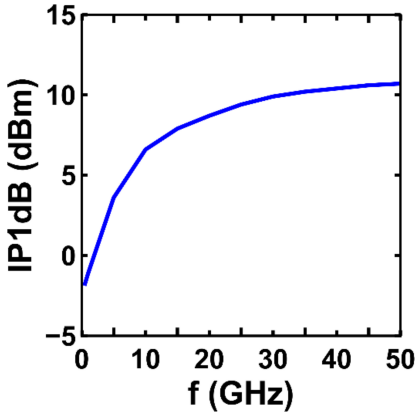

Fig. 10. Measured iP_{1dB} for input tones from 0.5 to 50 GHz.

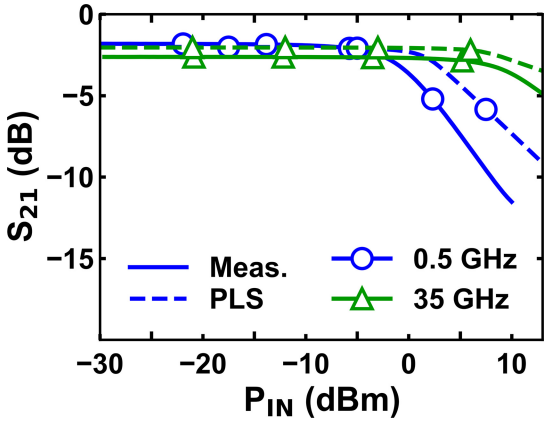

Fig. 11. Measured and simulated S_{21} for input tones of 0.5 and 35 GHz.

CMOS. The switch consists solely of three n-MOSFETs and does not require any large passive components prone to large parasitic effects, such as resistive losses and capacitive couplings, and that require large area on silicon.

Two n-MOSFETs are fabricated on a specially treated region, which allows reducing the substrate parasitic effects. As effect of the reduced parasitics, the switch has a low roll-off of the insertion loss over a wide range of frequencies. The isolation of the switch has been further improved by introducing an additional n-MOSFET in parallel with the gate resistance of the n-MOSFET in series with the signal path.

Unlike other switch circuits of the prior art, it does not make use of any dynamic biasing technique, and this facilitates its control and allows the reduction of complexity of the control circuitry within the host system. The switch occupies a very small area, i.e., up to about two or more orders of magnitude smaller than prior wideband mm-wave switches, which is crucial in all applications requiring a large number of array elements.

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