0.52-mW 30-GHz LNA in 22-nm FDSOI CMOS

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***Abstract*—This brief reports a novel low-power 30GHz LNA in 22nm FDSOI CMOS technology. The LNA is based on an active network with CMOS inverting amplifier stages, and input and output feedforward impedance matching networks. It exhibits a peak gain of 11.4 dB, a noise figure of 5.8 dB, with a record power consumption of 0.52 mW from a 0.8 V supply. Owing to its circuit topology, the LNA is compact in size and its core area amounts to 0.20 × 0.22 mm^2.**

***Index Terms*—Low noise amplifier, low power, mm-wave, sub-mW.**

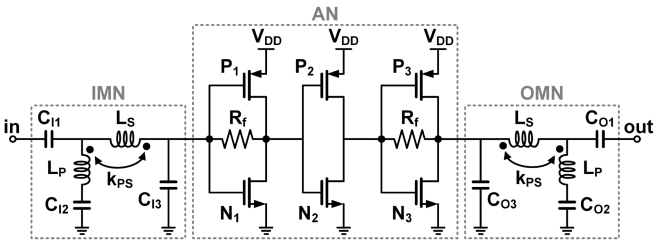

Fig. 1. Novel LNA topology. The dashed lines identify the input matching network (IMN), output matching network (OMN) and active network (AN).

I. Introduction

THE CONSTANT evolution of silicon microelectronic technologies has led to the development of innovative ultra-scaled transistors (active devices) capable of outstanding performances. MOSFETs in cutting-edge CMOS technologies have reached peak transition frequency (f_T) and maximum oscillation frequency (f_{max}) higher than 300 GHz [1], [2], [3]. For instance, thin oxide n-MOSFETs in 22nm FDSOI CMOS technology exhibit f_T/f_{max} as high as 347/371 GHz [2]. The high values of f_T and f_{max} are key enabling factors for emerging applications, such as 5G [3], [4], 6G [5], IoT [3], and quantum computing [6].

The traditional design paradigm for microwave and mm-wave integrated circuits relies on the cascade connection of active LC resonant stages [7], [8], [9], [10], [11], [12], [13], [14], made of transistors and large passive components, such as metal-insulator-metal capacitors, spiral inductors and transformers, and transmission lines (TLs). These are typically fabricated with the top thick metal layers of the back-end-of-line (BEOL) in order to limit the losses and capacitive effects towards the substrate. Despite the transistors have reached high f_{max} and low values of minimum noise figure (NF_{min}) [1], [2], [3], their full potential at the microwaves and mm-waves is severely impaired by the losses in passive components [15], [16], [17], especially for very low power consumption (P_C) where losses dominate [15], [16], [18]. In order to compensate the losses introduced by the passive components and their interconnections, including vias, from the transistor level all the way up the top thick metal layers of the passives, the current consumption of the transistors has to be increased to reach the desired performances. Compact broadband amplifier solutions with no LC resonant stages are attractive, also in terms area (e.g., [19]), but the inherent parasitic capacitances limit the desired maximum frequency of operation, which is typically mitigated by increasing the power consumption. Overall, low-power amplifier solutions with small footprint on silicon die are very attractive for microwave/mm-wave radios and radars based on phase-array transceivers with a large number of array elements [20], but also for qubit control circuits in monolithic quantum processors scalable to large number of qubits [21].

In this brief, we report the design of the 30GHz low-power low noise amplifier (LNA) based on an active network (AN) circuit topology in Fig. 1. This approach with no passive components in the active network breaks the well-established design paradigm above, providing reasonable performances with lower power consumption. In [20] we have addressed its application as variable-gain low noise amplifier for low-power tapered mm-wave 5G/6G phased-array receivers. In [21] we have addressed the design implementation tailored for 60 GHz operations at cryogenic temperatures (2K) as a key circuit, i.e., a "qubit size" amplifier for qubit control in monolithic quantum processors. In this brief we present all the features of the low-power amplifier topology of Fig. 1 together with its more inherent as well as more comprehensive design aspects for 30GHz operations and its experimental characterization at room temperature, for more general purposes in microwave and mm-wave communication and sensing applications [22], [23], such as radars [24], [25], radiometers [26] and 5G/6G mobile broadband phased-array transceivers [27].

This brief is organized as follows. Section II addresses the circuit design and implementation, and the post-layout simulation (PLS) results. Section III reports the

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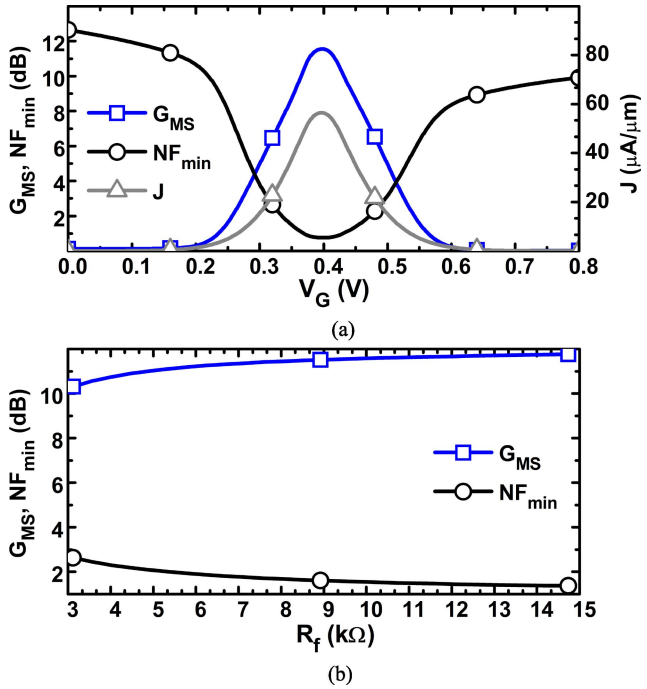

Fig. 2. (a) Performances of the INV versus V_G: Current density (J); G_{MS} and NF_{min} at 30 GHz. (b) G_{MS} and NF_{min} of SBI at 30 GHz.

experimental results. Finally, in Section IV, the conclusions are drawn.

II. LNA Design

A. Active Network

The AN takes advantage of the complementary current reuse [28] and consists of a self-biased CMOS inverting (SBI) amplifier as a fist stage, followed by a Cherry-Hooper amplifier stage, which is made of a CMOS inverting (INV) amplifier and an SBI. Typically, low-power LNA designs exploit forward body-bias (FBB) to lower, in magnitude, the threshold voltage (V_t) of MOSFETs and, in turn, allow a reduction of the supply voltage (V_{DD}) [11], [12]. However, FBB requires further control voltages and reducing V_{DD} has detrimental impact on linearity [12]. The LNA reported here is designed to operate at the nominal V_{DD} of 0.8 V and zero back-gate voltages.

The process design kit (PDK) offers several transistor flavors [3], with different V_t and allowed ranges for the back-gate voltages. To achieve the targeted power consumption (P_C) of 0.5 mW from the nominal V_{DD}, we have selected regular-V_t (rvt) transistors. All transistors are sized equally with gate width (W) of 3.9 μm. The even transistor sizing for all stages results from a trade-off between linearity and noise performances, and facilitates the layout implementation.

Fig. 2(a) reports the current density (J), i.e., the ratio of the source current of the p-MOSFET and W, the maximum stable gain (G_{MS}), and NF_{min} of the INV as a function of the DC gate voltage (V_G).

At V_G = 396 mV ≈ V_{DD}/2, the DC drain voltage V_D amounts to 397 mV ≈ V_G and the INV exhibits the peak current density of 56 μA/μm, peak G_{MS} of 11.5 dB, and optimum NF_{min} of 0.76 dB.

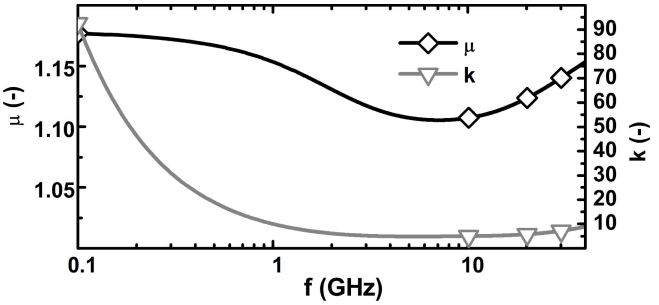

Fig. 3. Stability factors k and μ of the AN: The AN is unconditionally stable.

Moreover, the transconductances of the n-MOSFET and p-MOSFET amount to 3.2 mS and 2.9 mS, respectively. The results prove that the n-MOSFET and p-MOSFET, equally sized, are well balanced, as strain technologies have mitigated the gap between electron and hole mobilities in n-MOSFETs and p-MOSFETs, respectively.

Fig. 2(b) reports the G_{MS} and NF_{min} of the SBI as a function of the feedback resistor R_f. As R_f is increased from 3 to 10 kΩ, NF_{min} reduces from 2.6 dB to 1.5 dB and G_{MS} increases from 10.3 to 11.6 dB. Larger resistors do not improve significantly the performance of the SBI, but lead to a less compact layout. Thereby, we have selected an R_f of 10 kΩ as a good tradeoff. Both V_G and V_D of the SBI are equal to 396 mV and the current density J amounts to 56 μA/μm, as for the INV.

The AN is self-biased: The two SBIs and the INV have $V_G = V_D = 396$ mV and are biased at the peak current density of 56 μA/μm. The AN draws 0.52 mW from the 0.8V supply. Fig. 3 shows that the stability factors k and μ of the AN are greater than unity and therefore the AN is unconditionally stable.

At 30 GHz, the AN exhibits a minimum NF (NF_{min}^{AN}) of 1.86 dB and maximum available gain (G_{MA}^{AN}) of 23.2 dB. The input impedance (Z_{in}^{AN}) of the AN amounts to 292-j451 Ω and its complex conjugate $(Z_{in}^{AN})^*$ is matched to the optimum-noise impedance (Z_{ON}^{AN}) of AN. As a result, the coefficient $|\Gamma_N^{AN}| = |Z_{ON}^{AN} - (Z_{in}^{AN})^*|/|Z_{ON}^{AN} + Z_{in}^{AN}|$ [15], which provides a measure of the proximity between the two impedances, amounts to −12.1 dB.

As mentioned above, to fulfill gain and noise requirements, traditional mm-wave LNA design rely on cascading multiple active LC resonant stages [7], [8], [9], [10], [11], [12], [13], [14]. However, these results show that the outstanding performances of ultra-scaled active devices allow the AN to reach adequate performances at 30 GHz, so avoiding the losses (including those of the interconnections and vias through the BEOL) and power and area penalties caused by bulky spiral inductors, transformers, and TLs.

B. Matching Networks

On the basis of the AN performances, the LNA holds the potential to achieve $|S_{21}|^2 = G_{MA}^{AN}$ = 23.2 dB and NF ≈ NF_{min}^{AN} = 1.86 dB at 30 GHz. However, the full potential

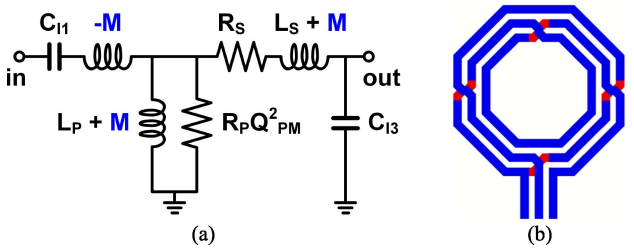

Fig. 4. (a) Equivalent circuit of IMN ($Q_{PM} >> 1$). (b) Layout of the transformer.

of the AN can only be achieved with ideal lossless reciprocal MNs [16].

Because of the IMN losses, the equivalent noise temperature T_N of the LNA has the following lower bound [16]:

$$\theta_1^{LNA} = T_0\left(1/G_A^{IMN} - 1\right) + T_{Nmin}^{AN}/G_A^{IMN}, \quad (1)$$

where $T_0 = 290$ K, T_{Nmin}^{AN} is the minimum equivalent noise temperature of AN, and G_A^{IMN} is the available gain of IMN.

The IMN is designed to maximize the power transfer at the input port of the LNA. This requirement leads to MNs with a quite large impedance transformation ratio, which is common in low-power designs [12], as the power budget constrains the maximum gate width of the MOSFETs and therefore the input impedance of the active stages is typically much larger than 50 Ω. The J adopted in our LNA design is 2-5 times lower than the optimum-NF_{min} and peak-f_{max} current densities applied in conventional mm-wave LNA designs [9], [11], [13], so leading to larger W and reduced $\mathrm{Re}\{Z_{in}^{AN}\}$ and $\mathrm{Im}\{Z_{in}^{AN}\}$ for the given drain current. To optimize the performances of the LNA with lossy IMN, we have applied the loss-aware design methodology in [15], [16], [18], i.e., input integrated matching for maximum power transfer and minimum cascade noise.

Fig. 4(a) reports the equivalent circuit of the IMN, where R_P and R_S denote the parasitic series resistances of the primary and secondary spirals of the transformer, with self-inductance L_P and L_S, respectively, and intrinsic Q-factors Q_P and Q_S, respectively, M denotes the mutual inductance, and $Q_{PM} = \omega(L_P + M)/R_P >> 1$ denotes the equivalent quality factor of the primary spiral. G_A^{IMN} is bounded by the maximum available gain of the IMN, which is, for a reciprocal network, solely determined by the stability factor [16], here denoted as k_{IMN}. $Q_{SM} = \omega(L_S + M)/R_S$ is the equivalent Q-factor of the secondary spiral and $n_M = (L_S + M)/(L_P + M)$ is the equivalent turn ratio. Neglecting the losses in the capacitors, we get

$$k_{IMN} \approx 1 + n_M/(Q_{SM}Q_{PM}). \quad (2)$$

As M increases, n_M decreases while Q_{SM} and Q_{PM} increase, which, in turn, improves k_{IMN}. Thereby, the coupling coefficient k_{PS} of the transformer can be used as a free parameter to minimize G_A^{IMN} and, in turn, minimize the noise temperature T_N^{IMN+AN} of the cascade of the IMN and AN, i.e., the cascade noise [16]. The results of the input integrated matching for maximum power transfer and minimum cascade noise applied to the schematic design of the IMN are reported in Figs. 5(a) and (b). Fig. 5(a) reports the T_N^{IMN+AN} and θ_1^{LNA}; Fig. 5(b) reports the S_{11} of the network formed by the IMN and AN

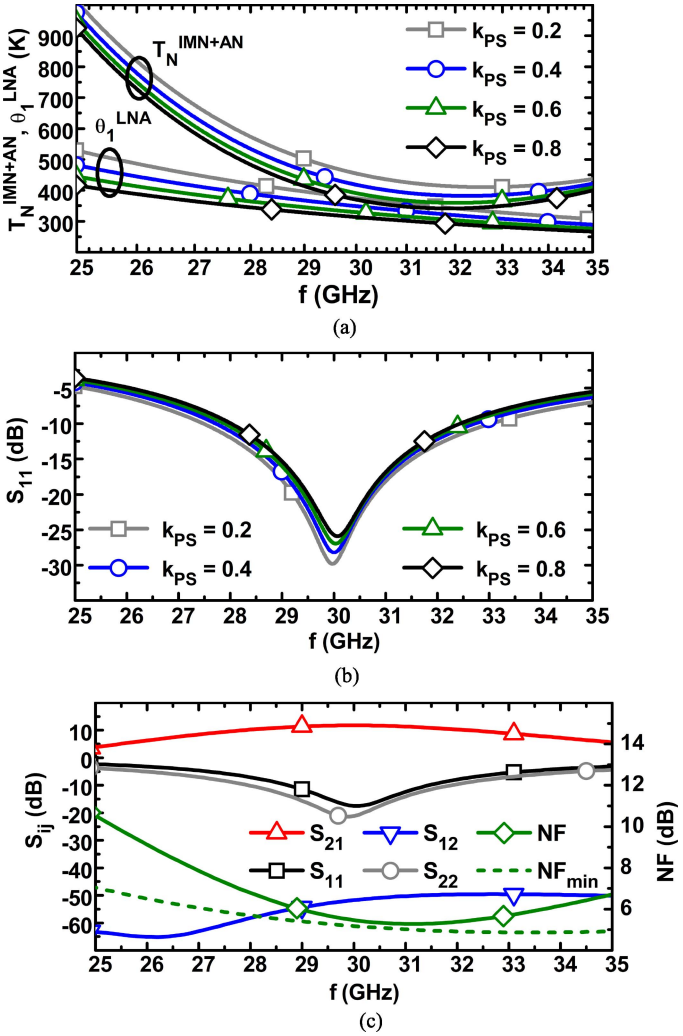

Fig. 5. Design of the IMN ($Q_P = Q_S = 10$, $L_S/L_P = 2$, $C_{I1} = 100$ fF, $C_{I3} = 26$ fF): (a) Equivalent noise temperature (T_N^{IMN+AN}) of the cascade of the IMN and AN, i.e., IMN + AN, theoretical lower bound θ_1^{LNA}, and (b) S_{11} of IMN + AN for different values of the coupling coefficient k_{PS}. (c) PLS results: S-parameters, NF, and NF_{min} of LNA.

for different values of k_{PS}. At 30 GHz, T_N^{IMN+AN} decreases from 454 K to 370 K as k_{PS} increases from 0.2 to 0.8. For all cases, T_N^{IMN+AN} approaches the lower bound θ_1^{LNA}, which decreases monotonically with k_{PS}.

The OMN employs the same transformer as IMN and the capacitors in OMN are fine-tuned to achieve maximum power transfer at the output port.

Last, a further consideration it is worth mentioning that, despite this design is focused on the proof of concept of the approach reported above, using the coupling factor to accomplish primarily the noise performance. Alternatively, the coupling factor could be used as a design parameter to adjust other circuit performance, such as the bandwidth extension of the input impedance matching. However, this may depend also on the entity of the desired bandwidth performance. Likely accomplishing specific bandwidth extensions could require more sophisticated matching networks with some further circuit element to be used as an additional design parameter.

TABLE I
CIRCUIT SIZING

C_{I1} (fF)	C_{I2} (fF)	C_{I3} (fF)	C_{O1} (fF)	C_{O2} (fF)	C_{O3} (fF)
238	548	26	26	730	550
L_P [pH]	Q_P [-]	L_S [pH]	Q_S [-]	k_{PS} [-]	
119	9.6	267	13.1	0.59	

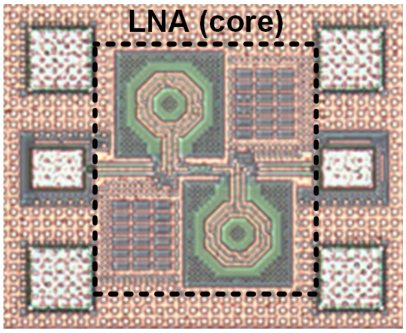

Fig. 6. Die micrograph.

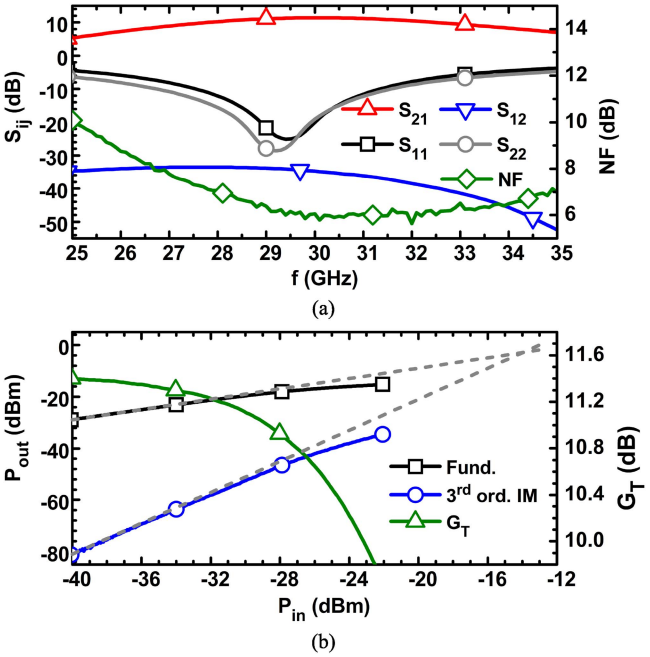

Fig. 7. Measurement results: (a) S-parameters and NF; (b) G_T at 30 GHz as a function of the P_{in}; IP_3 for two tones at 30.0 and 30.1 GHz.

However, these additional considerations go beyond the work reported in this brief.

C. Design Implementation

The technology offers several BEOL stack options [9], [13]. The selected option [9] includes nine copper metal layers (ML_1-ML_9) and one aluminum cap layer (ML_{10}). The layout of the custom-designed transformer is shown in Fig. 4(b); it is implemented in the two topmost thick copper metal layers (ML_8 and ML_9) [9]. The electromagnetic (EM) simulations have been performed in Momentum by Keysight Technologies. The circuit sizing is reported in Table I. Fig. 5(c) reports the results of the PLS. The LNA exhibits S_{21} of 11.8 dB and NF of 5.5 dB at the center frequency (f_0) of 30 GHz with a power consumption of 0.52 mW. The LNA exhibits an input-referred 1dB compression point (iP_{1dB}) of -24.1 dBm at f_0 and an input- referred 3^{rd} order intercept point (iIP_3) of -15 dBm for two tones at 30.0 and 30.1 GHz. Fig. 6 shows the die micrograph. The core area amounts to 0.20×0.22 mm^2.

III. EXPERIMENTAL RESULTS

On-die measurements have been carried out with the Keysight PNA-X N5245A and FormFactor Infinity Probes GSG i40. Power calibrations were carried out with the power meter N1914A and power sensor N8487A by Keysight. The measurement results are reported in Fig. 7. Fig. 7(a) plots the S-Parameters and NF. The LNA exhibits f_0 of 30.1 GHz, S_{21} of 11.4 dB and NF of 5.8 dB. Fig. 7(b) reports the transducer gain (G_T) of the LNA as a function of the input power (P_{in}) at 30 GHz. The LNA exhibits iP_{1dB} of -24.9 dBm. Also, Fig. 6(b) reports the results of the two-tone test with a frequency spacing of 100 MHz; the iIP_3 amounts to -14 dBm.

Overall, the measurements show a very good agreement with the PLS results, so demonstrating the effectiveness of the LNA design approach and methodology presented above. In such a design approach, unlike the common microwave/mm-wave design approaches, the amplifier stages of the ANs do not include any spiral inductors/transformers for peaking and inter-stage matching networks that require connecting the transistors to the top metal layers all through the BEOL and then introduce substantial losses. This design paradigm shift leads to very compact layouts with reduced parasitics and allows taking better advantage of the inherent performance of ultra-scaled MOSFETs, as these are not heavily impaired by lossy interconnects whose effects are predominant in low-power designs at high frequencies. However, the effectiveness of this approach reduces as the operating frequency increases, due to the inherent parasitic capacitances of the MOSFETs. Altogether, the results reported here demonstrate the very high potential as LNA element for microwave/mm-wave 5G/6G radios and radars based on phase-array transceivers with a large number array elements [20]. However, in [21] we have shown that with the same technology process, i.e., 22nm FDSOI CMOS, it can be still a viable design approach also for operations at 60 GHz, and possibly even beyond owing to the increase of gain, and reduction of thermal noise and losses at cryogenic temperatures.

Table II summarizes the LNA performances and reports the comparison with the prior-art low-power LNAs in the relevant microwave/mm-wave frequency range. The LNA achieves a record P_C, about 45% to 95% lower than prior-art low-power microwave/mm-wave LNAs. Among the sub-mW LNAs, it exhibits the best iP_{1dB}, -3dB bandwidth (BW_3) and -10dB bandwidth (BW_{10}), and it has the most compact core area.

IV. CONCLUSION

This brief reports a very low-power microwave/mm-wave LNA in 22nm FDSOI CMOS. The LNA consists of a novel circuit topology with a compact broadband active network and input and output impedance matching networks. The

TABLE II
SUMMARY OF PERFORMANCE AND COMPARISON WITH PRIOR-ART WORKS

Work	This	[10]	[9]	[11]	[12]
Tech.	**22 nm FDSOI**	22 nm FDSOI	22 nm FDSOI	22 nm FDSOI	90 nm Bulk
f_0 (GHz)	**30.1**	25[a]	22	22[a]	39.2
BW_3 (GHz)	**26.7-33.9**	19-34	20-36	19.5-29	38-41.1[a]
BW_{10} (GHz)	**27.6-31.3**	26-34[a]	22.5-32.2	22-32[a]	36.5-39.5[a]
S_{21} (dB)	**11.4**	12	17.9	16.9	11.7
NF (dB)	**5.8[b]**	1.46[b]	2.1-2.9	2.2[c]	5.4[b]
iP_{1dB} (dBm)	**-24.9**	-7.6	-	-10.2[d]	-29.7
iIP3 (dBm)	**-15[f]**	3[f]	-13.1[f]	+2.6[g]	-
P_C (mW)	**0.52**	9.8	5.6	3.2	0.92
Core area (mm^2)	**0.044**	0.12	0.05	0.19	0.19[e]

[a]Deduced from plot. [b]Minimum in -3dB band. [c]Mean value in -3dB band. [d]At 28 GHz for high-power mode (P_C = 9.6 mW). [e]Including pads. [f]100MHz tone spacing. [g]Tone spacing not reported.

LNA has been designed and implemented for operations at 30 GHz, and shows good performance with a record power consumption of 0.52 mW and area on silicon, and among the sub-mW LNAs exhibits comparable noise and gain performances, lowest power consumption, best iP_{1dB} and largest bandwidth.

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