A 79.2-μW 19.5-kHz-BW 94.8-dB-SNDR Fully Dynamic DT ΔΣ ADC Using CLS-Assisted FIA With Sampling Noise Cancellation

Akira Matsuoka, *Member, IEEE*, Yo Kumano, Tomohiro Nezuka, *Member, IEEE*, Yoshikazu Furuta, *Member, IEEE*, and Tetsuya Iizuka, *Senior Member, IEEE*

***Abstract*—This brief proposes a fully dynamic discrete-time (DT) ΔΣ ADC using a correlated level shifting (CLS)-assisted floating inverter amplifier (FIA) with a sampling noise cancellation (SNC) technique. The CLS-assisted FIA improves amplifier gain with a single-stage configuration, which has lower input-referred noise than the cascaded one. In combination with the proposed SNC, the noise contribution of the 1st-stage integrator can be minimized. We also propose a novel passive integrator cascaded with a passive adder that avoids unwanted inter-stage loading without a speed penalty. The prototype of the proposed ADC fabricated in a 65 nm bulk CMOS process realizes a fully dynamic operation and achieves 94.8 dB SNDR with an OSR of 256 for 19.5 kHz bandwidth while consuming 79.2 μW from a 1.2V supply at a 10 MHz sampling frequency. The Schreier and Walden FoMs are respectively 178.7 dB and 45.2 fJ/conv.-step, which are the best among recent fully dynamic DT ΔΣ ADCs with similar bandwidth.**

***Index Terms*—Delta sigma, analog-to-digital converter, dynamic, floating inverter amplifier, correlated level shifting, sampling noise cancelling, passive integrator.**

I. Introduction

DISCRETE-TIME (DT) ΔΣ ADCs using dynamic amplifiers [1], [2], [3], [4] are suitable for the analog front end of various sensor devices thanks to their scalability in power consumption with the operating frequency, compared to the DT ΔΣ ADCs using conventional amplifiers. Recently, a floating inverter amplifier (FIA) [5] has been widely used as a power efficient dynamic amplifier [1], [2], [3], [4], [5], [6], [7]. The FIA offers a stable output common-mode voltage as well as robustness to the input common-mode fluctuation as it works in its isolated power domain powered by a floating reservoir capacitor. To achieve high resolution with a DT ΔΣ ADC, the noise contribution of each building block has to be carefully optimized. Suppose that the quantization noise is usually designed to be lower than other random noise within signal band, the input sampling noise and the input-referred noise of the 1st-stage integrator usually have dominant contribution as these noise are not mitigated by noise-shaping. When FIA is used as an amplifier in the integrator, the input-referred noise of the integrator for a single-stage FIA and a two-stage one are respectively given by $2kT\gamma/C_S$ and $(2kT\gamma/C_S) \times Gm_2Ro_1$ [3], [8]. Here, k, T, C_S, and γ are Boltzmann's constant, absolute temperature, input sampling capacitance and noise factor of a transistor, respectively. Gm_2 and Ro_1 are the transconductance of the 2nd-stage amplifier and the output resistance of the 1st-stage amplifier at the end of the amplification phase, respectively. Although the single-stage FIA has lower input-referred noise than the two-stage one by a factor of Gm_2Ro_1, the gain of the single-stage FIA is not high enough to suppress the subsequent stage noise and quantization noise to negligible level. There are two architectures to solve this trade-off. One is a single-stage cascode FIA [3], which improves the gain of the FIA without degrading its noise performance, but results in a reduced output voltage range. The other one is an amplifier using correlated level shifting (CLS) technique. A single-stage FIA with CLS (CLS-FIA) [2] can also improve the gain without noise penalty by two-phase operation. By employing these amplifier architectures, the noise contribution of the integrator can be efficiently suppressed, thus the input sampling noise becomes the most dominant source and limits the performance of DT ΔΣ ADCs.

It has been demonstrated that the input sampling noise improves by adopting the cancellation or attenuation techniques [9], [10], [11], [12], [13]. To the best of authors' knowledge, there is no sampling noise cancellation (SNC) technique for switched-capacitor integrators, as it was not so meaningful when the input-referred noise of the amplifier dominates the total noise performance. However, CLS-FIA shows excellent input-referred noise performance and therefore the sampling noise becomes dominant noise source in an integrator with CLS-FIA. In this brief, the SNC applied to the switched-capacitor integrator is proposed. The proposed technique efficiently combines the SNC with a single-stage CLS-FIA in a switched-capacitor integrator. By sharing the output capacitor for CLS operation also for the SNC purpose, the noise performance of the integrator can be improved with minimal circuit penalty. In addition, to lower the power consumption of the overall ΔΣ ADC while achieving higher-order modulation, a novel passive filter cascaded with a passive

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Akira Matsuoka and Yo Kumano are with the Department of Electrical Engineering and Information Systems, The University of Tokyo, Tokyo 113-0032, Japan (e-mail: matsuoka@silicon.t.u-tokyo.ac.jp; kumano@silicon.t.u-tokyo.ac.jp).

Tomohiro Nezuka and Yoshikazu Furuta are with the Sensor R&D Division, MIRISE Technology Corporation, Kariya 448-8661, Aichi, Japan (e-mail: tomohiro.nezuka.j5h@mirise-techs.com; yoshikazu.furuta.j8e@mirise-techs.com).

Tetsuya Iizuka is with the Systems Design Lab, School of Engineering, The University of Tokyo, Tokyo 113-0032, Japan (e-mail: iizuka@vdec.u-tokyo.ac.jp).

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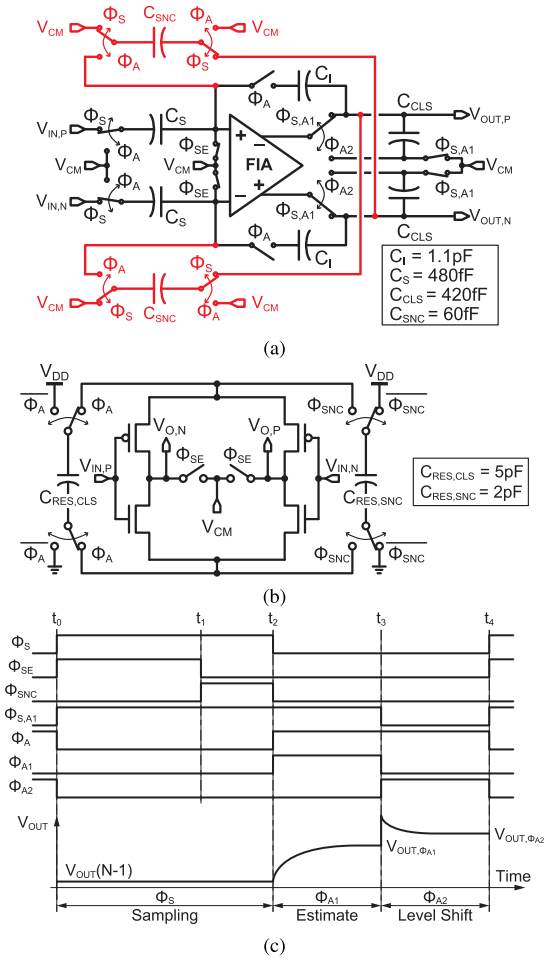


Fig. 1. (a) A schematic diagram of the integrator using the proposed CLS-assisted FIA with SNC, (b) a schematic diagram of the FIA and (c) the timing diagram of the proposed CLS-assisted FIA with SNC.

adder is also proposed. The proposed passive filter avoids the noise transfer function (NTF) degradation due to unwanted inter-stage charge sharing. These proposed techniques are demonstrated in a single-loop 3rd-order fully dynamic DT $\Delta\Sigma$ ADC.

II. Proposed CLS-Assisted FIA With SNC

Figure 1(a) illustrates the schematic diagram of the integrator using the proposed CLS-assisted FIA with SNC. A simple non-cascoded FIA [5] is employed for the amplifier, but two reservoir capacitors are integrated for consecutive SNC and CLS operations as shown in Fig. 1(b). By using two separate reservoir capacitors instead of a single large one, more stable gain during SNC as well as faster slew rate at the beginning of CLS are achieved. By applying CLS, the effective gain of the FIA is boosted by the two amplification phases, estimation (Φ_{A1}) and level shift (Φ_{A2}) as shown in the output waveform of the FIA V_{OUT} in Fig. 1(c) [2]. To implement SNC, two capacitors C_{SNC} and a few switches are added as indicated by the red lines in Fig. 1(a). For SNC operation, the input sampling capacitor C_S first samples the input signal together with the sampling noise at the falling edge of Φ_{SE} at t_1 in Fig. 1(c). Then, while Φ_{SNC} is high, the FIA is activated to amplify the input voltage change and sampling noise. When Φ_S becomes low at t_2, the FIA output is sampled by C_{SNC}. At this moment, V_{SNC}, the voltage across C_{SNC}, is given by

$$V_{SNC} = A_{OP} \cdot (V_{IN}(t_2) - V_{IN}(t_1) - v_{ns}) + v_{nsnc}, \quad (1)$$

where A_{OP}, V_{IN}, v_{ns} and v_{nsnc} are the open loop gain of the FIA, the input voltage, the sampling noise, and the noise sampled by C_{SNC}, respectively. Next, during the amplification phase (Φ_A), both the charge on C_S and C_{SNC} are transferred to the integration capacitor C_I. At the end of the amplification phase t_4, the output voltage V_{OUT} is given by

$$V_{OUT}(N) = V_{OUT}(N-1) + \frac{C_S}{C_I} \cdot (V_{IN}(t_1) + v_{ns}) + \frac{C_{SNC}}{C_I} \cdot V_{SNC}, \quad (2)$$

where N represents the number of cycles. By substituting (1), this equation is rewritten as follows:

$$V_{OUT}(N) = V_{OUT}(N-1) + \frac{C_{SNC}}{C_I} \cdot A_{OP} \cdot V_{IN}(t_2) + \frac{C_S}{C_I} \cdot \left(1 - \frac{C_{SNC}}{C_S} \cdot A_{OP}\right) \cdot (V_{IN}(t_1) + v_{ns}) + \frac{C_{SNC}}{C_I} \cdot v_{nsnc}. \quad (3)$$

When $(C_{SNC}/C_S) \cdot A_{OP} = 1$ is satisfied, (3) is simplified as

$$V_{OUT}(N) = V_{OUT}(N-1) + \frac{C_S}{C_I} \cdot V_{IN}(t_2) + \frac{C_S}{C_I} \cdot \frac{v_{nsnc}}{A_{OP}}. \quad (4)$$

As given by (4), the sampling noise v_{ns} is ideally cancelled and the additional noise v_{nsnc} is attenuated by A_{OP}. According to [5], A_{OP} can be approximated for the FIA as follows:

$$A_{OP} \approx \frac{2C_{RES} \cdot \Delta V_S}{n \cdot (C_{SNC} + C_{CLS}) \cdot kT/q}, \quad (5)$$

where n, q, C_{RES}, and ΔV_S are the weak-inversion slope factor, elementary charge, the reservoir capacitor, and the change of input transistor's source voltage in the FIA at the end of amplification, respectively. Using this approximation, the additional noise at the output is given by

$$\frac{\overline{v_{nsnc}^2}}{A_{OP}^2} \approx \frac{2kT \cdot n}{A_{OP}(C_{SNC} + C_{CLS})}. \quad (6)$$

As shown with this equation, by combining the proposed SNC with CLS, C_{CLS} is efficiently reused to suppress the additional noise. In this brief, $C_{SNC} = 60\,\text{fF}$, $A_{OP} = 8$, $C_{CLS} = 420\,\text{fF}$ and $C_S = 480\,\text{fF}$ are used. Substituting these values to (6), the proposed SNC reduces the sampling noise by 82%. Assuming $\gamma = 2/3$ [14], the total noise of the 1st integrator is suppressed by 44%, which is translated to 2.6 dB SNR improvement. When there is a gain error in A_{OP}, the sampling noise is not completely canceled and appears at the output. Based on process-corner simulations with a temperature range of 0 °C to 80 °C, A_{OP} fluctuates at most 30%. This gain error introduces less than 0.4 dB SNR drop. Therefore, we do not implement a gain tuning capability to avoid performance overhead as well as more design complexity.

III. Proposed Discrete-Time $\Delta\Sigma$ ADC

Figure 2 illustrates the schematic and timing diagrams of the proposed DT $\Delta\Sigma$ ADC. The ADC consists of a single-loop 3rd-order 1.5-bit $\Delta\Sigma$ modulator with an input feed-forward path. The 1.5-bit quantizer is chosen because the number of comparators is limited to only 2 thus the DWA is not required, while compared with the 1-bit case, the quantization noise of the 1.5-bit quantizer is smaller and the voltage swing can be limited, which relaxes the requirements for the FIA-based

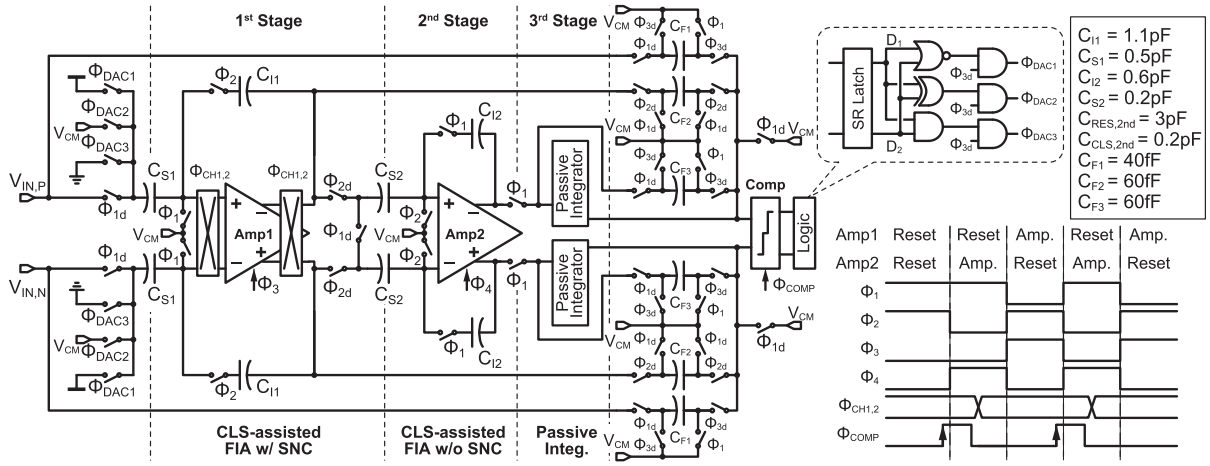
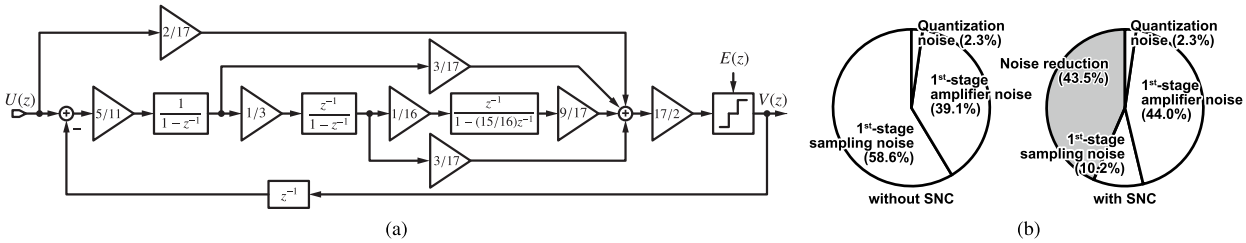


Fig. 2. Schematic and timing diagrams of the proposed single-loop 3rd-order fully dynamic DT ΔΣ ADC. Subscript 'd' for the switch control phase means that its falling edge is slightly delayed from the original one.



(a) (b)

Fig. 3. (a) Signal flow graph of the proposed single-loop 3rd-order ΔΣ ADC and (b) noise breakdowns without and with the SNC.

amplifiers. The 1st and 2nd integrators are each composed of the CLS-assisted FIA, with and without SNC, respectively. For the 3rd stage, the proposed passive integrator described in Section IV is used to minimize the power consumption without penalizing the FoM. To reduce the effect of $1/f$ noise on the ADC, chopping of the FIA is employed for the 1st stage. V_{CM} is set to $V_{DD}/2$. The 1.5-bit quantizer is composed of two StrongARM latch comparators [15]. The reset and amplification phases of the FIAs in the 1st and 2nd integrators are operated alternately with a half-cycle phase difference.

Figure 3(a) illustrates the signal flow graph of the ΔΣ modulator. The scaling factors are determined by behavioral simulation to ensure that the amplifier outputs are within an appropriate range, *e.g.*, from 200 mV to 1 V. The quantizer gain of 8.5 was adjusted with the reference voltages of the comparators, which are externally provided in the prototype in this brief. Figure 3(b) shows the noise breakdowns of the proposed ADC without and with the SNC. The contributions of other noise sources such as the 2nd-stage amplifiers are about 0.1% and thus ignored. Though the 1st-stage noise contribution is slightly increased by employing the SNC, about 44% of the total noise is reduced. The signal transfer function (STF) and noise transfer function (NTF) of the ΔΣ modulator normalized by the sampling frequency are shown with solid lines in Fig. 4. The STF is flat at low frequency, and the NTF exhibits nearly 3rd-order noise shaping characteristics (60 dB/dec).

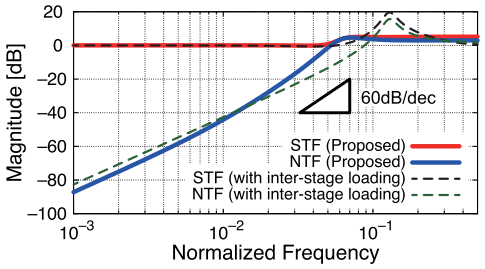


Fig. 4. STF and NTF versus the frequency normalized by the sampling frequency.

IV. Proposed Passive Integrator With Passive Adder

As shown in Fig. 2, the 3rd stage of the ΔΣ modulator consists of a passive integrator. In the conventional two-stage passive integrator, the signal is transferred from the 1st stage holding capacitor to the 2nd stage sampling capacitor by connecting them with a switch, without buffer amplifiers. Therefore, the charge in these capacitors can move in both directions, which is so called inter-stage loading effect [16]. If the passive integrator is applied to a ΔΣ modulator, it causes an unintentional feedback path, resulting in the degradation of the noise shaping characteristics and loop stability. In our work, this unwanted effect will happen between the 3rd-stage passive integrator and the subsequent passive adder. Supposing that this unwanted effect exists in our signal flow graph in Fig. 3(a), the STF and NTF are both changed to the ones shown with dashed lines in Fig. 4, which exhibit the degraded noise shaping characteristics as well as the peaking due to the reduced phase margin. Moreover, especially in our architecture that uses the passive adder cascaded with the passive integrator, this inter-stage loading will also affect to the scaling factors of the feed-forward paths in the actual implementation, which substantially changes the loop characteristics.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	A-SSCC 2016 [17]	JSSC 2020 [18]	CICC 2021 [4]	TCAS II 2022 [1]	JSSC 2022 [3]	ISSCC 2022 [2]	This work
Type	DT ΔΣ	DT ΔΣ	DT ΔΣ	DT ΔΣ	DT ΔΣ	DT ΔΣ	DT ΔΣ
Power/F_S Scalability	No	No	Yes	Yes	Yes	Yes	Yes
Technology [nm]	65	65	180	65	180	55	65
Supply [V]	1.0	0.8	1.5	1.0	1.8	1.2	1.2
Area [mm^2]	0.11	0.12	0.75	0.04	0.8	0.136	0.048
Noise Shaping Order	2	2	3	2	3	2	3
Bandwidth [kHz]	24	24	0.8	19.5	24	1	19.5
Oversampling Ratio	64	64	125	256	64	125	256
Sampling Frequency [MHz]	3.072	3.072	0.2	10	3.072	0.25	10
SNR [dB]	91.2	89.6	89.3	88.5	96.4	95.8	95.7
SNDR [dB]	91.2	89.6	89.3	88.5	96.2	94.0	94.8
Power [μW]	94	60	4	43.5	340	2.87	79.2
FoM_S [dB]	175.2	175.6	172.3	175.0	174.7	179.4	178.7
FoM_W [fJ/c.-s.]	66.2	50.6	104.8	51.2	130	35.0	45.2

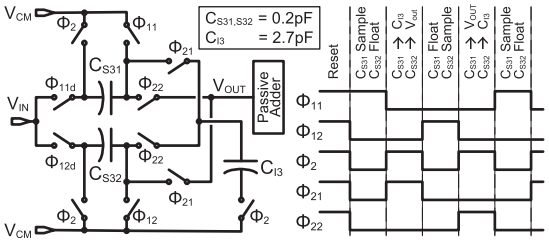
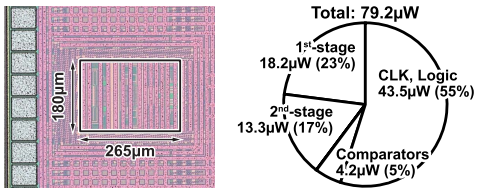


Fig. 5. Schematic diagram and timing diagram of the proposed passive integrator.



(a) (b)

Fig. 6. (a) Die micrograph and (b) measured power breakdown.

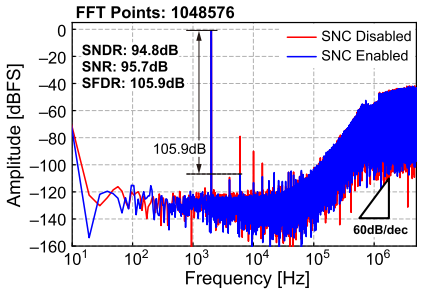


Fig. 7. Measured output spectra at 10 MHz sampling frequency.

To overcome the inter-stage loading effect, a charge-sharing rotation technique is proposed in [16], but it requires three phases: sampling, 1st-stage integration, and 2nd-stage integration. Figure 5 shows the proposed passive integrator, whose operation is outlined as follows. First, the sampling capacitor C_{S31} samples the input voltage. Next, C_{S31} is connected to the integration capacitor C_{I3}. In the next sampling phase, C_{S31} is floated while the replica sampling capacitor C_{S32} samples the next input voltage. Finally, the C_{S31} is connected to the output while C_{S32} is connected to the integration capacitor C_{I3}. In short, the proposed architecture uses two sampling capacitors in a ping-pong manner to realize integration in two phases. Even though some additional noise is introduced by this ping-pong structure, it will be mitigated by 2nd-order noise shaping through the loop.

V. MEASUREMENT RESULT

The prototype of the proposed DT ΔΣ ADC is fabricated in TSMC 65 nm bulk CMOS process. Figure 6(a) shows a die micrograph. The active area of the ADC is 180 μm × 265 μm. The measurement setup of the prototype uses a Stanford Research System DS360 and a Tektronix AFG31252 function generator as the differential input signal and clock sources, respectively. The 1.5-bit bitstream output is captured by a Digilent Digital Discovery logic analyzer and then processed with a PC. The ADC consumes 79.2 μW with SNC and 74.0 μW without SNC from a 1.2 V supply at 10 MHz sampling frequency. Figure 6(b) shows the power breakdown of the ADC with SNC, where the analog and the digital parts consume 35.7 μW (45%) and 43.5 μW (55%), respectively. Figure 7 shows the measured output spectrum of the ADC with −1.1 dBFS input at 2.01225 kHz with a blue line. The ADC achieves 94.8 dB SNDR and 95.7 dB SNR with the OSR of 256. SFDR is 105.9 dB. The Schreier and Walden FoMs are 178.7 dB and 45.2 fJ/conv.-step, respectively. As shown in Fig. 7 with the red line, SNR is 94.0 dB without SNC, which indicates that the proposed SNC improves SNR by 1.7dB.[1]

Figure 8 shows the measured SNDR/SNR versus the input amplitude. The ADC achieves 92.0 dB DR. The measured DR is limited by idle tones that become prominent when the input signal amplitude is below −55 dBFS. Based on system-level simulations, these idle tones are expected to be caused by

[1] Although some harmonic components arise in the red spectrum in Fig. 7 without SNC, this is mainly caused by the clock signal generation unoptimized for the case without SNC, thus it is not a fundamental difference between the cases with and without SNC.

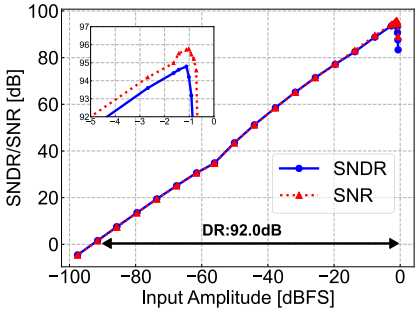


Fig. 8. Measured SNDR/SNR versus input amplitude.

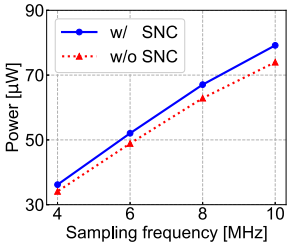


Fig. 9. Measured power consumption versus sampling frequency.

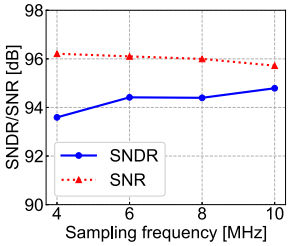


Fig. 10. Measured SNDR/SNR versus sampling frequency.

the offset due to the mismatch in the switches and capacitors, and can be suppressed by adding dither. Figures 9 and 10 show the power consumption and SNDR/SNR versus the sampling frequency, respectively. The proposed ADC shows power scalability to sampling frequency thanks to its fully dynamic operation. The reduced SNDR at low sampling frequency is mainly caused by the leakage after the C_{RES} in the FIA is almost fully discharged, which limits the amplifiers' output voltage swing and introduces some more distortion. Since the capacitance of the C_{RES} is optimized for 10 MHz operation in this prototype, the SNDR is slightly reduced at low-sample-rate operation. Table I shows the performance summary and the comparison with recent fully dynamic DT ΔΣ ADCs. The proposed ADC achieves the highest FoM_S and the lowest FoM_W among ADCs with bandwidth around 20 kHz.

VI. Conclusion

This brief proposes a fully dynamic 3rd-order DT ΔΣ ADC using a CLS-assisted FIA with SNC. A novel passive filter cascaded with a passive adder is also proposed to avoid the unwanted inter-stage loading effect while saving power for higher-order noise shaping. The measurement results of the prototype fabricated in a 65 nm CMOS process demonstrate that the SNR improves 1.7dB by enabling the proposed SNC in the CLS-assisted FIA. The proposed ADC exhibits the best FoM_S and FoM_W among recent fully dynamic DT ΔΣ ADCs with similar bandwidth.

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