A 460 800 Pixels CMOS Capacitive Sensor Array With Programmable Fusion Pixels and Noise Canceling for Life Science Applications

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Abstract—Capacitive sensor array (CSA) plays an important role in life science applications, such as cell monitoring, DNA detection, or drug screening. This brief presents a 480×960 time-sharing TDC (ts-TDC) architecture of global shutter CSA. It provides an opportunity to merge interfacing, read-out and sampling circuits in pixel and dynamically adjust the electrode size according to the characteristic of biosample. Each pixel size is within 2.25×2.25 μm^2. The sensitivity of the proposed CSA is 6.896 codes/fF, and 43 fps can be adopted for real-time monitoring. Experiment results show that noise canceling significantly improves the sensing performance. Moreover, sensitivity can be optimized by given fusion-pixel pattern, making our proposal very flexible and suitable for cell biology applications and personalized medicine.

Index Terms—CMOS lab-on-chip, capacitance sensor array, fusion pixels, high throughput, ts-TDC.
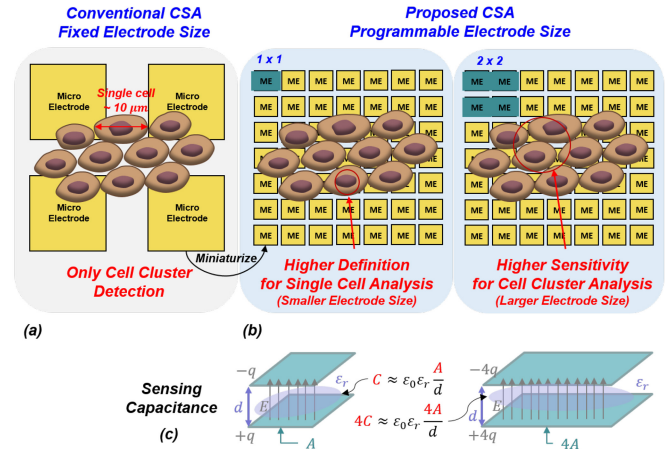
Fig. 1. Comparison. (a) conventional CSA with fixed electrode size. (b) proposed CSA with programmable electrode size (c) relationship between electrode size and corresponding induced sample capacitance.

I. INTRODUCTION

THE PAST decade has seen rapid development and innovation of CMOS Lab-on-Chip to perform unprecedented actuation and sensing for life science applications, such as, fast medical test with digital microfluidic (DMF) [1], cell sorting with traveling-wave dielectrophoresis (tw-DEP) [2], polymerase chain reaction (PCR) with heating micro-electrode array (H-MEA) [3]. They provide lower cost, faster operation, smaller regent volumes, and higher throughput than traditional approaches. Among these promising technologies, capacitive sensor array (CSA) plays a vital role in collecting electric-physical responses from the biotarget and offering a precise operation strategy [4]. A wide variety of non-destructive, label-free CSAs have been successfully demonstrated to perform cell growth monitoring [5], [6], [7], [8], DNA detection [9],

particle identification [10], drug screening [11] or super resolution cell imaging [12], [13]. Unlike optical sensors, CSA needs no more expensive equipment, such as a microscope, and can effectively prevent phototoxicity and photobleaching from cell observations, which is one of the reasons leading to unexpected cell behavior.

Miniaturized electrode size toward high throughput screening remains a challenge in CSA research [14]. Take cells application for instance, [6] demonstrated a 8×8 biosensor array with charge-based capacitance measurement (CBCM). It successfully monitored cell growth utilizing a 50×50 μm^2 interdigitated electrode. However, it is difficult to inspect single-cell behavior due to the mismatch size between individual electrode and single-cell, roughly 10 μm. Likewise, [7] converts capacitance to frequency by ring oscillator(RO) and shows real-time cell proliferation monitoring with 4×4 CSA, and 30×30 μm^2 electrode size. Although it is enough to identify cell cluster adhesion, there is still room for improvement in spatial resolution to observe single-cell behavior.

In this brief, we proposed a new sensing architecture for CSA with smaller and programmable electrode size as shown in Fig. 1. Compared to conventional sensing platforms with fixed electrode size, we enable the possibility to dynamically adjust electrode size on the basis of biospecies characteristics and the observation of both single cell behavior and cell cluster
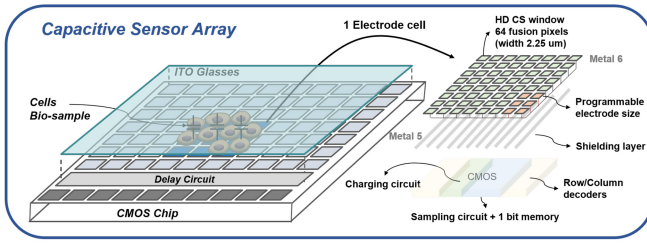
Fig. 2. Proposed CSA hierarchical architecture. Each EC consist of 64 pixels, shielding layer, row/column decoders, charging circuit, sampling circuit and 1-bit memory. The in-pixel sensing circuit is shared among all 64 pixels, improving spatial efficiency.

morphology. For single cell experiments, it is important to use electrodes that are similar in size to the cells being studied. The sizes of different cell types can vary, with iPSC [15], HeLA [16], MCF-7 [16], and Cardiomyocytes [17] having diameters of approximately 6.5 μm, 8.5 μm, 10.2 μm, and 20-35 μm, respectively. When studying cell clusters, a larger electrode size may be more effective in obtaining a stronger sensing result due to the larger area being covered. However, the choice of electrode size will depend on the specific experiment and the size of the cell cluster being studied. Therefore, the best sensing strategy is to predict the sample size and adopt a corresponding electrode size to balance spatial resolution and sensitivity.

In an effort to minimize electrode size, a hierarchical electrode design, shown in Fig. 2, has been employed in the development of a new CSA. This design features 64 pixels that share a single in-pixel sensing circuit, thereby improving spatial efficiency. To further enhance the CSA's performance, an innovative approach to capacitance sensing has been introduced. Instead of converting capacitance to voltage, its value is determined through conversion to time and use of a time-sharing time-to-digital converter (ts-TDC). This approach enables the CSA to operate in global shutter mode, freeing up more area under the electrode and holding the potential for future multi-modality integration. The programmable electrode shape in this design also allows for improved digital image processing through acquisition of multiple frames with the same or different patterns, leading to enhanced sensing performance.

The remainder of this brief is organized as follows. Section II presents the concept of fusion-pixel and ts-TDC based capacitance sensing approach. Section III introduces the details of CSA system implementation. Section IV shows the experiment results. Finally, the conclusion is drawn in Section V.

II. CAPACITANCE SENSING

Most of capacitive sensor arrays comprise three major components, interfacing circuit, read-out circuit and sampling circuit. Interfacing circuit first converts capacitance into different physical parameters, such as voltage, current, or frequency. Next, these small change would be read out and amplified once it is selected by controller. Finally, sampling circuit performs a quantization, so that digital code is derived to decide the exact value of capacitance. As the sampling circuit, like ADC, is often in a large area and complex system to reach
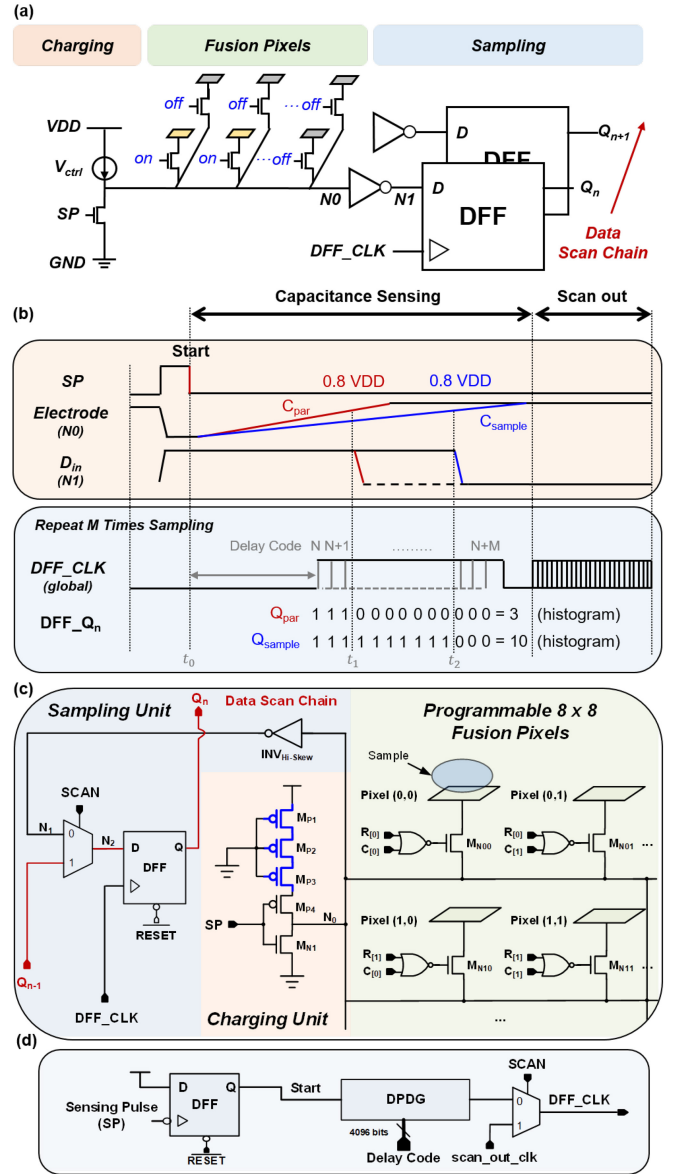

Fig. 3. ts-TDC based method (a) simplified circuit diagram (b) timing diagram (c) EC circuit design (d) global clock design.

higher precision, it is tough to be embedded into pixels and limits the sensing throughput. Moreover, since these signals need to pass through an analog switch and long metal line, it will probably increase the coupling noise and thermal variation. Therefore, we proposed a ts-TDC method for sampling that is capable of combining three major components into one electrode cell (EC).

A. ts-TDC Based Approach

The concept of using ts-TDC approach was inspired by location sensing in [1]. The basic components of ts-TDC are shown in Fig. 3. First, a charging circuit is employed to convert capacitance into time. When sensing pulse (SP) ties low, the current source starts to charge electrodes. The output of hi-skewed inverter is turned down until EC reaches $0.8VDD$. Then, the D-flip flop (DFF) performs sampling at delay-code N. Picture (b) shows without sample (C_{par}) and with sample

(C_{sample}) conditions, and both Q_{par} and Q_{sample} would be logic 1. These processes will be repeated again with a small delay in the DFF sampling time. For Q_{par} after t_1, it becomes logic 0 due to early achieving to 0.8VDD, whereas Q_{sample} remains logic 1. For Q_{sample} after t_2, it eventually drops to logic 0. Lastly, we sum all Q values to derive the exact time difference for these two objects. It can be inferred to its corresponding capacitance measurement result. This method is capable of embedding sampling circuit into pixel and uses only one simple delay generator to achieve the objective.

B. Fusion-Pixel Design

Based on the ts-TDC approach, the equation (1) provides a straightforward method to determine the sensitivity (S):

$$S = \frac{\Delta code}{\Delta C} = \frac{\Delta T_{charging}/\Delta C}{\Delta T_{step}/\Delta code} \tag{1}$$

This involves calculating the ratio of the timing window ($\Delta T_{charging}/\Delta C$) obtained from the charge pump under capacitance C to the timing resolution ($\Delta T_{step}/\Delta code$) of the delay generator. The timing window is related to the charging time constant $\tau_{charging}$. It could be expressed as a simplified model:

$$\tau_{charging} = R_{total}C_{total}, \tag{2}$$

where R, C is the total resistance and capacitance on the current path. Hence, as shown in Fig. 3(c), applying a 8×8 NMOS switches connected separately to the top metal can derive the C_{total} and R_{total}:

$$C_{total} = C_{parasitic} + \sum_{i,j=1}^{8}\sum On_{(i,j)}C_{sample(i,j)}, \tag{3}$$

where $On_{(i,j)}$ is determined by row/column signals, i.e., $R_{[i]}/C_{[j]}$ in picture (c). This allows the possibility to alter pixel numbers and shapes by changing patterns of $On_{(i,j)}$.

$$R_{total} \simeq R_P + R_{parasitic}, R_P \gg R_{parasitic}, \tag{4}$$

where R_P is the equivalent resistance of PMOS. The larger R_{total} is applied, the smaller C_{sample} could be detected due to bigger timing window for ts-TDC. We apply a cascade PMOS(M_{P1},M_{P2},M_{P3}) with larger gate length to boost R_P and get better sensing performance. However, it should be noted that the limited area resources under one electrode cell could be a constraint.

C. Noise Canceling

In the context of the charging-based approach, slight variations among die may lead to disparate experimental results. To mitigate these effects, a sensing flow has been proposed as depicted in Figure 4. The objective of this flow is to eliminate parasitic capacitance ($C_{parasitic}$), which arises from process variation and thermal conditions. This flow starts by determining the electrode shape through the adoption of different fusion pixel patterns, such as 1×1 or 2×2. A noise profiling is firstly performed to capture the noise map of $C_{parasitic}$ on the fabricated COMS chip. Subsequently, continuous sample profiling is performed, subtracting the noise map to obtain the pure sample value. This approach effectively remove most variations,
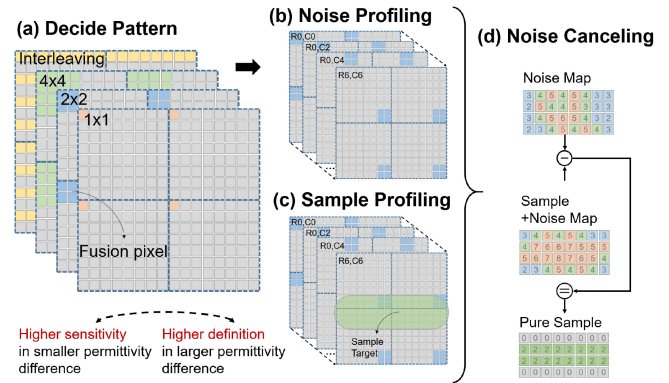

Fig. 4. Proposed sensing flow. (a) decide pattern (b) noise profiling (c) sample profiling (d) noise canceling.
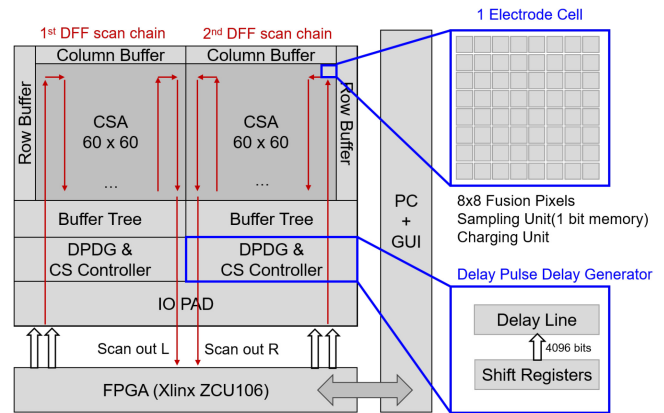

Fig. 5. System diagram and floorplan of the proposed biochip.

however, random thermal noise still poses a challenge. To further overcome these noises, multiple sampling and averaging of several frames can significantly improve precision. These processes can be easily achieved through FPGA digital signal processing.

III. IMPLEMENTATION

The proposed CSA biochip is implemented in standard 0.18 μm 1P6M CMOS technology. The overall system diagram is shown in Fig. 5. Biochip contains 2 sub-arrays with total 60×120 ECs. Each EC, including 64 sensing pixels with the size of 2.25×2.25 μm^2 and 1.5 μm spacing, can work individually and sample with other ECs simultaneously to perform global shutter mode. All 1-bit DFFs in EC are connected as a daisy chain so that data can be easily scanned out after sensing. The CSA controller, consisting of 16-bit shift registers, determines value of $R_{[0]} \sim R_{[7]}$ and $C_{[0]} \sim C_{[7]}$ to formulate equivalent electrode size. It also generates a pulse right after the negative edge of SP signal, as shown in Fig. 3 (d), sending it to delay pulse delay generator (DPDG). DPDG is employed to produce a continuous 126 ps delay of the sampling clock, of which output is connected to DFFs. Notice that the *SCAN* signal in EC is employed as a means of determining whether the mode of operation is data scan or sensing. This is achieved by assigning a value of 1 or 0 respectively to each mode.

The experimental setup is depicted in Fig. 6(a). The Field Programmable Gate Array (FPGA), Xilinx ZCU106 board, is
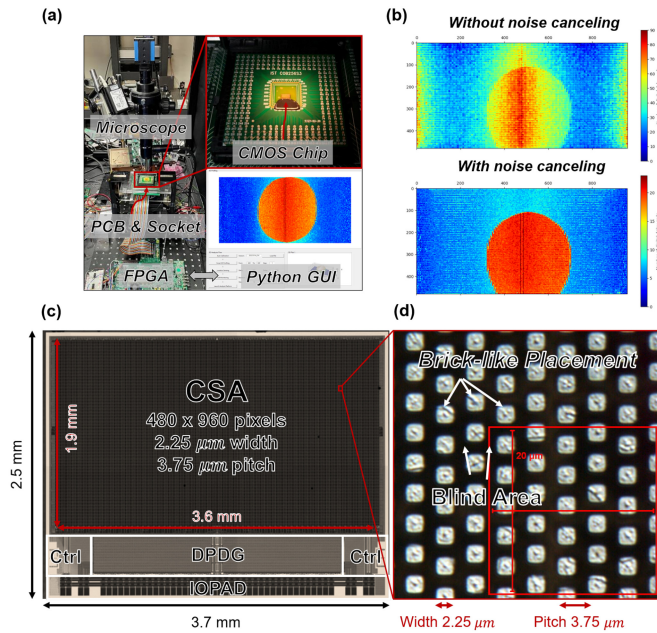
Fig. 6. Experiment and die photo. (a) system configuration. (b) noise canceling result (c) fabricated die (2.5×3.7 mm^2). (d) sensing electrodes (2.25×2.25 μm^2). Note that in (b), red region indicates higher capacitance, whereas blue region indicates lower capacitance.
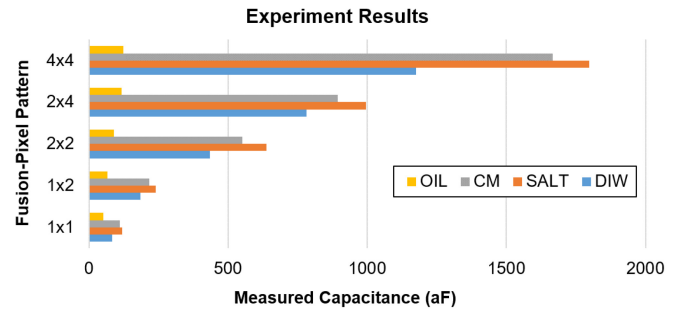

Fig. 7. Measured capacitance of four solutions in different fusion-pixel pattern.
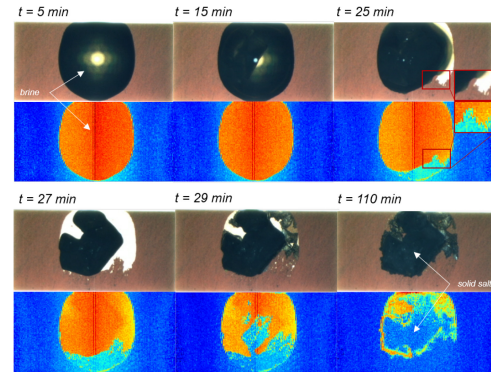

Fig. 8. Optical image and captured image of evaporation process as time for saturated salt solution on chip surface.

utilized to arrange the controlling signal, provide a simple power supply, perform data post-processing (such as histogram or averaging), and transmit data to the personal computer via USB port. The Python programming language is responsible for managing the sensing system, carrying out noise canceling, and providing a graphical user interface (GUI) that facilitates simpler parameter adjustment and visualizes 2D capacitance images. To verify the consistency of capacitance image and optical image, a microscope is necessary. The CMOS chip is packaged on one side only to ensure that the larger space can be further used by other operations.

IV. EXPERIMENT RESULTS

A. Noise Canceling

The experimental results depicted in Fig. 6(b) demonstrate the effectiveness of combining multiple sampling and the proposed noise profiling flow. When noise canceling was not employed, process variation and random noise were distributed throughout the entire array, resulting in an indistinct sample outline. However, by utilizing noise canceling and averaging the sample eight times, most of the variation was eliminated, and the sample shape was clearly delineated. Although some noise remains in the sensing result, it is likely due to leakage current from the turn-off NMOS switch.

B. Fusion-Pixel

To ensure the sensitivity of different fusion-pixel patterns, we use four types of solution, including silicon oil (OIL), *StemFlex^{TM}* stem cell culture medium (CM), saturated salt solution (SALT) and de-ionized water (DIW) as our target. Each electrode cell dynamically adjusts turn-on pixel pattern with 1×1, 1×2, 2×2, 2×4 and 4×4, separately. In addition,

we apply a post-processing methodology by averaging eight frames for each pattern to further reduce random noise. The result is shown in Fig. 7. Measured capacitance reflects the scale of relative permittivity. The value from large to small is SALT, CM, DIW, then OIL, which is consistent with literature. Furthermore, we find that larger detection area truly indicates more significant capacitance; however, it is not proportional to the number of pixels perfectly. Take SALT for example, 2×4 gets 994 *aF*, while enlarging size twice to 4×4 gets 1798 *aF*. This results from the parasitic effect and non-linearity of the charging circuit. Despite this, our platform still demonstrates that sensitivity and spatial resolution can be easily changed by applying a different pattern, which is crucial for most life science applications.

C. Real-Time Monitoring

To verify real-time imaging capability of this system, we chose saturated salt solution as our target sample and put a 10 μl droplet on the chip surface at room temperature, observing the detection result in both liquid and solid state. With four-by-four fusion-pixel enabled, Fig. 8 shows that the liquid droplet gradually becomes smaller before t = 27 min. After that, several pieces of salt crystal appear and reflect only the shape due to no direct contact with chip surface. It represents the longer distance between sample and chip, the minor change of capacitance induced by electrode. In addition, the proposed chip can derive the maximum frame rate of 43 fps at 10 MHz clock speed so that real-time sensing is possible. A summary of proposed capacitive sensor array and its comparison with the state-of-art is provided in Table I.

TABLE I
COMPARISON OF THE PROPOSED CAPACITIVE SENSOR ARRAY WITH THE STATE-OF-ART

Ref.	This work	[4]	[5]	[6]	[7]	[8]	[10]	[12]
Method	CTC + ts-TDC	CVC by CSA	CVC by ChS	CBCM	CFC	RO	CBCM	SR-EIS
Tech. (μm)	0.18	0.35	0.25	0.35	0.35	0.13	0.09	0.18
# of Electrodes	460K	102K	256	64	16	100	65K	131K
Electrode Size (μm)	2.25 $\times$ 2.25	20 $\times$ 20	14 $\times$ 16	50 $\times$ 50	30 $\times$ 30	5 $\times$ 5	0.55 $\times$ 0.72	10 $\times$ 10
Sensitivity	6.896 codes/fF	345 mV/fF	55 mV/fF	350 mV/fF	590 kHz/fF	-	-	-
Fusion Pixel	8$\times$8 Programmable	NO	NO	NO	NO	NO	NO	Super Resolution

CTC: capacitance-to-time converter, ts-TDC: time-sharing time-to-digital converter, CVC: capacitance-to-voltage converter, CSA: charge sensitive amplifier, ChS: charge sharing, CBCM: charge-based capacitance measurement, CFC: capacitance-to-frequency converter, RO: ring oscillator, SR-EIS: super-resolution electrochemical impedance spectroscopy

V. CONCLUSION

A novel CSA system equipped with fusion-pixel is described in this brief, and it enables simple and effective way to adjust electrode size to fit the sample size. Selecting the proper size for life science application can obtain a better sensing result and provide a opportunity to balance spatial resolution and sensitivity. In addition, we present a ts-TDC based approach and noise canceling method to achieve higher number of pixels, i.e., 460,800 pixels, with global shutter mode. The results clearly demonstrate that high-definition morphology of droplets can be captured without an optical microscope. From system perspective, the proposed concepts lead to the great convenience of CMOS Lab-on-Chip and can be further integrated with multiple functions that will contribute to plenty of bio-applications and personalized medicine.

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