A Current Monitoring and Over-Current Detection Circuit for Safe Electrical Stimulation

Yu-Kai Huang, *Graduate Student Member, IEEE*, Ana Rusu, *Member, IEEE*, and Saul Rodriguez, *Member, IEEE*

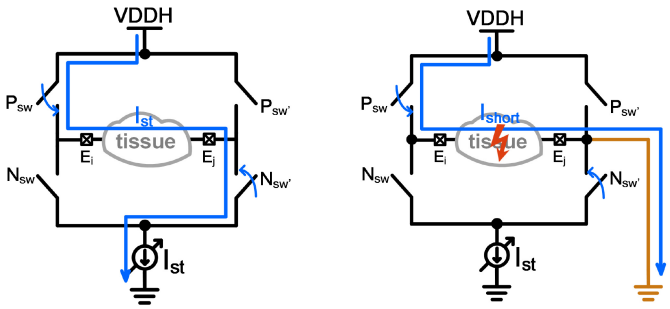
***Abstract*—This brief presents an integrated solution to over-current protection in neuromuscular stimulators. The proposed approach provides fast detection of a single-fault condition, i.e., unintentional electrode short circuit or malfunction of the stimulator, thereby preventing prolonged high-intensity currents from flowing into tissues. In addition, a programmable current threshold enables the system to be also used for monitoring the stimulation intensity. The proposed solution was designed in a 180 nm high-voltage CMOS technology, and its functionality was verified by post-layout simulations in which the safety mechanisms were tested under fault conditions. The implementation only occupies an area of 0.286 mm^2, making it feasible to be embedded in fully integrated NMES stimulators while providing the required patient safety.**

***Index Terms*—Neuromuscular electrical stimulation, current monitoring, over-current detection, safe electrical stimulation, HV CMOS process.**

I. Introduction

NEUROMUSCULAR electrical stimulation (NMES) is a widely used technique in clinical rehabilitation to control the muscle nerves by delivering electrical charges to the tissues. In order to achieve a sufficient depolarizing effect and evoke action potentials, high-intensity short-duration pulses, commonly up to several tens of mA are required [1]. High voltage compliance, well above the voltage rating of a standard CMOS process, is required since electrode-skin/tissue impedance has typical values ranging from a few hundred Ω to 1 kΩ. For this reason, NMES devices are usually powered by high-voltage (HV) sources and also require using HV CMOS technology.

In a conventional H-bridge bipolar stimulator [2], [3], [4], the current strength is controlled by the tail current source (I_{st}). A current path is formed from the HV power supply to the target tissues through switches as demonstrated in Fig. 1(a). Under fault conditions, such as semiconductor device failure, misuse of the device, or poor electrode-ground isolation, a short circuit path from the HV supply via tissues to the ground may be formed as depicted in Fig. 1(b), resulting in over-current stimulation. It has been reported in the literature that over-current stimulation leads to discomfort, pain, or even tissue damage [5], [6]. Therefore, a safety mechanism is an indispensable functional block in a muscular stimulator to cope with over-current stimulation.



(a) normal operation (b) fault condition

Fig. 1. A conventional H-bridge bipolar stimulator.

Placing a series blocking capacitor at the output of a stimulator is a straightforward approach for isolating tissue from the HV DC supply and limiting the maximum charge transfer [7], [8]. However, the blocking capacitor requires to be significantly large in order to minimize the voltage drop induced during normal operation. The capacitance is generally in the order of several μF which is impractical to implement on chip [9].

In this brief, an over-current detection and current monitoring solution that is amenable to on-chip integration is proposed. With the capability to monitor stimulation intensity, the proposed protection scheme requires only a single-fault condition, e.g., an over-current event, to trigger the stimulator into safe mode. In this mode, the system is forced to shut down and the patient is completely disconnected from the HV supply to prevent potential harm caused by over-stimulation.

The rest of this brief is organized as follows. Section II describes the system architecture and the operation principle in detail. Section III presents the circuit implementation of key blocks. The post-layout simulation results are shown in Section IV to demonstrate the functionality. Finally, conclusions are drawn in Section V.

II. System Architecture

A. System Overview

The proposed design for over-current protection is based on current sensing and event-triggered shutdown control as

Manuscript received 2 February 2023; accepted 2 March 2023. Date of publication 6 March 2023; date of current version 12 May 2023. This work was supported by the Swedish Foundation for Strategic Research (SSF) under Project ITM17-0079. This brief was recommended by Associate Editor E. Moisello. *(Corresponding author: Yu-Kai Huang.)*

The authors are with the School of Electrical Engineering and Computer Science, KTH Royal Institute of Technology, 10044 Stockholm, Sweden (e-mail: ykhuang@kth.se; arusu@kth.se; saul@kth.se).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2023.3252804.

Digital Object Identifier 10.1109/TCSII.2023.3252804

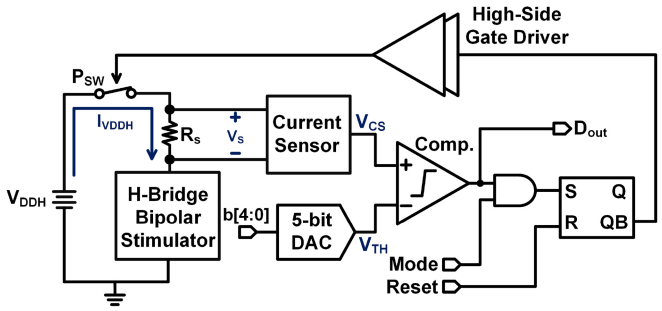


Fig. 2. Block diagram of the proposed system.

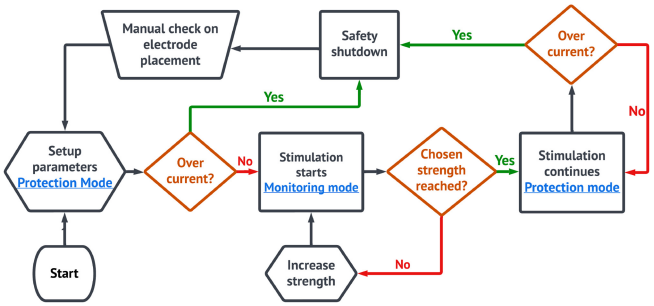
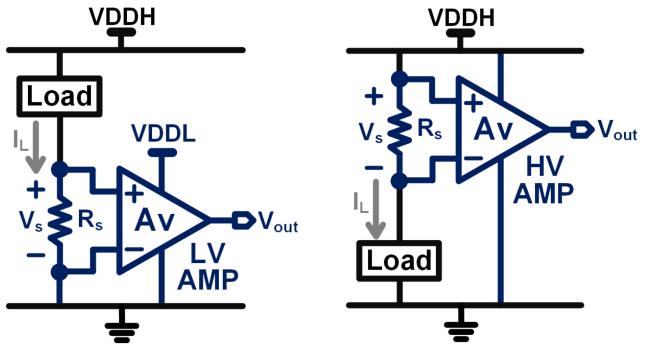


Fig. 3. Flow chart of system operation.



(a) low-side sensing (b) high-side sensing

Fig. 4. Conceptual diagram of current-shunt monitors.

illustrated in Fig. 2. It comprises four fundamental circuits: i) a current sensor, ii) a comparator with programmable thresholds, iii) digital logic for mode selection and shutdown control, and iv) a high-side gate driver. The current sensor monitors the current, I_{VDDH}, that flows from the HV supply to tissues via the H-bridge. Its output, V_{CS}, is a voltage proportional to the sensed current. V_{CS} is applied to a continuous-time comparator and compared with a voltage threshold V_{TH}. The comparison result, D_{out}, is interpreted differently depending on the mode selection. In the protection mode (Mode = 1), D_{out} indicates the occurrence of an over-current event that is registered in an SR latch. Once the over-current is detected, D_{out} sets the SR latch, and the high-side gate driver then turns off the PMOS switch P_{SW} that connects the HV power supply to the stimulator, preventing high-intensity $I_{VDDH}$from flowing into tissues. In monitoring mode (Mode = 0), the shutdown control is disabled and D_{out} tells if the chosen stimulation level is reached or not. Fig. 3 shows the system operation flow. To start an NMES treatment, the stimulation parameters such as stimulation frequency, pulse width, current intensity, and over-current threshold are set. The system is initially in protection mode to ensure protection during start-up and configuration. The system then starts stimulation and changes to monitoring mode. Once the chosen strength is reached, the electrical treatment continues and the system changes to protection mode to prevent an over-current stimulation event. To support the operation of these two modes, V_{TH} requires programmability such that different levels of current strength can be distinguished in monitoring mode, and various over-current thresholds can be defined to accommodate diverse safety scenarios.

B. Current Sensing

The current-shunt monitor architecture [10] shown in Fig. 4 is chosen for current sensing as it offers a simple approach to measure the current flowing between a voltage source and a load. In this architecture, a small shunt resistor, R_S, is inserted into the circuit, and a voltage, V_S, proportional to the load current is induced across R_S. Therefore, the current sensing can be accomplished by measuring this voltage difference using an instrumentation amplifier as demonstrated in Fig. 4. Depending on the placement of R_S, there are two possible topologies: low-side current sensing [11] (Fig. 4(a)) and high-side current sensing [12] (Fig. 4(b)).

In the low-side sensing architecture, the circuit implementation of the instrumentation amplifier is simpler. Nonetheless, the major disadvantage of this topology is its lack of ability to detect short-circuit currents not flowing through R_S. For instance, a situation in which an electrode is touching ground will not be detected. For this reason, high-side current sensing is selected and implemented in this system. However, this topology poses design challenges because of the high input common-mode voltage ($V_{CM,in}$). Due to the small value of R_S, both inputs of the instrumentation amplifier can be considered to be connected to VDDH. As a result, its implementation requires a HV-tolerant interface with a high common-mode rejection ratio (CMRR) and voltage translation to a low-voltage output such that the rest of the circuits can be implemented using standard low-voltage transistors, offering lower power consumption and saving silicon area.

C. System Programmability

It has been reported that the safety limits and the patient's comfort level have a direct correlation to charge injection density (C/cm^2), electrode material, and stimulation protocols [5], [13], [14]. These factors combined with individual variances between patients require the current threshold to be programmable. The proposed design provides a programmable current threshold as shown in Fig. 2. In this design, a 5-bit digital-to-analog converter provides tunable current thresholds, ranging from 2.5 mA to 80 mA with a stepsize of 2.5 mA. This current range covers the current intensity used in general neuromuscular electrical stimulation [1].

III. Circuit Implementation

The building blocks of the proposed system were designed and implemented using a 180 nm CMOS technology that provides 40 V high-voltage transistors with 18 V gate-oxide breakdown.

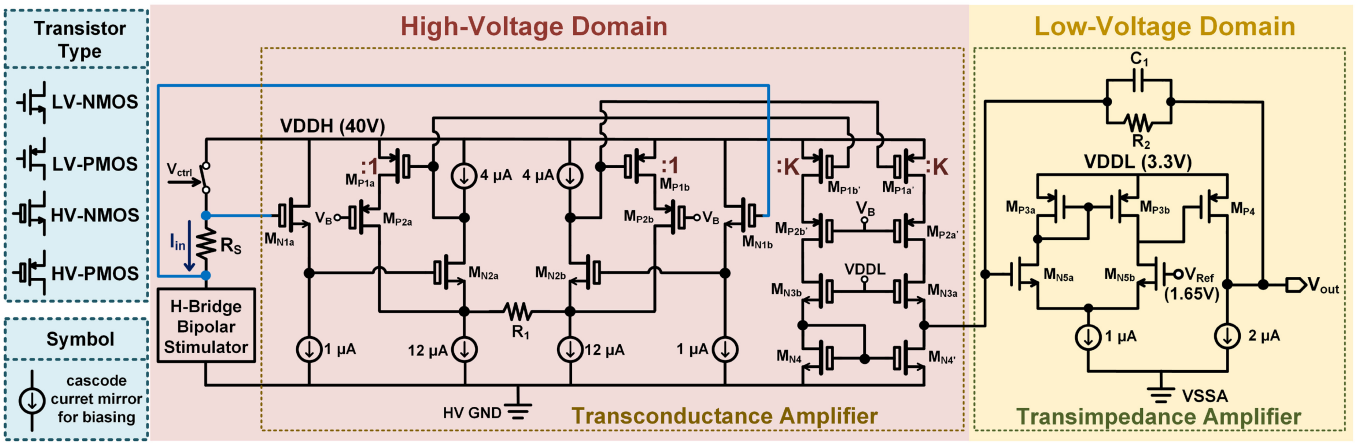


Fig. 5. Schematic of the current-sensing amplifier.

A. High-Side Current Sensor

Fig. 5 shows the transistor-level implementation of the high-side current sensor. It consists of a high-voltage transconductance amplifier (HV-TCA) and a low-voltage transimpedance amplifier (LV-TIA). The HV-TCA is implemented with double-diffused MOS (DMOS) which allows high-voltage operation. The HV-TCA converts the voltage across R_S into an output current that can be later processed by LV-TIA.

The input transistors $M_{N1a,b}$ are configured as common-drain amplifiers in order to shift down the input DC level and set proper DC operating points of $M_{N2a,b}$. This is necessary because of the high $V_{CM,in}$ which is around VDDH. The voltage difference between $V_{G,MN1a}$ and $V_{G,MN1b}$ is sensed by the degeneration resistor R_1 and the resulting current is mirrored to the output by $M_{P1a/b}$ and $M_{P1a'/b'}$. The output voltage of the HV-TCA is limited within the safe-operation-area (SOA) of LV transistors in this CMOS technology by cascoding M_{N3}. The negative feedback at the LV-TIA results in an input impedance much lower than $1/g_{m,M_{N3}}$, enabling it to efficiently sink the output current of the HV-TCA. This current is then converted into voltage through the feedback resistor R_2. The bandwidth of the current-sensing amplifier is determined by R_2 and C_1. These components provide first-order filtering to suppress high-frequency voltage spikes induced by the on-off transition of the switches in the H-bridge structure during normal operation. As a result, the voltage gain of the current sensing amplifier is approximately given by:

$$A_{V,CSAmp}(s) = \frac{V_{out}}{V_{in}}(s) \cong K\frac{R_2}{R_1}\frac{1}{1+sR_2C_1} \tag{1}$$

where K is the W/L ratio of $M_{P1a'/b'}$ to $M_{P1a/b}$. The resistors R_1 and R_2, and the current mirror are well matched in layout, making the voltage gain less sensitive to process variations. Besides voltage gain error (e_{gain}), the accuracy of the current sensing is also limited by the current-to-voltage conversion at the shunt resistor (e_{shunt}). Since standard on-chip resistors have a large variation in resistance, some means of calibration or the use of a thin film precision resistor [15] may be necessary to reduce this error. Finally, the input common-mode

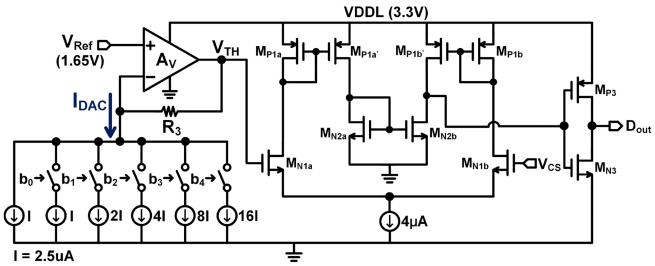


Fig. 6. Schematic of the comparator and 5-bit DAC.

voltage, $V_{CM,in}$, introduces an offset error (e_{offset}) that can be derived by:

$$e_{offset} = \frac{V_{CM,in}}{V_{shunt}} 10^{-CMRR(dB)/20} \times 100\% \tag{2}$$

As a consequence, the first-order total error of the current sensing is given by [16]:

$$e_{total} = \sqrt{e_{gain}^2 + e_{shunt}^2 + e_{offset}^2} \tag{3}$$

Accordingly, the current-sensing amplifier requires an accurate gain, a high-precision shunt resistor, and a high CMRR in order to sense a small V_{shunt} in the presence of a high $V_{CM,in}$.

B. Comparator With Programmable Thresholds

The continuous-time comparator in Fig. 6 is implemented by using a conventional OTA-based push-pull comparator [17] as it offers lower latency compared to the open-drain output counterpart. The comparator compares the output of the current sensing amplifier (V_{CS}) and a tunable threshold voltage (V_{TH}) from the DAC's output, and produces the output digital signal D_{out} that is used for shutdown control and stimulation strength monitoring. The programmability of the threshold voltage is achieved by a 5-bit binary-weighted current-scaling DAC and a transimpedance amplifier. This architecture offers high power efficiency and simplicity for low-resolution designs. The current threshold can be calculated by:

$$I_{th} = \frac{R_1R_3(\sum_{i=0}^{4} b_i 2^i I + I)}{KR_SR_2}. \tag{4}$$

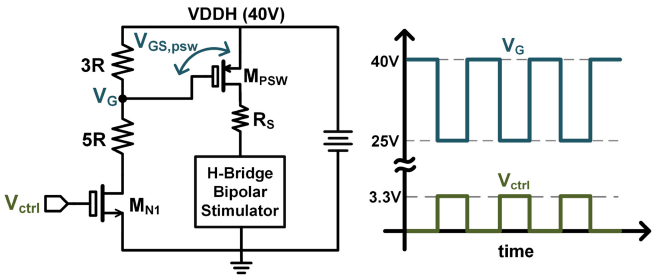


Fig. 7. Schematic of the high-side gate driver.

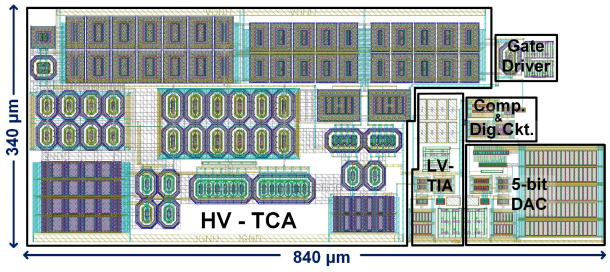


Fig. 8. Layout of the proposed design.

C. High-Side Gate Driver

Fig. 7 presents the high-side gate driver circuit that controls the PMOS switch M_{PSW} which is used to isolate the H-bridge driver from the HV supply when an over-current event is identified. The gate driver is based on an open-drain topology with a resistive voltage divider [18]. This is a flexible solution that allows to define proper driving voltage levels only by sizing the resistors. Accordingly, M_{PSW} is driven on/off by an appropriate $V_{GS,psw}$ without exceeding the gate-oxide breakdown voltage which is 18 V in this CMOS technology.

IV. Post-Layout Simulation Results

The layout of the design is shown in Fig. 8. The whole solution occupies a silicon area of 0.286 mm^2.

Fig. 9 shows a post-layout simulation of an over-current event-triggered shutdown control when the system is in protection mode. The testbench emulates a situation in which the electrode is accidentally shorted to ground during stimulation. In this example, the over-current threshold is set to 50 mA. As shown in the plot, the stimulator circuit constantly delivers biphasic current stimuli until the short-circuit event occurs. At $t = 2.05$ ms, a short-circuit current that exceeds the over-current threshold is observed, and the system immediately responds to this abrupt change in current, resulting in an increase of the sensed voltage V_{CS}. Once V_{CS} exceeds the threshold voltage that corresponds to 50 mA current threshold, the high-side gate driver turns off the PMOS switch and shuts down the system. The simulated response time is 1.57 µs.

Fig. 10 presents simulation waveforms of the proposed system when it is configured in monitoring mode. In this demonstration, the stimulation current is set to 10 mA and the current threshold increases in steps of 2.5 mA. Both the stimulation current and the current threshold are translated into the voltages V_{CS} and V_{TH} respectively before they are processed by the comparator. In the first four cycles, the output

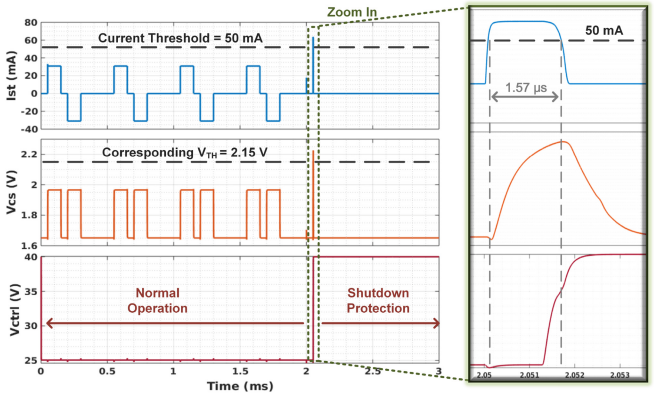


Fig. 9. Simulated waveforms of event-triggered shutdown protection.

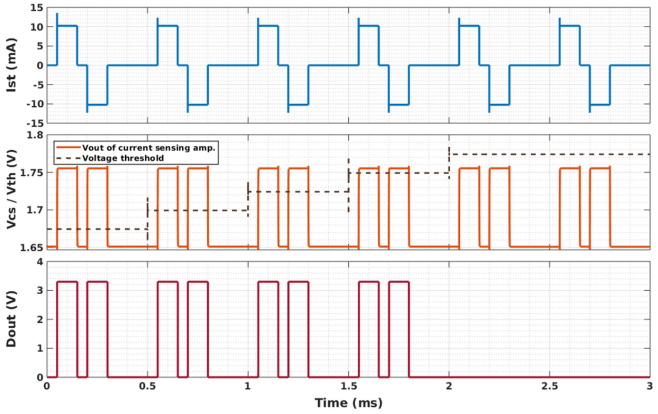


Fig. 10. Simulated waveforms of stimulation monitoring.

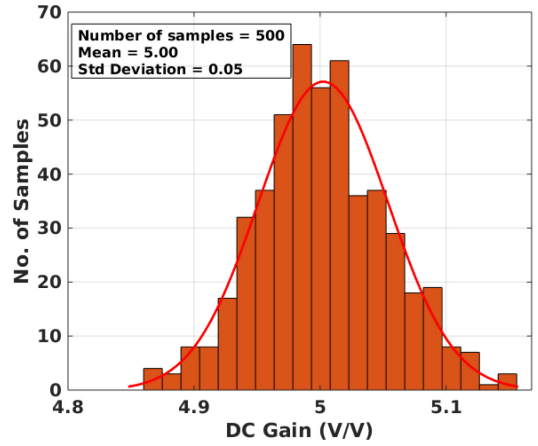
TABLE I
Specification & Design Summary

Parameter	This work
Technology	180 nm HV CMOS
LV/HV Supply voltage	3.3 V / 40 V
Shunt Resistor	2 Ω
Input current sensing range	0 - 80 mA
CMRR of current-sensing amplifier	103.7 dB
Maximum total error in current sensor	5.2 %
Programmable current threshold	2.5 - 80 mA with 2.5 mA/step
Response time to an over-current event	$<$ 2 µs
Static power consumption	34 µA from the HV supply 15 µA from the LV supply
Silicon area	840 µm × 340 µm

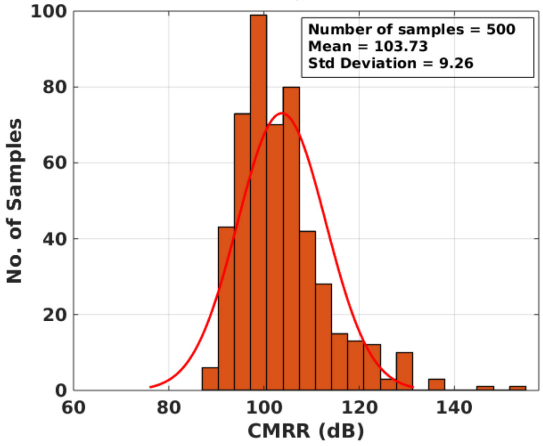
of the comparator D_{out} toggles between low and high, meaning that more iterations are required. Once V_{TH} exceeds V_{CS}, D_{out} remains low, indicating that the current measurement has been completed.

Fig. 11 presents Monte Carlo simulation results of the current sensing amplifier (Fig. 5) under process variations and mismatch. The statistical results show that the current sensing amplifier provides a precise voltage gain and a sufficiently high CMRR. Based on (3), it corresponds to a 5.2% maximum total error assuming that R_S has 0.1% tolerance [15].

Table I shows a summary of the design specifications and performance metrics of the proposed design.



(a) DC gain



(b) CMRR

Fig. 11. Monte Carlo simulation results (500 samples with Gaussian distribution are simulated).

V. Conclusion

This brief presented an integrated solution that targets patient safety during NMES treatment. The proposed approach is able to monitor stimulation current levels and detect over-current events caused by device malfunction, or unintentional short circuits. The circuits are designed in a 180 nm CMOS process that offers 40V DMOS devices and occupy a silicon area of approximately 0.286 mm^2 while consuming only a few tens of µA. Being compact and low-power, the proposed solution has a strong potential to serve as an additional functional block in next-generation fully integrated NMES stimulators.

References

[1] N. A. Maffiuletti, "Physiological and methodological considerations for the use of neuromuscular electrical stimulation," *Eur. J. Appl. Physiol.*, vol. 110, no. 2, pp. 223–234, 2010.

[2] Y.-K. Huang, A. Rusu, and S. Rodriguez, "A 4-channel NMES IC for wearable applications," in *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*, 2021, pp. 1–5.

[3] J. V. Shah, C. J. Quinkert, B. J. Collar, M. T. Williams, E. N. Biggs, and P. P. Irazoqui, "A highly miniaturized, chronically implanted ASIC for electrical nerve stimulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 16, no. 2, pp. 233–243, Apr. 2022.

[4] S. Oh et al., "Light-controlled biphasic current stimulator IC using CMOS image sensors for high-resolution retinal prosthesis and *invitro* experimental results with rd1 mouse," *IEEE Trans. Biomed. Eng.*, vol. 62, no. 1, pp. 70–79, Jan. 2015.

[5] M. A. Rahman, N. S. Tharu, S. M. Gustin, Y.-P. Zheng, and M. Alam, "Trans-spinal electrical stimulation therapy for functional rehabilitation after spinal cord injury: Review," *J. Clin. Med.*, vol. 11, no. 6, p. 1550, 2022.

[6] D. R. Merrill, M. Bikson, and J. G. R. Jefferys, "Electrical stimulation of excitable tissue: Design of efficacious and safe protocols," *J. Neurosci. Methods*, vol. 141, no. 2, pp. 171–198, 2005.

[7] X. Liu, A. Demosthenous, and N. Donaldson, "An integrated implantable stimulator that is fail-safe without off-chip blocking-capacitors," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 3, pp. 231–244, Sep. 2008.

[8] M. Van Dongen and W. Serdijn, *Design of Efficient and Safe Neural Stimulators*. Cham, Switzerland: Springer, 2016.

[9] N. Butz, A. Taschwer, S. Nessler, Y. Manoli, and M. Kuhl, "A 22 V compliant 56 μW twin-track active charge balancing enabling 100% charge compensation even in monophasic and 36% amplitude correction in biphasic neural stimulators," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2298–2310, Aug. 2018.

[10] S. Ziegler, R. C. Woodward, H. H.-C. Iu, and L. J. Borle, "Current sensing techniques: A review," *IEEE Sensors J.*, vol. 9, no. 4, pp. 354–376, Apr. 2009.

[11] V. B. Vulligaddala, R. Adusumalli, S. Singamala, and M. B. Srinivas, "A digitally calibrated bandgap reference with 0.06% error for low-side current sensing application," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2951–2957, Oct. 2018.

[12] L. Xu, J. H. Huijsing, and K. A. A. Makinwa, "A ±4-A high-side current sensor with 0.9% gain error from -40 °C to 85 °C using an analog temperature compensation technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3368–3376, Dec. 2018.

[13] C. Günter, J. Delbeke, and M. Ortiz-Catalan, "Safety of long-term electrical peripheral nerve stimulation: Review of the state of the art," *J. Neuroeng. Rehabil.*, vol. 16, no. 1, pp. 1–16, 2019.

[14] A. Butterwick, A. Vankov, P. Huie, Y. Freyvert, and D. Palanker, "Tissue damage by pulsed electrical stimulation," *IEEE Trans. Biomed. Eng.*, vol. 54, no. 12, pp. 2261–2267, Dec. 2007.

[15] "High power aluminum nitride, wraparound surface mount, precision thin film non-magnetic chip resistor." Vishay Intertechnology. Jan. 2022. [Online]. Available: https://www.vishay.com/docs/60130/pcnm.pdf

[16] "Simplifying current sensing—How to design with current sense amplifiers, [rev. A]," Data Sheet, Texas Instrum., Dallas, TX, USA, 2020.

[17] H. Y. Yang and R. Sarpeshkar, "A time-based energy-efficient analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1590–1601, Aug. 2005.

[18] C.-C. Wang, T.-C. Sung, Y.-H. Wu, C.-H. Hsu, and D. Shmilovitz, "A reconfigurable 16-channel HV stimulator ASIC for spinal cord stimulation systems," in *Proc. IEEE Asia–Pacific Conf. Circuits Syst.*, 2012, pp. 300–303.