Homogeneity Enforced Calibration of Stage Nonidealities for Pipelined ADCs

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***Abstract*—Pipelined analog-to-digital converters (ADCs) are fundamental components of various signal processing systems requiring high sampling rates and a high linearity. Over the past years, calibration techniques have been intensively investigated to increase the linearity. In this brief, we propose an equalization-based calibration technique which does not require knowledge of the ADC input signal for calibration. For that, a test signal and a scaled version of it are fed into the ADC sequentially, while only the corresponding output samples are used for calibration. Several test signal sources are possible, such as a signal generator (SG) or the system application (SA) itself. For the latter case, the presented method corresponds to a background calibration technique. Thus, slowly changing errors are tracked and calibrated continuously. Because of the low computational complexity of the calibration technique, it is suitable for an on-chip implementation. Ultimately, this brief contains an analysis of the stability and convergence behavior as well as simulation results.**

***Index Terms*—Pipelined ADC, ADC calibration, equalization-based, background calibration, adaptive algorithm.**

I. Introduction

MANY state-of-the-art signal processing systems require analog-to-digital converters (ADCs) with a high sampling rate, a high dynamic range, and a high linearity. Pipelined ADCs are a popular choice for such challenging applications. As discussed in [1], the time-interleaved architecture of pipelined ADCs enables high sampling frequencies, albeit it introduces additional error sources. Besides random errors, i.e., thermal and quantization noise, digital-to-analog converter (DAC) or gain mismatches cause systematic errors. To maintain a high linearity, calibration techniques for these systematic errors become inevitable and were heavily investigated throughout the past decades [2], [3]. To reduce power consumption and relax the analog design, calibration techniques are preferably carried out in the digital domain [4]. These techniques may be grouped in equalization-, histogram-, and correlation-based approaches. A crucial part of calibration techniques is the identification of the ADC nonidealities [4]. Typically, this requires either long test times [5], [6], [7], exceedingly linear test signal generators (SGs) [8], [9], or additional hardware components [10], [11].

Much effort was spent to overcome the need of a highly linear test SG [12]. In [13] a histogram-based method is introduced, which relaxes the linearity requirements of the test SG heavily. This is achieved by injecting a test signal twice to the ADC, whereas for the second time, it is shifted by a constant voltage-offset. Therewith, the nonlinear test signal is identified and it is possible to subsequently estimate the ADC nonideality. In literature, this method is referred to as the stimulus error identification and removal (SEIR) approach. Improvements can be found in [14], [15], which address enhanced robustness concerning reference voltage stationarity and a reduced hardware overhead, respectively. The identification of the ADC nonidealities in [16] is based on the same principle as the SEIR approach. However, by using a segmented nonlinearity model it significantly reduces the required test time.

As the ADC under calibration is nonlinear, it violates the linearity conditions. Specifically, a nonlinear system $f(x) : \mathbb{R} \rightarrow \mathbb{R}$ violates at least one of the following two conditions:

$$f(\alpha x) = \alpha f(x) \ldots \text{ homogeneity} \tag{1}$$

$$f(x+y) = f(x) + f(y) \ldots \text{ additivity} \tag{2}$$

with x, y as the system inputs and an arbitrary constant $\alpha \in \mathbb{R}$. A closer look at the principle of [16] shows that in this sense, it relies on a weak form of additivity, where the constant voltage-offset replaces the second input signal y in (2).

In this brief, we propose a calibration technique that focuses on the homogeneity condition in (1). The ADC calibration is achieved by injecting a test signal twice into the ADC, whereas for the second time, it is scaled by a constant factor α. From here on the calibration technique will be referred to as homogeneity enforced calibration (HEC) approach. By scaling the input signal with α, the HEC approach replaces the necessity for a highly constant voltage-offset. The scaling, however, can easily be implemented using a voltage divider. Along with a low complex post correction model, the

Manuscript received 11 July 2022; revised 9 September 2022 and 31 October 2022; accepted 28 November 2022. Date of publication 9 December 2022; date of current version 29 March 2023. This work was supported by the Linz Center of Mechatronics (LCM) GmbH as part of a K2 Project. K2 Projects are financed using funding from the Austrian COMET K2 Program. The COMET K2 Projects at LCM are supported in part by the Austrian Federal Government; in part by the Federal State of Upper Austria; in part by the Johannes Kepler University; and in part by the Scientific Partners, which form part of the COMET K2 Consortium. This brief was recommended by Associate Editor D. G. Muratore. *(Corresponding author: Matthias Wagner.)*

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Digital Object Identifier 10.1109/TCSII.2022.3227441

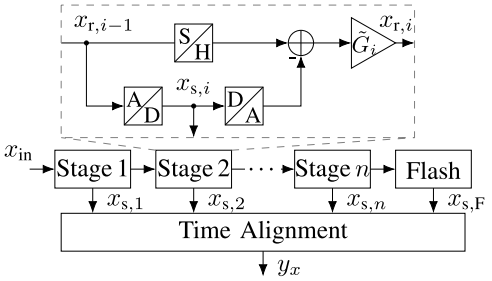

Fig. 1. Block diagram of a pipelined ADC including the stage building blocks.

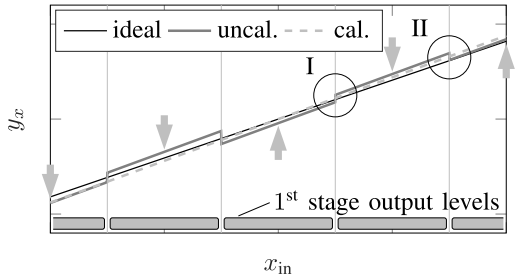

Fig. 2. Transition function affected by errors in the first stage.

HEC approach is suitable for off- as well as on-chip calibration. Nonetheless, injecting a test signal twice prevents an implementation without the interruption of the sampling task of the ADC. Therefore, this brief additionally introduces an extension of the HEC approach that allows for background calibration. It will be shown that the HEC approach exhibits

- a fundamentally novel estimation approach,
- faster convergence times,
- high spurious-free dynamic range (SFDR) improvement,
- and lower remaining integral nonlinearity (INL),

compared to prior work [5], [7], [17], while requiring only a few additional hardware components.

The rest of this brief is organized as follows. In Section II, a detailed derivation of the ADC output signal including its nonidealities is presented. A post correction model is discussed in Section III. The HEC approach is derived in Section IV including analysis of its convergence and stability behavior. The findings are numerically verified in Section V. Finally, Section VI concludes this brief.

II. System Model

This section provides an introduction to the ADC model employed in this brief. Furthermore, the impact of DAC and gain mismatches caused, e.g., by component variation, aging- or temperature effects, on the transition function of a pipelined ADC is derived in detail.

Typically, pipelined ADCs consist of n equally built stages followed by a final flash ADC stage. As Fig. 1 shows, each stage involves a sample and hold (S&H) block, a stage ADC, a stage DAC, a subtracter, and a residue amplifier. Conventional architectures combine the DAC, the subtracter, and the amplifier in a switched capacitor circuit, referred to as a multiplying DAC entity. Because of the S&H blocks, each stage simultaneously resolves a stage output with respect to consecutive input voltages. These stage outputs $x_{\mathrm{s},i}$, $i = 1, \ldots, n$, are then time aligned and combined to form the overall ADC output y_x, where the index i refers to the stage under consideration. By neglecting the time alignment to increase readability, the output can be expressed as

$$y_x = x_{\mathrm{s},1} + \frac{x_{\mathrm{s},2}}{G_1} + \frac{x_{\mathrm{s},3}}{G_1 G_2} + \ldots + \frac{x_{\mathrm{s,F}}}{\prod_{i=1}^{n} G_i}, \tag{3}$$

with the ideal stage gains G_i and $x_{\mathrm{s,F}}$ denoting the output of the final flash ADC. In the presence of DAC and gain mismatches, the real stage outputs do not match the ideal ones. Thus, the output signal in (3) is distorted.

According to Fig. 1, the residue signal of each stage may be written as

$$x_{\mathrm{r},i} = \tilde{G}_i\Big(x_{\mathrm{r},i-1} - x_{\mathrm{s},i} - e^{\mathrm{DA}}_{\mathrm{s},i}(x_{\mathrm{s},i})\Big), \tag{4}$$

where $\tilde{G}_i$ denotes nonideal stage gains and $e^{\mathrm{DA}}_{\mathrm{s},i}(x_{\mathrm{s},i})$ represents errors caused by DAC mismatches. The argument of $e^{\mathrm{DA}}_{\mathrm{s},i}(x_{\mathrm{s},i})$ should point out that each stage output level can result in a different DAC error. By introducing the quantization error $e^{\mathrm{q}}_{\mathrm{s},i}$, the stage output can be expressed as

$$x_{\mathrm{s},i} = x_{\mathrm{r},i-1} - e^{\mathrm{q}}_{\mathrm{s},i}. \tag{5}$$

Inserting (5) into (4) yields the transformed residue signal

$$x_{\mathrm{r},i} = \tilde{G}_i\Big(e^{\mathrm{q}}_{\mathrm{s},i} - e^{\mathrm{DA}}_{\mathrm{s},i}(x_{\mathrm{s},i})\Big), \tag{6}$$

which depends only on nonideal stage gains, the stage quantization signal and the DAC errors. With (5) and (6) the ADC output signal in (3) may be written as

$$\begin{aligned} y_x = x_{\mathrm{in}} &+ \zeta_1 e^{\mathrm{q}}_{\mathrm{s},1} - (1+\zeta_1) e^{\mathrm{DA}}_{\mathrm{s},1} + \frac{\zeta_2}{G_1} e^{\mathrm{q}}_{\mathrm{s},2} \\ &- \frac{1}{G_1}(1+\zeta_2) e^{\mathrm{DA}}_{\mathrm{s},2} + \ldots + \frac{\zeta_n}{\prod_{i=1}^{n-1} G_i} e^{\mathrm{q}}_{\mathrm{s},n} \\ &- \frac{1}{\prod_{i=1}^{n-1} G_i}(1+\zeta_n) e^{\mathrm{DA}}_{\mathrm{s},n} + \frac{e^{\mathrm{q}}_{\mathrm{s,F}}}{\prod_{i=1}^{n} G_i}. \end{aligned} \tag{7}$$

where $e^{\mathrm{q}}_{\mathrm{s,F}}$ denotes the quantization error of the final flash ADC. Note that for the sake of readability, the argument of the DAC error $e^{\mathrm{DA}}_{\mathrm{s},i}(x_{\mathrm{s},i})$ is omitted as it is clear from the context and an relative gain error ζ_i is introduced which results in a nonideal residue gain $\tilde{G}_i = G_i(1+\zeta_i)$. The equation above shows, that nonidealities in less significant stages marginally affect the overall ADC output because they are weighted with the inverse product of all previous stage gains. Consequently, sufficient calibration performances for many applications might be achieved by considering only the most significant stages [11], [17]. Additionally, (7) shows that $\zeta_i \neq 0$ distorts the transition function by a remaining stage quantization error. DAC errors, on the other hand, add an offset to the corresponding stage output levels. This is illustrated in Fig. 2, which shows an exemplary transition function of a pipelined ADC affected by errors in the first stage. Additionally, Fig. 2 highlights two types of discontinuities, i.e., missing codes (I), and nonmonotonous errors (II). Because of these discontinuities, the transition function is not invertible, such that applying the inverse system for calibration is not feasible. Nonetheless, as shown in [18], this issue may be coped by using the stage outputs separately for calibration.

III. Post Correction Model

The post correction model employed in this brief corrects the discontinuities by adding corrective offsets to the corresponding stage output levels. In Fig. 2, the output levels of the first stage are schematically illustrated. The added offsets serve as parameters to be identified for the calibration and are summarized in a parameter vector $\boldsymbol{\theta}$. Let p denote the total number of stage output levels of all stages used for calibration. Storing all offsets would usually require a vector of length p. However, there are some dependencies between the offsets of consecutive stages, by means that one parameter in the i-th stage can be represented by an offset of all parameters in the $(i+1)$-th stage. Eliminating these dependencies by excluding the redundant entries of $\boldsymbol{\theta}$ results in a parameter vector of length $\bar{p} = p - (q-1)$, with q denoting the number of stages considered for calibration.[1] The entries of $\boldsymbol{\theta}$ that contribute to a particular ADC output are isolated by the selection vector $\mathbf{h}_x$. To do so, the corresponding entries of $\mathbf{h}_x$ are set to 1 and 0 for active and inactive output levels, respectively. However, gain errors do not only affect one dedicated stage output level but all corresponding stage output levels similarly. It can be shown that the employed post correction model is more effective if one parameter of each stage affects not only one stage output level but all output levels of the corresponding stage. This may be achieved by replacing q entries of $\mathbf{h}_x$, which are related to different stages[2] with $z_j = G_{j-1} z_{j-1} + x_{\mathrm{s},j}$, where $z_1 = x_{\mathrm{s},1}$ and $j = 2 \ldots q$. For example, consider a two stage ADC with three output levels in each stage, as well as an input signal x_{in} such that the middle output level of the first stage and the highest output level of the second stage is active. This yields the selection vector $\mathbf{h}_x^T = \begin{bmatrix} 1 & x_{\mathrm{s},1} & 0 & 0 & G_1 x_{\mathrm{s},1} + x_{\mathrm{s},2} \end{bmatrix}$, with $(\cdot)^T$ denoting transposition. Finally, the post-corrected output signal can be written as

$$y_x^{\mathrm{c}} = y_x + \mathbf{h}_x^T \boldsymbol{\theta}. \tag{8}$$

The impact of this post correction model to the transition function is illustrated in Fig. 2. Therein the arrows indicate the offsets applied for calibration, and the dashed line represents the corrected transition function. As can be seen, the post correction model only eliminates the discontinuities, while an overall gain error remains. This overall gain error, however, does not affect the ADC linearity and may be eliminated in an additional processing step.

IV. Homogeneity Enforced Calibration

The basic structure of the HEC approach is shown in Fig. 3. There, the first step is to feed an input sample $x_{\mathrm{in}}[k]$ into the ADC, where k is the sample index. This sample may originate from an SG or from the system application (SA) itself stored in an S&H block. The corresponding output sample is denoted as $y_x[k]$. In the second step, the same input sample is scaled by a factor α, and subsequently fed into the ADC. The resulting ADC output sample is denoted as $y_{\alpha x}[k]$. Since the

[1] In this brief, always the parameter corresponding to the lowest stage output level is excluded.

[2] Every output level providing $x_{\mathrm{s},i} \neq 0$ may be utilized for the replacement. In this brief, the highest stage output level of each considered stage is used.

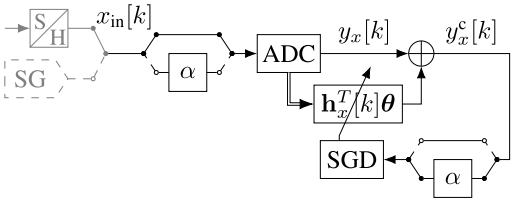

Fig. 3. Block diagram of the HEC approach including different test signal sources.

ADC violates the homogeneity condition, the output $y_{\alpha x}[k]$ is in general not equal to $\alpha y_x[k]$. Applying the post correction in (8) on both values yields the inequality

$$y_{\alpha x}[k] + \mathbf{h}_{\alpha x}^T[k]\boldsymbol{\theta} \neq \alpha\big(y_x[k] + \mathbf{h}_x^T[k]\boldsymbol{\theta}\big). \tag{9}$$

The squared difference of these two terms is used as a cost-function according to

$$J[k] = \big(y_{\alpha x}[k] + \mathbf{h}_{\alpha x}^T[k]\boldsymbol{\theta} - \alpha\big(y_x[k] + \mathbf{h}_x^T[k]\boldsymbol{\theta}\big)\big)^2. \tag{10}$$

A standard approach to identify the parameters $\boldsymbol{\theta}$ in the equation above is the method of least squares [19]. However, for this approach an appropriate number N of output samples must be stored and it features a high computational complexity with $\mathcal{O}(\bar{p}^2 N)$. Although the computational complexity may be relaxed with the approximate least squares (ALS) algorithm [20], still storing N output samples is necessary. This drawback is overcome by adaptive algorithms, such as the HEC approach derived in the following. Applying the stochastic gradient descent (SGD) method to (10) yields the parameter update equation

$$\boldsymbol{\theta}[k] = \boldsymbol{\theta}[k-1] - \mu \Delta\mathbf{h}[k]\big(\Delta y[k] + \Delta\mathbf{h}^T[k]\boldsymbol{\theta}[k-1]\big), \tag{11}$$

where $\Delta y[k] = y_{\alpha x}[k] - \alpha y_x[k]$, $\Delta\mathbf{h}^T[k] = \mathbf{h}_{\alpha x}^T[k] - \alpha\mathbf{h}_x^T[k]$ and μ denotes the step-size [21]. In general each update step requires $2\bar{p}$ digital multiplications which translates to an overall computational complexity of $\mathcal{O}(\bar{p}N)$ for N update steps. Moreover, the already low computational complexity is further reduced by the large number of zeros in $\Delta\mathbf{h}^T$. The proposed HEC approach in (11) is analyzed with respect to convergence, stability, and practical aspects in the following.

A. Convergence

It can be shown that the presented parameter estimation converges on the mean toward the corresponding minimum mean squared error (MMSE) solution [22]. To prove this, the MMSE solution is computed first, utilizing the mean squared error (MSE) cost-function

$$J = E\Big[\big(\Delta y[k] + \Delta\mathbf{h}^T[k]\boldsymbol{\theta}\big)^2\Big], \tag{12}$$

with $E[\cdot]$ denoting the expected value. Minimizing the equation above yields $\boldsymbol{\theta}_0 = -\mathbf{R}_{\mathbf{hh}}^{-1}\mathbf{r}_{\mathbf{h}y}$, with the autocorrelation matrix $\mathbf{R}_{\mathbf{hh}} = E\big[\Delta\mathbf{h}[k]\Delta\mathbf{h}^T[k]\big]$ and the cross-correlation vector $\mathbf{r}_{\mathbf{h}y} = E\big[\Delta\mathbf{h}[k]\Delta y[k]\big]$. Subtracting the MMSE solution $\boldsymbol{\theta}_0$ from both sides of (11), and using $\mathbf{v}[k] = E[\boldsymbol{\theta}[k] - \boldsymbol{\theta}_0]$, results in

$$\mathbf{v}[k] = (\mathbf{I} - \mu\mathbf{R}_{\mathbf{hh}})\mathbf{v}[k-1]. \tag{13}$$

Assuming that μ is chosen such that $\|(\mathbf{I}-\mu\mathbf{R_{hh}})\|_2 < 1$, it follows that the parameter estimation converges on average toward the MMSE solution.

B. Stability

As the convergence proof above requires statistical knowledge of $\Delta\mathbf{h}[k]$, it is more of a theoretical statement. To obtain practical boundaries on the step-size, an alternative way is pursued in the following. Subtracting the MMSE solution from both sides of (11), and denoting $\mathbf{e}[k] = \boldsymbol{\theta}[k] - \boldsymbol{\theta}_0$, allows rewriting (11) as

$$\begin{aligned}\mathbf{e}[k] = \ & \mathbf{e}[k-1] \\ & - \mu\Delta\mathbf{h}[k]\big(\Delta y[k] + \Delta\mathbf{h}^T[k](\mathbf{e}[k-1]+\boldsymbol{\theta}_0)\big). \quad (14)\end{aligned}$$

With $\boldsymbol{\Lambda}[k] = (\mathbf{I} - \mu\Delta\mathbf{h}[k]\Delta\mathbf{h}^T[k])$, and $\Delta\epsilon[k] = \Delta y[k] + \Delta\mathbf{h}^T\boldsymbol{\theta}_0$, the equation above may be written as

$$\mathbf{e}[k] = \boldsymbol{\Lambda}[k]\mathbf{e}[k-1] - \mu\Delta\mathbf{h}[k]\Delta\epsilon[k]. \quad (15)$$

The term $\Delta\epsilon[k]$ denotes errors not covered by the MMSE solution, i.e., nonidealities in stages not considered for calibration, as well as the ADC quantization noise. In (15) this error is weighted by the step-size μ, by means that although $\Delta\epsilon[k]$ cannot be eliminated, its impact may be reduced by choosing a smaller step-size. Inspecting (15) reveals that stability is achieved for $\|\boldsymbol{\Lambda}[k]\|_2 < 1$. This yields the deterministic step-size boundaries

$$0 < \mu < \frac{2}{\max\limits_k \|\Delta\mathbf{h}[k]\|_2^2}. \quad (16)$$

Fortunately, as shown above $\Delta\mathbf{h}[k]$ originates from the selection vectors according to $\Delta\mathbf{h}[k] = \mathbf{h}_{\alpha x}[k] - \alpha\mathbf{h}_x[k]$. Moreover, if the post correction model is employed in a way, that no entries of $\mathbf{h}_x[k]$ are replaced with z_k, as discussed in Section III, the maximum number of ones in these selection vectors corresponds to the number of considered stages q. Thus, $\Delta\mathbf{h}[k]$ contains q elements with value 1 and q elements with value α. Based on that, the step-size boundaries may be written as

$$0 < \mu < \frac{2}{(1+\alpha^2)q}. \quad (17)$$

Nevertheless, if the post correction model is extended by replacing q entries with z_k, the values of these q entries depend on the unknown ADC nonideality. Consequently, for this case, the step-size boundaries cannot be derived a priori as in (17).

C. Practical Aspects

As discussed at the beginning of this section, the input samples $x_{\text{in}}[k]$ may originate from a dedicated test SG or the SA stored in an S&H block. The latter one has the advantage that the application is not interrupted for calibration. On the downside, storing each sample in an S&H block and feeding it into the ADC twice reduces the effective sampling rate of the ADC by a factor of two. Another drawback might be that the application signal does not necessarily cover the full ADC transition function, such that only a part of it will be calibrated. Hence, the applicability of using the HEC approach with the SA signal depends on the application. By using a test SG and a dedicated calibration time slot, these drawbacks can easily be overcome. To achieve the full potential of the HEC approach, the authors suggest a two-phase calibration. In the initial phase, after the power-on of the device, an SG is used as the test signal source. Within this phase a full scale test signal is injected, such that the entire ADC transition function is calibrated. After the initial calibration, the signal source is switched to the SA. With this second phase, the nonidealities are tracked continuously without repeatedly interrupting the ADC sampling task. To track slowly changing nonidealities, it is not necessary to use each sample for calibration. Moreover, depending on how rapidly the nonidealities are changing, holding every m-th sample with the S&H block and utilizing these samples for calibration may be sufficient. Therefore, the impact of the S&H block regarding ADC bandwidth can be reduced as well. Note that this increases the required calibration time by a factor of m but does not impact the achievable calibration accuracy.

Furthermore, to omit additional digital hardware caused by different estimation algorithms in the two phases, the ALS algorithm [20] may be utilized for the initial calibration. Then both estimators support the same architecture, except for the memory used in the first phase. Additionally, many signal processing systems include a micro controller unit (MCU) after the ADC. In this case, the proposed calibration technique supports an implementation of the update equation (11) on the MCU, eliminating the need for a hardware implementation of (11). However, simulations have shown, that to achieve results as presented in the following section, the implementation of (11) requires a minimum number of 12 bits.

V. Simulation Results

The calibration performance of the HEC approach is demonstrated with behavioral MATLAB simulations in this section. We consider a 13 Bit pipelined ADC with six stages and a sampling rate of 100 MHz. The stages 1-5 are implemented as 2.5 Bit stages, while the final flash ADC resolves 3 Bits. Regarding nonidealities, the first five stages suffer from gain and DAC mismatches. All gain and DAC mismatches were chosen from a uniform probability density function (PDF). This uniform PDF was designed such that in the worst case the first stage gain and DAC mismatches contribute to the overall ADC nonideality with ± 25 LSBs and ± 15 LSBs, respectively. Note that, mismatches corresponding to less significant stages are weighted appropriately. Additionally, $\alpha = 0.5$ is chosen as the scaling factor.

The HEC approach employed in this simulation covers the three most significant stages, which results in 19 parameters to be estimated. A full scale sine wave at 10.77 MHz was injected as the test signal. Fig. 4 shows the error norm $\|\boldsymbol{\theta}[k] - \boldsymbol{\theta}_0\|_2$ for different step-sizes μ. As can be observed, the error reduces significantly for smaller step-sizes. This reduction results from the fact, that the step-size dependent error term $\Delta\epsilon[k]$ becomes smaller. Nonetheless, smaller step-sizes obviously cause longer calibration times. As a compromise of these two aspects, $\mu = 0.2$ is chosen for all further simulations. With this

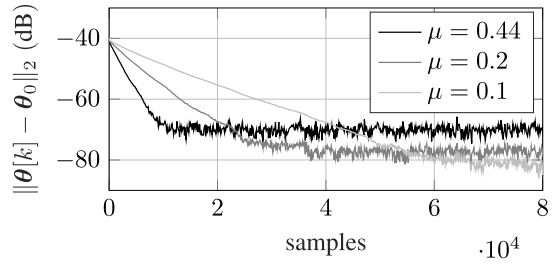

Fig. 4. Error norm with respect to different step-sizes.

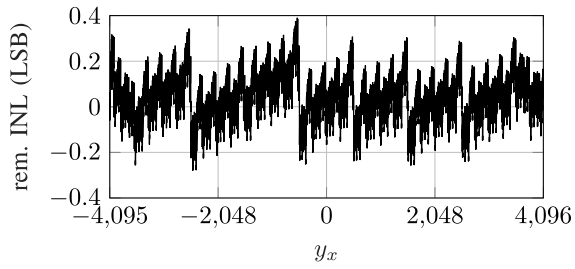

Fig. 5. Remaining INL after calibration.

TABLE I
COMPARISON WITH OTHER CALIBRATION TECHNIQUES

Ref.	[5]	[7]	[17]	This work
Add. analog circuit	none	moderate	low	low
Add. digital hardware	low	low	low	low
Required samples for calibration	$1 \cdot 10^6$	$5 \cdot 10^6$	$5 \cdot 10^4$	$3 \cdot 10^4$
SFDR (dB)	75.8	82.3	83	95.5
SFDR improvement (dB)	40.8	25.5	41	43
SNDR improvement (dB)	34.1	21	28	28
INL (LSB)	-	<1	2.2	<0.4
Resolution (bits)	12	12	12	13

step-size a full calibration is achieved after $3 \cdot 10^4$ samples. Considering a sampling frequency of 100 MHz this yields a calibration time of 300 μs. The calibration performance is verified in Fig. 5 regarding the remaining INL of the ADC. The INL can be derived by subtracting the input signal x_{in} and the quantization error $e^{\text{q}}_{\text{s,F}} \prod_{i=1}^{n} \frac{1}{G_i}$ from (7), and is plotted over the ADC output. It can be observed that the HEC approach achieves a remaining error of less than 0.4 LSBs. A comparison to other calibration techniques and additional performance characteristics, i.e., SFDR, and signal to noise and distortion ratio (SNDR) are provided in Table I.

VI. CONCLUSION

In this brief, an equalization-based calibration technique for pipelined ADCs, denoted as the HEC approach, was proposed. The HEC approach allows for different test signal sources, such as a test SG, or the SA signal itself. In the latter case, the HEC approach corresponds to a background calibration technique. Ultimately, simulation results of the proposed calibration technique were compared to prior work which show faster calibration times, lower INL after calibration and an improved SFDR.

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