A G_m-Boosting Technique for Millimeter-Wave Low-Noise Amplifiers in 28-nm Triple-Well Bulk CMOS Using Floating Resistor in Body Biasing

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***Abstract*—This paper presents a simple yet effective G_m-boosting technique for improving gain and noise performance of millimeter-wave (mm-wave) low-noise amplifiers (LNAs) comprising triple-well transistors typically found in the modern bulk CMOS processes. The proposed technique uses a resistor that connects the p-well and deep n-well terminals of the triple-well transistor, leaving the terminals floating instead of conventionally connecting them to the ground and supply voltage. This arrangement exploits a leakage current through a diode formed between the drain/source and p-well of each transistor, thus autonomously setting its bulk potential for increased transconductance, while ensuring its robustness to the process variation. The improved isolation between the p-well and the substrate further improves the gain and noise performance. We provide a theoretical analysis of this floating resistor-based body biasing method and support it with simulation results. For experimental validation, a two-stage cascode LNA was designed and fabricated in 28-nm bulk CMOS. The measurement results show that 3.3–4 dB noise figure (NF) and 19.1–16.1 dB gain are achieved at 24.7–29.5 GHz. To ensure a fair comparison, another identical LNA with the normally expected triple-well biasing was also fabricated. The proposed method reveals a 0.6 dB improvement in minimum NF and an additional ∼3.5 dB gain without any significant linearity degradation.**

***Index Terms*—5G, floating resistor, G_m-boosting, low-noise amplifier (LNA), millimeter-wave, noise reduction.**

I. Introduction

To meet the demand for higher data rates and larger system capacities of wireless communications, the fifth generation (5G) systems are moving towards millimeter-wave (mm-wave) frequencies [1]. As carrier frequencies increase, it becomes more difficult to maintain the noise performance of a low noise amplifier (LNA), which is the key receiver block, as the minimum noise figure (NF) of a single MOS device is proportional to its operating frequency [2].

Different noise cancellation techniques have been proposed in the literature to reduce NF. Among them, the differential topology has been widely adopted as it can eliminate the effects of common-mode noise sources and provide better isolation to the noise coupling from the supply [3], [4], [5]. However, that approach requires a balun to convert a single-ended signal to a differential signal, but baluns tend to occupy a considerably large area compared to active devices. Yet another technique is based on boosting the equivalent transconductance of the circuit (G_m) [6], [7], [8], [9], [10]. G_m-boosting can be achieved by using three different schemes. First, an auxiliary amplifier is inserted between the source and gate of the common-gate transistor to apply a negative voltage gain to the gate. However, the auxiliary amplifier causes additional dc power and noise, especially at mm-wave frequencies. Therefore, instead of using an auxiliary amplifier, passive devices, such as capacitors or transformers, can be adopted [6]. Using a pair of cross-coupled capacitors is another option but it is only possible in a differential topology [9]. The third scheme is based on magnetic coupling using a transformer [10]. Just as baluns, however, transformers are also area-inefficient. Alongside the conventional approaches, some new noise canceling techniques have also been proposed [11], [12]. While these technique can be very effective at RF frequencies, their performance is limited by the degraded quality factor of the lumped components at mm-wave.

Recently, there has been a growing interest in exploiting triple-well transistor structures of bulk CMOS for performance improvements in a variety of applications. For instance, a self-biasing arrangement was introduced in [13], where the p-well is connected to the transistor's gate to increase the capacitance density of the pumping capacitor with the beneficial use of the parasitic capacitance for a dc-dc converter. Furthermore, [14] employs a dynamic body biasing to improve performance of a power amplifier. In [15] and [16], a large resistor was added between the bulk and substrate (ground) nodes to improve the

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isolation. That method aimed to increase the maximum gain of the transistor at high frequencies without boosting G_m.

In this paper, we propose a new G_m-boosting technique for a mm-wave cascode LNA, leveraging characteristics of triple-well bulk transistors by introducing a resistor between the p-well and deep n-well (DNW) terminals and leaving them floating instead of customarily tying them to ground or supply. Compared to other classical body-biasing approaches [14], [17], [18], this technique provides an autonomous body biasing with the leakage diode current between drain/source and the p-well, resulting in an improved G_m. In addition, it offers a large impedance between the p-well and the substrate, which improves the isolation across the chip. In this regard, [15] and [16] also aim particularly to have high isolation between these two nodes, however, these works do not include G_m-boosting for further performance improvement. Moreover, unlike the conventional methods discussed in [3], [4], [5], [6], [7], [8], [9], and [10], the proposed technique does not require an additional chip area. Furthermore, contrary to the solutions in [11] and [12], it is not affected by the degraded quality factor of the lumped components at mm-wave. In fact, even better gain and noise performance can be achieved with increasing frequency. As a proof-of-concept, a two-stage cascode LNA using the proposed technique and another LNA with the same structure but using the conventional triple-well biasing were implemented in TSMC 28-nm LP CMOS technology for fair comparison. The measurement results show that the proposed technique achieves a 0.6 dB improvement in the minimum NF and approximately 3.5 dB additional gain at an extra cost of ~5 mW in power consumption, from 20.3 mW to 25.5 mW, while maintaining its linearity performance between 24.7–29.5 GHz.

The rest of the paper is organized as follows. In Section II, the analysis of the proposed floating resistor technique is applied in a cascode structure to compare its effectiveness for G_m-boosting. Section III details the circuit implementation and optimization techniques for mm-wave amplifiers. The measurement results are shown in Section IV and conclusions are drawn in Section V.

II. Proposed G_m-Boosting Technique Using a Floating Resistor

This section presents a detailed explanation of the concept of G_m-boosting using a floating resistor in the body biasing. First, it will be shown how this method leads to an increase in transconductance of a single transistor. Then, the application of this technique in a cascode structure will be explored by providing the gain and noise analysis of both the conventional biasing of triple-well bulk CMOS transistors and the proposed scheme using a floating resistor.

A. G_m Boosting With Floating Resistor

Transconductance g_m of a single transistor can be represented as [19]:

$$g_m = \mu_n C_{\text{ox}} \frac{W}{L} \left(V_{\text{gs}} - V_{\text{th}} \right), \tag{1}$$

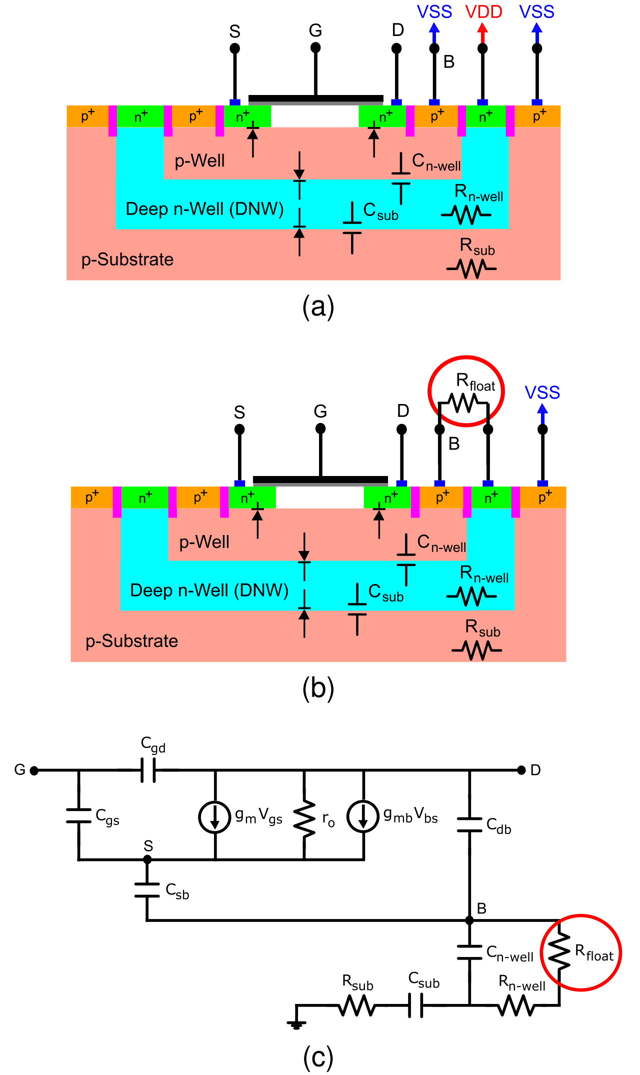

Fig. 1. (a) Cross-section diagram of the conventional biasing of triple-well NMOS transistor structure, (b) cross-section diagram, and (c) small-signal circuit model of the proposed biasing with the floating resistor between the triple-well NMOS device layers.

where μ_n denotes the electron mobility, and C_{ox} represents the gate oxide capacitance per unit area. W and L are the width and length of the transistor, respectively. Threshold voltage V_{th} can be calculated from $\phi_{\text{MS}} + 2\phi_{\text{F}} + Q_{\text{dep}}/C_{\text{ox}}$, where ϕ_{MS} defines the difference between the work functions of polysilicon gate and silicon substrate, while ϕ_{F} and Q_{dep} represent the substrate doping effect and the charge in the depletion region, respectively. As governed by (1), g_m can only be readily controlled at run-time by V_{gs} or V_{th}.

Fig. 1(a) and (b) show the cross-section diagrams of a triple-well NMOS transistor structure with the conventional and proposed biasing techniques. Conventionally, the p-well is connected to ground ($V_{\text{B}} = 0$) so as to avoid the body effect, i.e. the back-gate effect, as shown in Fig. 1(a). Fig. 2 indicates the effect of the back-gate biasing on the transistor's V_{th} and on its leakage diode current between the source and p-well (i_{SB}). Here, the back gate voltage V_{B} is applied to node B, while DNW is connected to V_{DD}. Normally, a non-positive V_{B} should be used to prevent the diode from

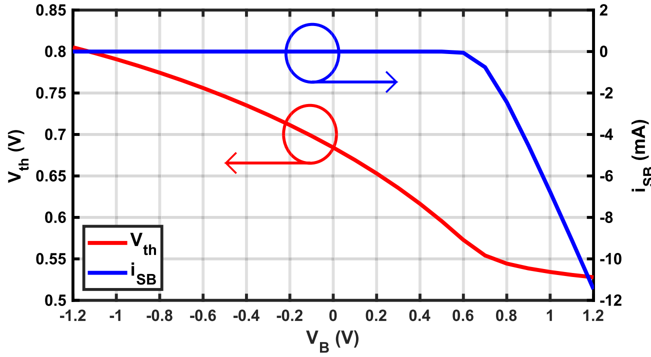

Fig. 2. Back-gate V_B effect on V_{th} and the leakage diode current between the source and p-well of triple-well NMOS transistor structure.

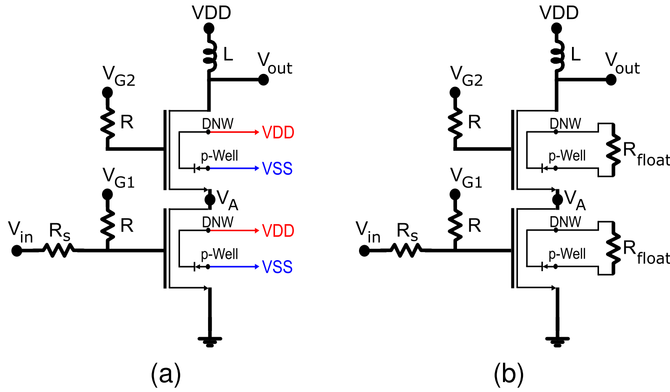

Fig. 3. Schematic representations of a cascode (a) with the conventional biasing, and (b) with the proposed floating resistor biasing of the triple-well nodes.

turning on and thus a possible device break-down. However, in some applications, positive V_{B} up to the diode's turn-on voltage can also be applied [14]. As an alternative approach, in the proposed technique shown in Fig. 1(b), the p-well and DNW are connected via a high-valued resistor R_{float} and left floating rather than connected to ground or voltage source. This configuration can effectively increase the voltage at the two nodes due to diode leakage, resulting in a reduction of ϕ_{MS} and hence a decrease in V_{th}. Consequently, g_m of the transistor will be increased.

Compared to other conventional body biasing approaches in [17], [18], and [14], our proposed technique, that take advantage of the leakage diode currents between the drain/source and the p-well, provides a dynamic body biasing to the transistors by autonomously establishing V_{B} as 0.2 V without any additional chip area or control circuitry. Furthermore, the fact that the p-well and DNW are connected through R_{float}, it ensures that the diode between these two wells is always OFF since the voltage at DNW also settles at 0.2 V. It is worth mentioning that to achieve the same performance with the conventional back-gate biasing, approximately 0.5 V must be applied to node B. That is not practical, since it is very close to the diode turn-on voltage.

B. Analysis of Cascode Transistor Case

Fig. 3 illustrates the schematics of cascode designs with two different body biasing schemes. Fig. 3(a) depicts the conventional biasing, while the structure of the proposed floating resistor biasing is shown in Fig. 3(b). In these figures, L and R are high-valued inductance and resistance for biasing purpose only and R_s denotes the source resistance. The common substrate is connected to ground. To verify the G_m-boosting capability of the proposed technique, Table I presents the simulated g_{m} and V_{th} of CS and CG transistors in an example cascode structure with transistor dimensions of $2\times 38.4\,\mu$m/30 nm. The comparison in Table I indicates that the proposed method results in lower V_{th}, thus ultimately higher g_{m}, for both transistors. Still, it should be noted that V_{th} of the CG transistor decreases more than that of the CS transistor, i.e., the proposed floating resistor technique is more efficient for the CG transistor in the cascode.

TABLE I

TRANSCONDUCTANCE g_{m} AND THRESHOLD VOLTAGE V_{th} OF THE CS AND THE CG TRANSISTORS OF A CASCODE STRUCTURE FOR DIFFERENT WELL BIASING CASES

	Conventional Biasing		**Floating Resistor**	
	g_{m} **(S)**	V_{th} **(mV)**	g_{m} **(S)**	V_{th} **(mV)**
CS	25.05	722.7	29.74	685.1
CG	26.17	736.4	30.72	654.8

Building upon Figs. 1(c) and 3, Fig. 4 presents a small-signal equivalent circuit for the cascode structure, including the noise sources, where Z_{eq} represents the equivalent impedance seen at the drain of the CS transistor including all parasitics, and $Z_{\text{eq2}} = Z_{\text{eq}}||C_{\text{gd}}$ is at the drain of the CG transistor. The derivation of Z_{eq} can be found in Appendix. To analyze the voltage gain of the cascode amplifier for the cases with the proposed floating resistor ("float") and the conventional biasing ("conv"), the voltage noise source in Fig. 4 can be short-circuited whereas the current noise sources can be open-circuited while applying the Kirchoff's Current Law (KCL) to the simplified circuit. For the sake of simplicity, it is assumed that $\lim_{R_{\text{float}}\to\infty}$, $g_m r_o \gg 1$, $(g_m + g_{mb})\, r_o \gg 1$, $C_{\text{db}} \approx C_{\text{sb}}$ and $C_{\text{gd}} \approx C_{\text{gs}}$. The derived voltage gain equations include all the parasitics; hence, they are too long. By further simplification, the following equations can be obtained for the voltage gain of the two cases:

$$\left|A_{v,\text{float}}\right| \approx \frac{A}{B} \tag{2}$$

where

$$\begin{cases} A = 4\left(g_{\text{m,float}} + g_{\text{mb,float}}\right)\left(\omega^2 C_{\text{gd}}^2 + g_{\text{m,float}}^2\right)^{1/2} \\ B = \left(\omega^2\left(C_{\text{db}}^2 + 4\ C_{\text{db}}C_{\text{gd}} + 4\ C_{\text{gd}}^2\right) + g_{\text{mb,float}}^2\right)^{1/2} \\ \Big(\omega^2 R_s^2(72\omega^2 C_{\text{db}}C_{\text{gd}}^3 + 36\omega^2 C_{\text{gd}}^4 + 4\ C_{\text{gd}}^2 g_{\text{m,float}} \\ +8\ C_{\text{gd}}^2 g_{\text{m,float}} g_{\text{mb,float}} + 4\ C_{\text{gd}}^2 g_{\text{mb,float}}^2) + g_{\text{mb,float}}^2\Big)^{1/2} \end{cases} \tag{3}$$

$$\left|A_{v,\text{conv}}\right| \approx \frac{C}{D} \tag{4}$$

where

$$\begin{cases} C = \left(g_{\text{m,conv}} + g_{\text{mb,conv}}\right)\left(\omega^2 C_{\text{gd}}^2 + g_{\text{m,conv}}^2\right)^{1/2} \\ D = 2\omega R_s C_{\text{gd}}\left(\omega^2 r_{\text{o,conv}}^2 (C_{\text{db}} + C_{gd})^2 + 1\right)^{1/2} \\ \left(2\omega^2 C_{\text{db}}\left(2\ C_{\text{db}} + 3\ C_{\text{gd}}\right) + g_{\text{m,conv}}\right)^{1/2} \end{cases} \tag{5}$$

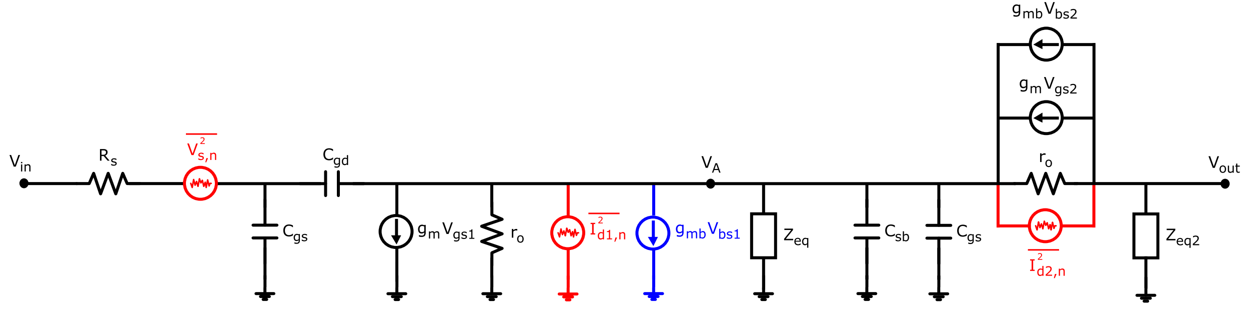

Fig. 4. Simplified circuit representation of a cascode amplifier used for gain and noise calculations. The blue current source is only available in *with* the floating resistor case and the red sources are the noise sources.

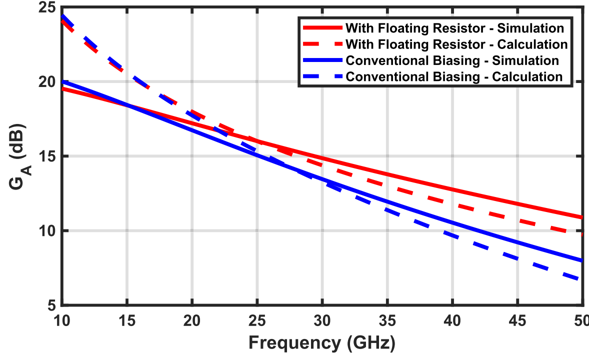

Fig. 5. Available gain of a cascode amplifier for the case with the floating resistor and the reference case with the conventional biasing. Note that due to the simplifications in deriving (2) and (4), they do not reflect well the parasitics at lower frequencies that are of less interest in this work.

To verify these simplified equations, Fig. 5 compares them with circuit-level simulations. As evident, the proposed technique provides a slightly lower gain than in the conventional case at lower carrier frequencies, but at higher frequencies it consistently offers a significant improvement. This analysis confirms that the gain advantage becomes more distinct at frequencies beyond 20 GHz. To evaluate the maximum available gain advantage, the ratio between the voltage gain equation of the case with the floating resistor, $A_{v,\text{float}}$, and that of the reference case with the conventional biasing, $A_{v,conv}$, is investigated as ($\lim_{\omega\to\infty}$):

$$\lim_{\omega\to\infty}\left|\frac{A_{v,\text{float}}}{A_{v,conv}}\right| \approx \frac{E}{2\left(g_{m,\text{conv}}+g_{mb,\text{conv}}\right)\left(R_n+R_{\text{sub}}\right)} \quad (6)$$

where

$$E = 3\left(g_{m,\text{float}}+g_{mb,\text{float}}\right)\left[\left(R_n+R_{\text{sub}}\right)\left(2C_{\text{gd}}+C_{\text{db}}\right) + C_{\text{db}}R_nR_{\text{sub}}g_{\text{mb,conv}}\right] \quad (7)$$

In case where there is no G_{m}-boosting, i.e. $g_{\text{m,float}}=g_{\text{m,conv}}$ and $g_{\text{mb,float}}=g_{\text{mb,conv}}$, (6) can be simplified to

$$\lim_{\omega\to\infty}\left|\frac{A_{v,\text{float}}}{A_{v,conv}}\right| \approx \frac{G}{2\left(R_n+R_{\text{sub}}\right)} > 1, \quad (8)$$

where

$$G = 3\left[\left(R_n+R_{\text{sub}}\right)\left(2C_{\text{gd}}+C_{\text{db}}\right)+C_{\text{db}}R_nR_{\text{sub}}g_{\text{mb,conv}}\right]. \quad (9)$$

As seen from (8), in the absence of G_m-boosting, the proposed technique still provides a gain improvement due to the improved isolation between the p-well and the substrate. However, the increased G_m introduced by the proposed method further increases the available gain.

To examine the noise of the cascode under a narrow-band condition, the noise factor with respect to R_s for the simplified circuit shown in Fig. 4 can be derived as

$$F = 1 + F_{\text{M1}}, \quad (10)$$

where $F_{\text{M1}} = \left(\overline{I^2_{d1,n}}|Z_1|^2\right)/\left(\overline{V^2_{s,n}}|A_v|^2\right)$, $\overline{V^2_{s,n}}$ describes the source-resistance noise, while $\overline{I^2_{d,n}}$ is the channel thermal noise and Z_1 denotes the impedance seen at the upper terminal of the noise source of $\overline{I^2_{d1,n}}$ shown in Fig. 4. Note that the impact of the cascode transistor on the noise factor is ignored, since the noise power contribution of the cascode transistor should be divided by the square of the voltage gain of the input transistor, which eventually becomes negligible in deep-submicron CMOS [20]. Similar to the gain analysis, separate equations for noise factor of both cases that include all parasitics can be derived and further simplified by assuming that $\lim_{R_{\text{float}}\to\infty}$, $g_mr_o \gg 1$, $(g_m+g_{mb})\,r_o \gg 1$, $C_{\text{db}} \approx C_{\text{sb}}$ and $C_{\text{gd}} \approx C_{\text{gs}}$ as follows

$$|F_{\text{float}}| \approx 1 + \frac{H}{I} \quad (11)$$

where

$$\begin{cases} H = \gamma\, g_{\text{m,float}}\omega^2C^2_{\text{gd}}R_s\left(\omega^2r^2_{o,with}\left(C_{\text{db}}+C_{\text{gd}}\right)^2 + g^2_{\text{mb,float}}r^2_{\text{o,float}}\right)^2\left(36\omega^4R^2_sr^2_{\text{o,float}}(C^2_{\text{db}}C^2_{\text{gd}}+2\ C_{\text{db}}C^3_{\text{gd}} + C^4_{\text{gd}}) + g^2_{\text{mb,float}}r^2_{\text{o,float}}\right) \\ I = r^2_{\text{o,float}}\left(\omega^2C^2_{\text{gd}}+g^2_{\text{m,float}}\right)\left(g_{\text{m,float}}+g_{\text{mb,float}}\right)^2\left(6\omega^6R^2_sr^4_{\text{o,float}}C^2_{\text{gd}}(6C^4_{\text{db}}+36C^3_{\text{db}}C_{\text{gd}}+13C^2_{\text{db}}C^2_{\text{gd}} + 12C_{\text{db}}C^3_{\text{gd}}+4C^4_{\text{gd}}) + g^4_{\text{mb,float}}r^4_{\text{o,float}}\right) \end{cases} \quad (12)$$

$$|F_{\text{conv}}| \approx 1 + \frac{J}{K} \quad (13)$$

where

$$\begin{cases} J = 4\gamma\, g_{\text{m,conv}}\omega^2R_s\left(\omega^2r^2_{\text{o,conv}}\left(C_{\text{db}}+C_{\text{gd}}\right)^2+1\right)^2\left(\omega^4R^2_sr^2_{\text{o,conv}}\left(16C^2_{\text{db}}C^2_{\text{gd}}+24C_{\text{db}}C^3_{\text{gd}}+9\ C^4_{\text{gd}}\right)+1\right) \\ K = \omega^2r^2_{\text{o,conv}}\left(g_{\text{m,conv}}+g_{\text{mb,conv}}\right)^2\left(\omega^6R^2_sr^4_{\text{o,conv}}C^2_{\text{gd}}\left(16C^4_{\text{db}}+56C^3_{\text{db}}C_{\text{gd}}+73C^2_{\text{db}}C^2_{\text{gd}}+42C_{\text{db}}C^3_{\text{gd}}+9\ C^4_{\text{gd}}\right)+1\right) \end{cases} \quad (14)$$

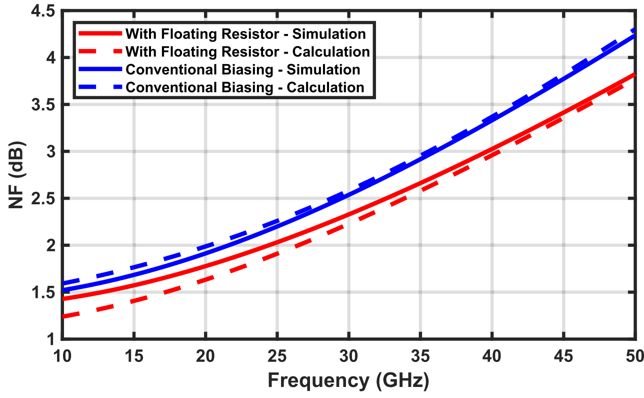

Fig. 6. NF of a cascode amplifier for the case with the floating resistor and the reference case with the conventional biasing. Similar to Fig. 5, due to the simplifications in deriving (11) and (13), they do not reflect well the parasitics at lower frequencies that are of less interest in this work.

Likewise, to validate the simplified noise equations, Fig. 6 compares the simulated and calculated NFs of the cascode amplifier for the two biasing cases. As revealed in Fig. 6, both have similar NFs at lower frequencies. However, at mm-wave frequencies, the proposed technique consistently offers a greater advantage in noise performance.

III. Circuit Description

In this section, the circuit implementation of the LNA is discussed in detail. Apart from the impedance matching networks, there are mainly three important parameters that need to be carefully set for this design: the transistor size, its multiplier setting, and the value of the floating resistor R_{float} between the DNW and p-well.

A. Device Size Selection

To find the optimal transistor size, a suite of simulations were conducted in Cadence for a triple-well transistor. Fig. 7(a) shows the schematic and the expected minimum NF for different transistor sizes across the frequency. Likewise, subplot (b) depicts the available gain, G_A, for different transistor sizes. As expected, G_A increases with the transistor width. However, this is not the case for the minimum NF. Even for the same transistor width, different combinations of finger width and number of fingers can lead to a different minimum NF. This is mainly due to the parasitic capacitors, the effects of which are more pronounced at higher frequencies. The minimum NF of a single-stage transistor in the common-source configuration should be as follows [21]:

$$\text{NF}_{\min} = 10\log\left(1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\,\delta\left(1-|c|^2\right)}\right) \qquad (15)$$

where, $\omega_T = g_m/(C_{\text{gs}}+C_{\text{gd}})$ defines the unity-gain frequency, γ is a bias-dependent factor and δ denotes the induced gate noise coefficient, while c represents the correlation coefficient between the gate noise and drain noise. Even though the overall transistor width can be identically constrained for different finger widths and the number of finger pairs, it may result in different C_{gs} and C_{gd} due to the additional parasitic capacitors. As implied by (15), the variance in C_{gs} or C_{gd} can directly affect the minimum NF. According to the simulation results in Fig. 7, $W = 20.8\,\mu$m (0.8μm$\times$26) provides the lowest $\text{NF}_{\min}$ with an acceptable available gain. However, if the transistor width is increased to $38.4\,\mu$m (1.2μm$\times$32), the available gain can be increased significantly with a slight increase in the minimum NF. As a result, $W = 38.4\,\mu$m (1.2μm$\times$32) was chosen in this design.

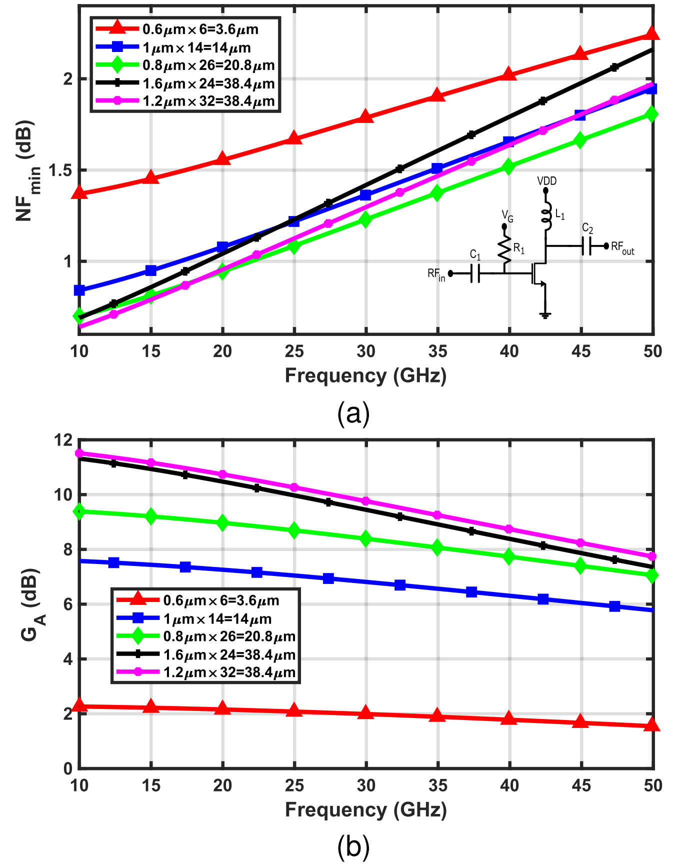

Fig. 7. Simulated (a) minimum NF across frequency and (b) available gain across frequency for different transistor sizes.

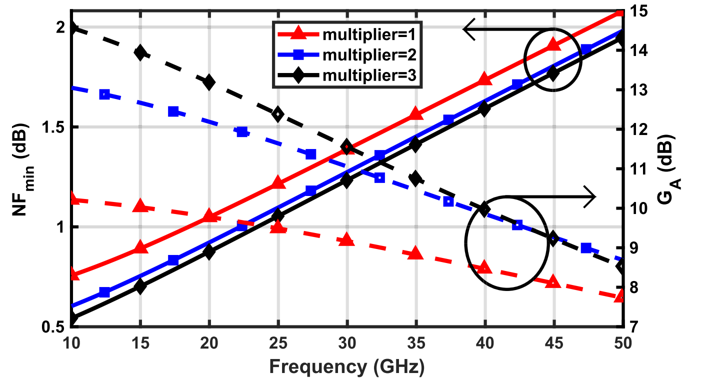

Fig. 8. Minimum NF and available gain for a sample transistor in a common-source configuration with different multiplier constants.

B. Transistor Multiplier Setting

Fig. 8 shows the simulated minimum NF and the available gain of the CS transistor with different transistor multipliers. During the simulations, an ideal connection was assumed

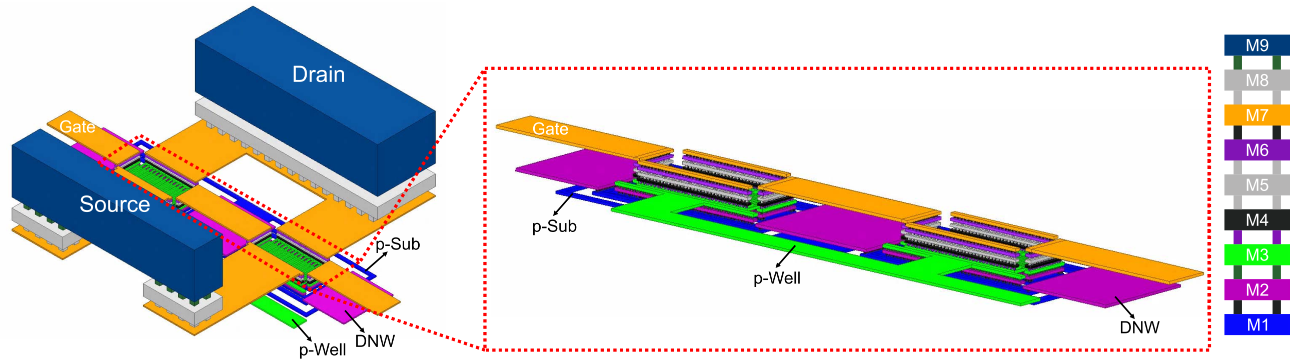

Fig. 9. Layout of two transistors connected in parallel.

between the unit transistors. In this regard, [22] states that more multi-finger devices connected in parallel would provide a lower noise level up to 30 GHz than would a single device. However, as seen in Fig. 8, this improvement in NF cannot be firmly observed after 30 GHz when the multiplier is increased from 2 to 3. This slight improvement will disappear altogether when the additional parasitics from the layout are taken into consideration. Furthermore, at higher frequencies, the available gains for the multiplier values of 2 and 3 are nearly the same. Thus, the multiplier of each transistor was set to 2 in this design. The layout of one of the transistor sets used in the design is presented in Fig. 9. For the connection of the DNW and p-well terminals of the transistors, the lowest available metals were used to provide the additional resistance, since the conductivity of the lower level metals is very small.

C. Resistor Value Selection

As stated earlier, the proposed technique in this paper introduces a resistor, R_{float}, connected between the p-well and the DNW terminals of a triple-well transistor, leaving them floating instead of conventionally connecting them to the ground and V_{DD}, respectively. To find the optimum resistance of R_{float}, the NF and the available gain of the designed cascode, including the layout related parasitics, at 28 GHz were simulated across R_{float}, as shown in Fig. 10. At this point, it should be clarified that $R_{\text{float}} = 0$ in Fig. 10 does not refer to the conventional biasing method where there is no R_{float} resistor at all. This particular configuration of $R_{\text{float}} = 0$ defines a short circuit between the p-well and the DNW. The simulations reveal that both the gain and noise performance do not change much after the resistance value exceeds 10 kΩ. A higher resistance can be beneficial for an ESD protection, but considering the area limitation, R_{float} was set to 18 kΩ.

D. Complete LNA Design

After determining the optimal values of the transistor widths and R_{float}, the cascode design was completed. The LNA with the proposed biasing technique consists of 2 consecutive cascode designs as discussed earlier. Different from the second stage, the first stage has an additional inductor connected to the source of the cascode structure to improve the linearity of the design. The two stages are connected via a decoupling capacitor, which also functions as a part of the inter-stage matching network. In the final cascode design, an additional capacitor is connected to the gate of the CG transistor rather than providing a RF short to allow for a voltage swing on the gate proportional to the swing of the corresponding source. Fig. 11 illustrates the detailed schematic of the proposed two-stage cascode amplifier. An almost identical copy was also fabricated as a reference, but with the conventional biasing of the p-well and DNW instead of the floating resistor R_{float} between them, as contrasted in Fig. 1(a) and Fig. 1(b).

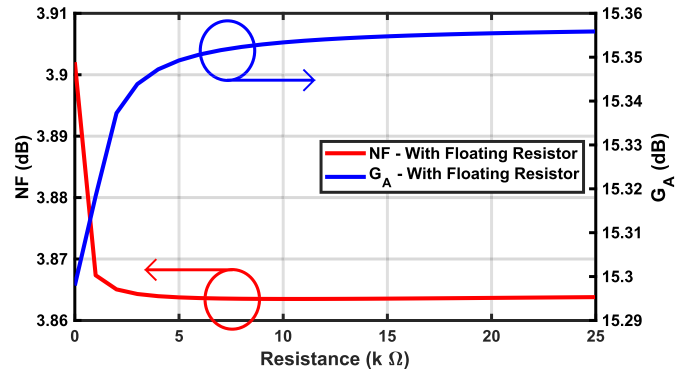

Fig. 10. Expected NF and available gain of a cascode at 28 GHz for different floating resistance values. For the conventional biasing case, NF and G_A equals to 4.38 dB and 14.17 dB, respectively.

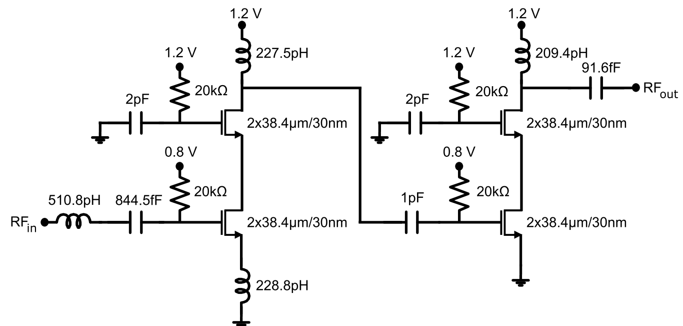

Fig. 11. Overall schematic of the proposed LNA. All four transistors are triple-well where a floating resistor is used between the DNW and p-well for the proposed LNA whereas normally expected voltages are provided to each well for the LNA with conventional biasing.

E. Process Variation Effect

To investigate the effect of process variation on noise and gain performance of the proposed LNA, simulations were

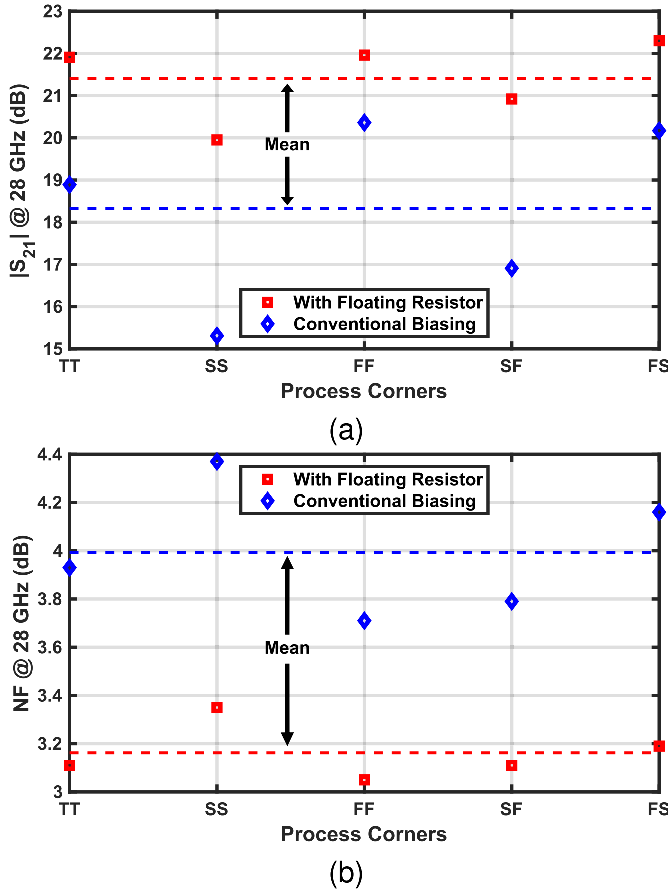

Fig. 12. Process variation effect on (a) $|S_{21}|$ and (b) NF for the cases with the floating resistor and the conventional biasing.

TABLE II

BULK VOLTAGES FOR THE CS AND THE CG TRANSISTOR OF THE CASCODE STRUCTURE WITH THE PROPOSED WELL-BIASING TECHNIQUE AT DIFFERENT PROCESS CORNERS

	TT	SS	FF	FS	SF
CS	171.5 mV	169 mV	174.6 mV	172.9 mV	170.1 mV
CG	674.4 mV	672.6 mV	678.8 mV	676 mV	673 mV

performed at different process corners. Fig. 12 shows the simulated $|S_{21}|$ and NF at 28 GHz for the cases with the floating resistor and the conventional well biasing at different process corners. As evident, the proposed design exhibits a much better robustness to process variations, in addition to improved noise and gain performance, thanks to the autonomous body biasing that changes the bulk voltage with the process variation, as can be seen in Table II.

IV. MEASUREMENT RESULTS

The proposed mm-wave LNA was fabricated in TSMC 28-nm LP CMOS process. Its chip micrograph is shown in Fig. 13. The reference case with the conventional well biasing was also fabricated for fair assessment of the performance improvements. The chips were measured using a Cascade Microtech Summit 9000 Analytical Probe Station and MPI T40A GSG-100 wafer probes. The design with the floating resistor consumes 25.5 mW power from a 1.2 V voltage supply, whereas the reference chip consumes 20.3 mW from the same voltage supply.

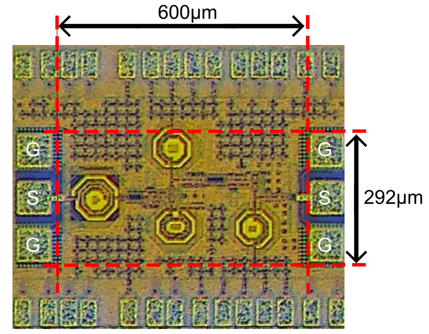

Fig. 13. Chip micrograph of the proposed LNA. The reference design with the conventional well biasing looks nearly identical.

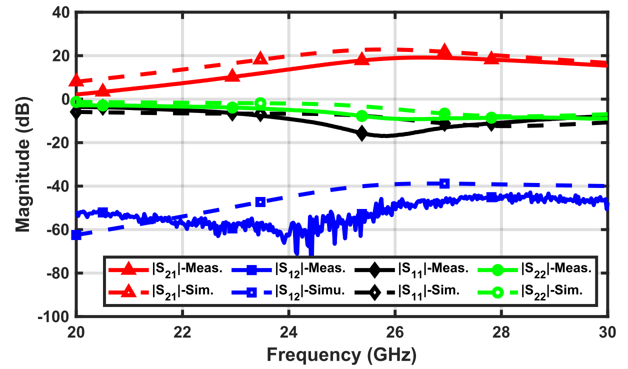

Fig. 14. Comparison of measured and simulated S-parameters of the proposed LNA.

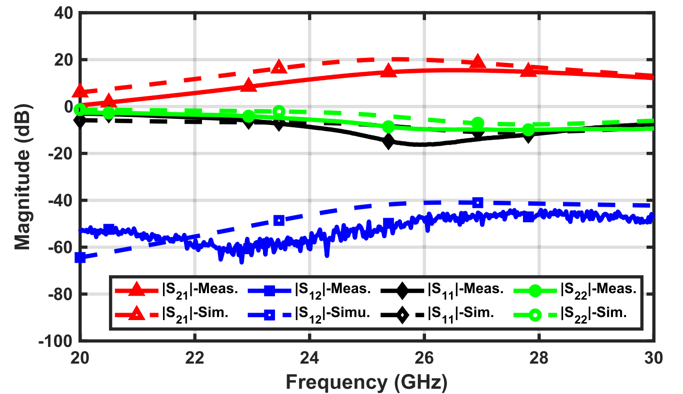

Fig. 15. Comparison of measured and simulated S-parameters of the reference LNA.

A. Small-Signal Measurement

S-parameters were measured with Agilent E8361A PNA, which was directly connected to the probes. On-wafer calibration was done with a AC-2 calibration substrate. Fig. 14 and Fig. 15 present a comparison between the measured and simulated S-parameters, while Fig. 16 compares the measured S_{21}. Based on these results, the LNA with the floating resistor can achieve a 19.1 dB maximum gain at 26.5 GHz while the reference LNA with the conventional well biasing can merely achieve a 15.5 dB maximum gain at the same frequency, thus offering a ~3.5 dB improvement in the maximum gain. Furthermore, the advantage in the gain becomes greater as the frequency increases. Moreover, the 3 dB bandwidth of the case with the floating resistor is 24.7–29.5 GHz while for the conventional biasing case it is 24.3–29.7 GHz.

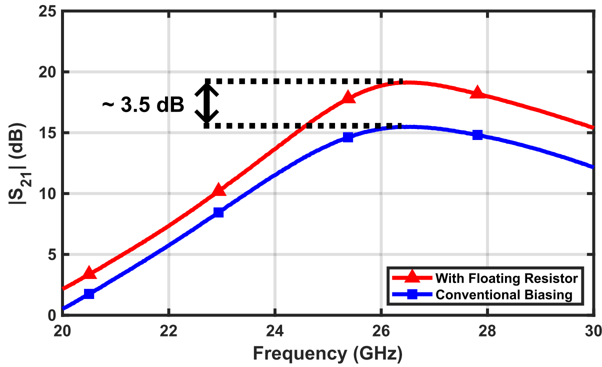

Fig. 16. Comparison of measured S_{21} of the implemented LNAs.

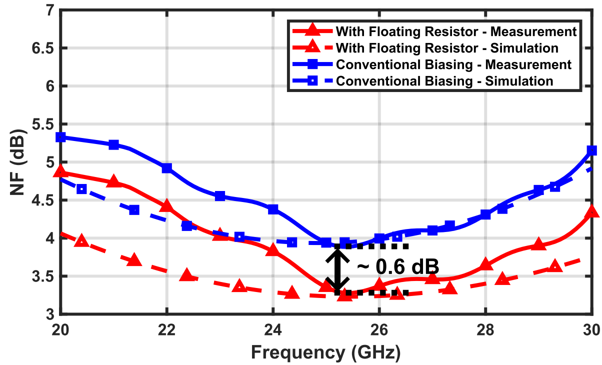

Fig. 17. Measured and simulated NF of the proposed and reference LNAs.

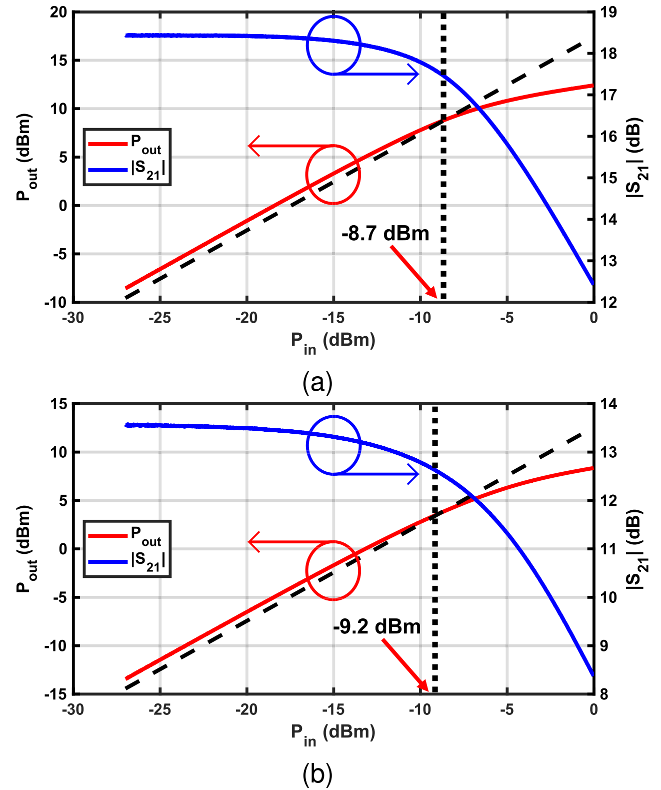

Fig. 18. P_{1dB} measurement at 28 GHz of the implemented LNAs: (a) proposed and (b) reference.

Regarding the return loss, the floating-resistor biasing and the conventional biasing outperform 10 dB between 24.4–28.55 GHz and 24.3–28.45 GHz, respectively. Consequently, the use of the proposed method does not significantly affect the 3-dB and matching bandwidths.

B. Noise Measurement

The NF of the fabricated chips were measured with a Y-factor method using R&S FSW50 spectrum analyzer and Keysight 346CK01 noise source. To reduce the measurement error, an additional LNA (HMC1040LP3CE) was used as a pre-amplifier before the spectrum analyzer. The measured and simulated NF can be found in Fig. 17. The minimum noise figure is 3.3 dB at 25.4 GHz and 3.9 dB at 25.3 GHz for the case with the floating resistor and the conventional biasing case, respectively. Thus, the proposed technique improves the NF by ~0.6 dB.

C. Linearity Measurement

For the input-referred 1-dB compression point (iP_{1dB}), the measurements were performed with the power sweep function of the Agilent E8361A PNA at 28 GHz. Fig. 18 shows the measured output power level and gain of the cases with the floating resistor and the conventional biasing at different input power levels. As plotted in this figure, at 28 GHz, iP_{1dB} was measured at −8.7 dBm and −9.2 dBm for LNA with the floating resistor and the reference LNA, respectively.

To characterize the LNA linearity, the input-referred third-order intercept point (IIP_3) was measured by applying two-tone signals with 100 MHz spacing at 28 GHz center frequency. The measured IIP_3 is −14.7 dBm for the implemented LNA with the floating resistor, whereas it is −14.2 dBm for the reference LNA with conventional biasing. The measurement results show that iP_{1dB} and IIP_3 exhibit a similar trend for both chips. Thus, it can be observed that the proposed technique does not affect the linearity of the design.

D. Performance Comparison

Table III summarizes the performance of the proposed and reference LNAs and compares them with state-of-the-art publications. The proposed technique offers approximately 3.5 dB improvement in the maximum gain. Although [18], [24], and [28] can offer a higher gain than the proposed design, they are in FDSOI CMOS and in III-V semiconductor technologies, which inherently yield better gain and noise performance compared to those in bulk CMOS. Similar reasoning applies to [24] and [18] for the NF performance. Thanks to the 0.6 dB improvement in the minimum NF, the proposed design achieves the lowest NF among the single-ended, 2-stage cascode LNAs in bulk CMOS, though the power consumption is increased by 5.2 mW, from 20.3 mW to 25.5 mW, which is due to the increase of the transconductance, G_m. Furthermore, it should be noted that the techniques introduced in [21], [24], [28], and [31] can be applied to the proposed design for bandwidth extension.

V. Conclusion

In this paper, a new G_m-boosting technique is presented for improving the noise and gain performance of a mm-wave

TABLE III

PERFORMANCE COMPARISON OF THE FABRICATED LNAS WITH THE STATE-OF-THE-ART

Reference	Technology	Topology	3 dB BW (GHz)	FBW (%)	Max. Gain (dB)	NF_{min} (dB)	IIP_3 (dBm)	iP_{1dB} (dBm)	VDD (V)	P_{dc} (mW)	Size (mm^2)	FoM_1 (GHz/mW)	FoM_{IP3} (GHz)
[23] JSSC'21	28-nm CMOS	Dual path noise cancelling	22.9–38.2	50.1	14.5	2.65	-12* @25 GHz	-2.5* @25 GHz	0.9	18.9	0.16	5.11	0.32
[21] TMTT'21	65-nm CMOS	1-stage cascode	7.2–27.3	116.5	16.6	3.3	-6 @20 GHz	-16* @20 GHz	1.2	13.2	0.14	9.05	2.27
[24] TCAS-I'20	0.13-μm SiGe	2-stage cascode	22–47	72.5	22.2	3	-13.8 @40 GHz	-23 @40 GHz	1.2	9.5	0.13	34.06	1.42
[25] TMTT'20	65-nm CMOS	2-stage CS, 1-stage cascode	24.4–32.3	27.9	24.4	4	Not reported	-23 @28 GHz	1.1	22	0.12	3.94	-
[18] TMTT'20	22-nm FDSOI CMOS	2-stage cascode	23–27	16	23.2	2.38	-10.4 @26 GHz	-21 @26 GHz	0.8	5.5	0.19	14.4	1.31
[26] MWCL'19	65-nm CMOS	2-stage cascode	29.2–33.1	12.5	20.8	3.71	Not reported	-20.4 @31 GHz	1.5	26.7	0.2	1.19	-
[27] RFIC'19	65-nm CMOS	1-stage diff. CS, 1-stage diff. cascode	24.9–32.5	26.5	18.33	3.25	Not reported	-24 @28 GHz	1.2	20.5	0.11	2.75	-
[28] MWCL'19	0.15-μm GaAs	3-stage cascode	0.1–52	199.2	22.5	3.9	2.5* @20 GHz	-7.5* @20 GHz	Not reported	396	1.42	1.20	2.14
[29] TCAS-II'18	28-nm LP CMOS	2-stage cascode	30.65–35.35	14.2	18.6	4.9	Not reported	-25.5 @33 GHz	1.2	9.7	0.23	1.97	-
[30] MWCL'18	40-nm CMOS	1-stage cascode, 2-stage diff. CS	26–33	23.7	27.1	3.3	-12.6* @27.1 GHz	-21.6 @27.1 GHz	1.1	31.4	0.26	4.44	0.24
[31] MWCL'17	65-nm CMOS	2-stage cascode	7.6–29	116.9	10.7	4.5	1.4 @21.5 GHz	Not reported	1	12.1	0.3	3.33	4.60
This work (float. resistor)	**28-nm LP CMOS**	**2-stage cascode**	**24.7–29.5**	**17.7**	**19.14**	**3.3**	**-14.7 @28 GHz**	**-8.7 @28 GHz**	**1.2**	**25.5**	**0.17**	**1.50**	**0.05**
This work (conv. biasing)	**28-nm LP CMOS**	**2-stage cascode**	**24.3–29.7**	**20**	**15.5**	**3.9**	**-14.2 @28 GHz**	**-9.2 @28 GHz**	**1.2**	**20.3**	**0.17**	**1.09**	**0.04**

* Estimated from plot. $\mathrm{FoM}_1 = \frac{\mathrm{Gain[abs.]}\times \mathrm{BW[GHz]}}{(F-1)\times P_{\mathrm{dc}}[mW]}$ $\mathrm{FoM}_{\mathrm{IP3}} = \frac{\mathrm{Gain[abs.]}\times \mathrm{BW[GHz]}\times \mathrm{IIP_3[mW]}}{(F-1)\times P_{\mathrm{dc}}[mW]}$

LNA. It introduces a dynamic body biasing of transistors in the triple-well device structures in bulk CMOS. To prove the efficacy, two nearly identical LNAs, one with the proposed floating resistor and the other with the conventional biasing, were designed and fabricated in TSMC 28-nm LP CMOS. The proposed LNA is more robust to process variation than the reference LNA, thanks to autonomous body-biasing which changes the bulk voltage with the process variation. The comparison of the measurement results, supported by the simulations and derived equations, indicates that the proposed technique provides an improvement in minimum NF and additional gain without obvious change in linearity.

APPENDIX
THE EQUIVALENT IMPEDANCE

The equivalent impedances, Z_{eq}, for the cases with the floating resistor (float) and with the conventional biasing (conv) can be derived as:

$$Z_{\mathrm{eq,float}} = \frac{X+Y}{j\omega C_{\mathrm{db}} Y}, \quad Z_{\mathrm{eq,conv}} = \frac{Q+Z}{j\omega C_{\mathrm{db}} Z} \tag{A.16}$$

where

$$\begin{cases} X = j\omega C_{\mathrm{db}} - \omega^2 C_{\mathrm{sub}} C_{\mathrm{db}} \left(R_{\mathrm{eq}} + R_{\mathrm{sub}}\right) \\ \quad - \omega^2 C_{\mathrm{n-well}} C_{\mathrm{db}} R_{\mathrm{eq}} - j\omega^3 C_{\mathrm{n-well}} C_{\mathrm{sub}} C_{\mathrm{db}} R_{\mathrm{eq}} R_{\mathrm{sub}} \\ Y = j\omega \left(C_{\mathrm{sub}} + C_{\mathrm{sb}}\right) - \omega^2 C_{\mathrm{sb}} C_{\mathrm{sub}} \left(R_{\mathrm{eq}} + R_{\mathrm{sub}}\right) \\ \quad - \omega^2 C_{\mathrm{n-well}} C_{\mathrm{sb}} R_{\mathrm{eq}} - \omega^2 C_{\mathrm{n-well}} C_{\mathrm{sub}} R_{\mathrm{eq}} \\ \quad - j\omega^3 C_{\mathrm{n-well}} C_{\mathrm{sb}} C_{\mathrm{sub}} R_{\mathrm{eq}} R_{\mathrm{sub}} \end{cases} \tag{A.17}$$

and

$$\begin{cases} Q = j\omega C_{\mathrm{db}} - \omega^2 C_{\mathrm{sub}} C_{\mathrm{db}} \left(R_{\mathrm{n-well}} + R_{\mathrm{sub}}\right) \\ \quad - \omega^2 C_{\mathrm{n-well}} C_{\mathrm{db}} R_{\mathrm{n-well}} \\ \quad - j\omega^3 C_{\mathrm{n-well}} C_{\mathrm{sub}} C_{\mathrm{db}} R_{\mathrm{n-well}} R_{\mathrm{sub}} \\ Z = j\omega \left(C_{\mathrm{sub}} + C_{\mathrm{sb}}\right) - \omega^2 C_{\mathrm{sb}} C_{\mathrm{sub}} \left(R_{\mathrm{n-well}} + R_{\mathrm{sub}}\right) \\ \quad - \omega^2 C_{\mathrm{n-well}} C_{\mathrm{sub}} \left(R_{\mathrm{n-well}} + R_{\mathrm{sub}}\right) \\ \quad - \omega^2 C_{\mathrm{n-well}} C_{\mathrm{sb}} R_{\mathrm{n-well}} \\ \quad - j\omega^3 C_{\mathrm{n-well}} C_{\mathrm{sb}} C_{\mathrm{sub}} R_{\mathrm{n-well}} R_{\mathrm{sub}} \\ R_{\mathrm{eq}} = R_{\mathrm{float}} + R_{\mathrm{n-well}} \end{cases} \tag{A.18}$$

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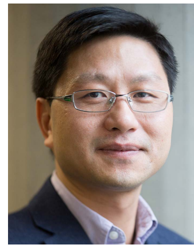

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