# Editorial
# Special Issue on Circuits and Systems for Emerging Computing Paradigms

As Dennard's law is coming to an end, on-chip power consumption reduction and throughput improvement due to technology scaling pose serious challenges; workloads of today's applications (such as AI, big data, and the IoT) have also reached extremely high levels of complex computation. Power dissipation has become the fundamental barrier to scale computing performance across all technology platforms. Computation at nanoscales requires innovative approaches. Moreover, many emerging computing paradigms have been widely studied (e.g., approximate, stochastic, neuromorphic, and in-memory), mostly at a system level to alleviate the encountered hurdles; however, their successful evolution necessitates implementations that require efficient circuits in a multitude of modules (such as memory, arithmetic, and control). Substantial challenges remain also at architectural and system levels. Although bridging of technology with circuit design has attracted significant attention from academic and industrial communities in the past decade, it still requires considerable efforts to accomplish implementations that are energy-efficient and high-performance for systems in diverse computing applications.

As Guest Editors, we are delighted and honored to introduce you to the readership of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS's Special Issue on Circuits and Systems for Emerging Computing Paradigms; it consists of eight articles that have been accepted through a rigorous peer-review process. Each submission has been reviewed by three experts in its research area, and only articles that have consistently shown the highest quality standards have been accepted.

It is well known that approximate computing (AC) is a promising paradigm to improve the energy efficiency of computing hardware for error-tolerant applications, with acceptable quality degradation at the output. In [A1], Wu *et al.* propose an energy-efficient and high-performance approximate divider based on logarithmic conversion and piecewise constant approximation. In this design, the range for the conversion between binary and logarithmic numbers is first expanded from [0,1] to [−0.5,1]. A heuristic search algorithm is then devised to find the most accurate constant set to approximate the reciprocal of the divisor by minimizing a statistical error. The hardware implementation is presented for both floating-point and integer dividers.

In [A2], Paludo and Sousa propose two architectures for the acceleration of number theoretic transforms (NTTs) using a novel Montgomery-based butterfly. The performance of the proposed architectures is assessed on a Xilinx Ultrascale+ FPGAs and with an application-specific integrated circuit (ASIC) on 28-nm CMOS technology. In FPGAs, the results for custom acceleration show substantial reductions in the number of lookup tables (LUTs) and registers, block RAMs (BRAMs), and digital signal processors (DSPs).

In [A3], de Abreu *et al.* present a technique for approximate comparison to constants referred to as C2Pax. It reduces area and energy of tree-based accelerators. This technique consists of finding alternative constants that reduce circuit area, while keeping an efficient prediction performance.

In [A4], Hou *et al.* address spin-orbit-torque magnetic random-access memory (SOT-MRAM), a technology that has received substantial attention in the research community. This article presents a reconfigurable physically unclonable functions (PUF) based on SOT-MRAM, which exploits thermal noise as a dynamic entropy source. Therefore, the MRAM cells could be configured to random final states by utilizing a stochastic switching mechanism.

Stochastic operation is also the focus of [A5] by Chen *et al*. This work proposes both the architecture of a stochastic computing (SC) multiply-and-accumulate (MAC) unit and the overall acceleration strategy of a CNN accelerator suitable to SC. A low-complexity bit-stream-extending method is also proposed to suppress the computation error of SC and ensure the trained fix-point model can be deployed to SC-based hardware without fine-tuning.

In [A6], Li *et al.* have addressed a different topic; computing systems working in harsh environments are prone to suffer from radiation-induced soft errors; for example, single event upsets (SEUs) and single event transients (SETs) are significant reliability issues for circuits fabricated at nanoscale ranges. In this article, a low-cost SET and SEU error-tolerant flip-flop (SETU-TOFF) is proposed; based on the traditional flip-flop, two high-level sensitive redundant latches are added to the input data of the latch at different times, and a voter is designed for generating the correct output.

The next article is by Li *et al.* [A7]; the complexity and size of recent deep neural network (DNN) models have increased significantly in pursuit of high inference accuracy. A chiplet-based accelerator is considered a viable scaling approach to provide substantial computation capability and on-chip memory for the efficient process of such DNN models. ASCEND introduces a novel photonic network that supports

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seamless intra- and inter-chiplet broadcast communication, and flexible mapping of diverse convolution layers; moreover, a tailored dataflow that exploits the ease of broadcast property and maximizes parallelism by simultaneously processing computations with shared input data is also accomplished.

In [A8], Liu *et al.* exploit an extended wireless technology to design a power-efficient and high-throughput DNN accelerator, e-WiNN, which can be configured for representative dataflows and arithmetic precisions. A novel design is leveraged by utilizing Dadda-algorithm-based MAC circuits. The proposed wireless transmitter integrates an ON–OFF keying (OOK) modulator with a power amplifier that results in significant energy savings.

We are confident that you will find these articles to be of invaluable help in your ongoing research investigations and appreciating them as we have enjoyed organizing this Special Issue.

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## APPENDIX: RELATED ARTICLES

[A1] Y. Wu *et al.*, "An energy-efficient approximate divider based on logarithmic conversion and piecewise constant approximation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Apr. 28, 2022, doi: 10.1109/TCSI.2022.3167894.

[A2] R. Paludo and L. Sousa, "NTT architecture for a linux-ready RISC-V fully-homomorphic encryption accelerator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Apr. 27, 2022, doi: 10.1109/TCSI.2022.3166550.

[A3] B. A. de Abreu, G. Paim, M. Grellert, and S. Bampi, "C2PAx: Complexity-aware constant parameter approximation for energy-efficient tree-based machine learning accelerators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Apr. 27, 2022, doi: 10.1109/TCSI.2022.3169028.

[A4] Z. Hou *et al.*, "Reconfigurable and dynamically transformable in-cache-MPUF system with true randomness based on the SOT-MRAM," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Apr. 27, 2022, doi: 10.1109/TCSI.2022.3168133.

[A5] Z. Chen, Y. Ma, and Z. Wang, "Hybrid stochastic-binary computing for low-latency and high-precision inference of CNNs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, May 18, 2022, doi: 10.1109/TCSI.2022.3166524.

[A6] J. Li, L. Xiao, L. Li, H. Li, H. Liu, and C. Wang, "A low-cost error-tolerant flip-flop against SET and SEU for dependable designs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Apr. 27, 2022, doi: 10.1109/TCSI.2022.3168082.

[A7] Y. Li, K. Wang, H. Zheng, A. Louri, and A. Karanth, "Ascend: A scalable and energy-efficient deep neural network accelerator with photonic interconnects," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, May 6, 2022, doi: 10.1109/TCSI.2022.3169953.

[A8] S. Liu, T. F. Canan, H. Chenji, S. Laha, S. Kaya, and A. Karanth, "Exploiting wireless technology for energy-efficient accelerators with multiple dataflows and precision," *IEEE Trans. Circuits Syst. I, Reg. Papers*, early access, Apr. 21, 2022, doi: 10.1109/TCSI.2022.3166752.