Automotive Switched-Capacitor DC–DC Converter With High BW Power Mirror and Dual Supply Driver

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***Abstract*— This paper presents circuit topologies and implementations for SC DC-DC converters with controlled charging current. It focuses on the power current mirror that regulates the charging current of the flying capacitor and on the switch drivers. The bandwidth and transient response of the power mirror are improved by inserting an auxiliary current mirror in its input signal path. Conventional switch drivers need power supplies with fast response to load transients; the driver presented here is less demanding, as only its core is biased internally, while the output stage is supplied directly by the converter input voltage. The circuit has an additional "Linear Regulator" mode of operation, whereby the power mirror is turned into a pass transistor. This expands the low-end limit of the converter input voltage. These solutions were used to design in a 130nm BCD technology an automotive SC DC-DC converter. Simulations and measurements performed over the entire automotive temperature range (−40C to +150C), for supply voltages between 8V and 28V, demonstrate that the converter meets all requirements: it can operate with output capacitors as small as 1μF; it provides regulated 5V output voltage for load currents up to 200mA, ensuring a low output voltage ripple, of 35mV and 9mV for output capacitors of 1μF and 10μF, respectively; its efficiency peaks at 81.3% for the typical battery voltage level, 12V.**

***Index Terms*— Switched capacitor, dc-dc converter, high bandwidth current mirror, switch driver, power management.**

I. Introduction

SWITCHED Capacitor (SC) DC-DC converters are increasingly popular choices for low- and mid-power applications [1]–[9], including in the automotive area [10], [11]. In general, their power efficiency is significantly larger than that of linear regulators and they can be more cost-effective than inductor-based converters for low power applications.

Several approaches to control the SC DC-DC output voltage have been reported, of which the current-mode control has at least two important advantages. First, during the charging phase, the inrush current drawn from the supply is significantly reduced, which improves the EMC performance. Second, the feedback regulation loop helps reduce the output voltage ripple.

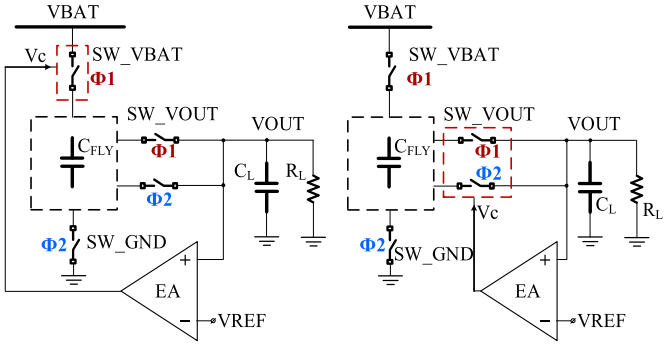

Fig. 1. Generic block diagram of a current-controlled SC DC-DC with two possible circuit positions for the regulated current source.

The current-mode regulation is achieved by controlling one or both of the charging or discharging currents. One or more of the power switches that ensure the SC DC-DC converter operation are also used to realize the current control. The converter performance is determined both by the phase(s) during which the current is controlled and by the position relative to the flying capacitor(s) of the switch turned into regulated current source. Fig. 1 presents two possible locations within a SC DC-DC converter with one flying capacitor, CFLY: i). between the input supply and CFLY – the switch denoted SW_VBAT and ii). between CFLY and output – the switch denoted SW_VOUT. It is also possible to use the switch placed between CFLY and ground – denoted SW_GND in Fig. 1 – as the control element. However, this topology is suitable only for step-up converters [12].

Table I. lists the solutions proposed in [2] - [12] considering the phase during which output regulation is performed and the position relative to CFLY of the regulated current source.

If the output is regulated during the discharging phase the inrush current drawn from the battery supply is not limited by the regulation loop. The large current glitches seen at the input of the voltage doubler proposed in [13] illustrate this drawback.

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TABLE I
SUMMARY OF SC SOLUTIONS WITH CONTROLLED CURRENT

Position of the regulated current source	Regulation Phase		
	Charging	Discharging	Both
VBAT	[3] [6] [10] [11][13] [14]	-	[15]
VOUT	[4]	[16]	[5] [12]
GND	[17]	-	[15] [2]

In [4] the switch connected between CFLY and VOUT – that corresponds to the switch denoted SW_VOUT in Fig. 1 - was used as the control element during the charging phase. It employs an NMOS having the bulk connected to ground. Unfortunately, this solution is not suitable in our case. Having the bulk at a lower potential than the source results in a larger threshold voltage. Therefore, a dedicated driver is required to accommodate the large gate drive overhead in order to fully open/close the switch. Moreover, safe operating area (SOA) constraints for the gate-bulk voltage impose the use of a bulkier device for this switch, instead of the dedicated power device.

The current-mode control achieved by regulating the switch placed between CFLY and the input supply – that corresponds to the switch denoted SW_VBAT in Fig. 1- during the charging phase is the most popular option [3], [6], [7], [10], [11], [13], [14].

Let us now focus on the SC DC-DC converter presented here: a step-down converter suitable for automotive applications, where VBAT can take values over a wide range. In this case, regulating the output during the charging phase is desirable as it limits the potentially large inrush current drawn from the battery supply. With respect to efficiency, controlling the output connected switch, SW_VOUT, is the best design option. However, this implies that the SW_VOUT switch must be implemented with NMOS transistors with the bulk connected to ground, similar to [4]. When the converter transitions to the discharging phase, the NMOS switch is closed by forcing its gate-source voltage to a low enough value. Fig. 1 shows that the NMOS source remains connected to the converter output while its drain is shorted to ground via SW_GND. Connecting the NMOS bulk to the source would cause the bulk diode to be forward biased; in turn, this would short the output to ground via the bulk diode and the SW_GND. Therefore, the bulk of the NMOS switch has to be connected to ground. This way, the NMOS switch passes no current during the discharging phase, regardless of the voltages that develop at its drain and source.

Having said that, this solution leads to a larger NMOS size than for the case the NMOS bulk is connected to its source. The area overhead is unacceptably large for automotive applications, where VBAT can go up to 26-30V. One concludes that for this application the optimal design solution is regulation of the output voltage during the charging phase achieved by using the switch connected to the input supply, SW_VBAT.

Fig. 2 presents a popular architecture for such SC DC-DC converters: regulation is performed during the charging phase – denoted Φ1 in Fig. 2 – and the SW_VBAT used as a current-controlling element implemented by the M1 and M2 current

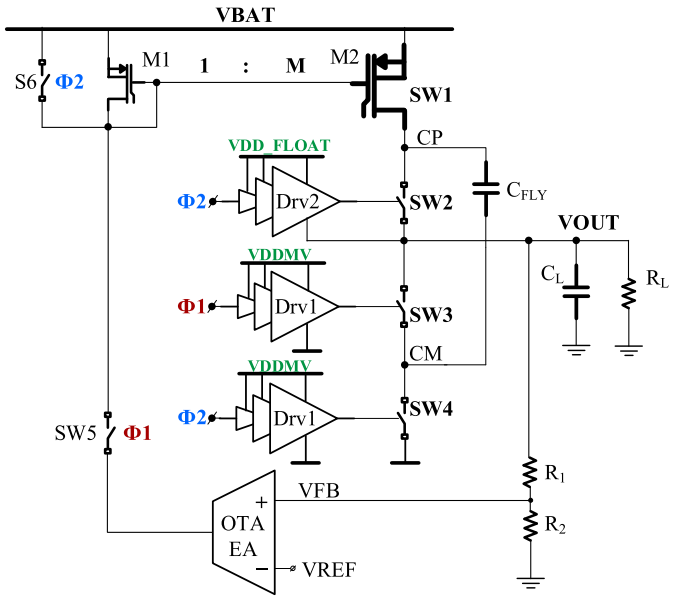

Fig. 2. Conventional architecture of SC DC-DC converters that perform regulation during the charging phase, by controlling switch SW1 connected to the input voltage, VBAT.

mirror [3], [6], [10], [11], [13], [14]. The current flowing through M2 is obtained by multiplying the current through M1 – controlled by the error amplifier denoted OTA in Fig. 2 - by the current mirror gain M. The value of M should be set considering the maximum value of the SC DC-DC output current and the output current capability of the OTA.

Usually, M is set to a large value, up to several thousands, so that the OTA load is relatively small. Therefore, one can push the OTA internal pole to high frequency by employing a small OTA output stage. Consequently, the converter loop exhibits only two poles: one at the output of the SC converter and the other given by the large parasitic capacitance in the gate of the power mirror. Using a lower value for M has certain advantages but makes frequency compensation more difficult. The OTA load is larger than for the large M save, so the OTA output stage has to be larger. This brings the OTA internal pole to lower frequencies, impacting stability. For a conventional design it is quite challenging to ensure the stability of this system while maintaining a large unity-gain frequency. This point will be detailed in the next Section. This work introduces a circuit topology that allows the designer to ensure the stability of a SC converter even for low value of the current multiplication factor M, while providing a wide bandwidth and fast response time.

Each switch within an SC converter needs a suitable driver – see blocks denoted Drv1,2 in Fig. 2. In turn, conventional high-speed drivers, capable of handling large capacitive loads, require low-impedance supply lines. Without such a low-impedance supply, the large current demanded by the output stage of the driver will cause the supply line to drop significantly, thereby degrading the performance of the driver. This paper proposes a solution that sidesteps the challenge of designing a low-impedance power supply required by a conventional driver. The main idea is to supply the last stage of the driver (which is current demanding) from the

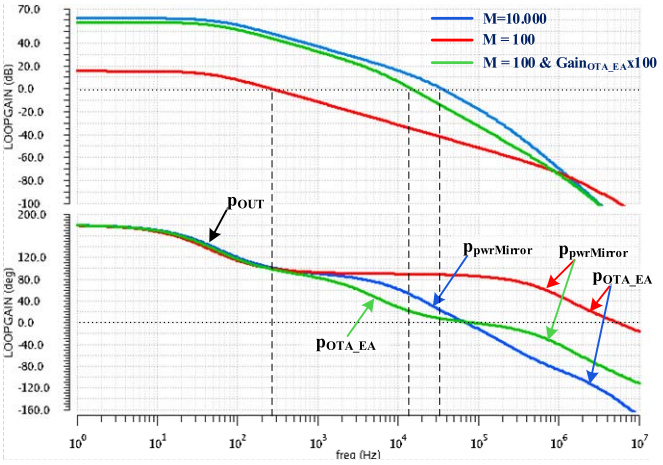

Fig. 3. Loop gain of the SC DC-DC converter shown in Fig. 2, in the regulation phase, for two values of the current mirror gain, M = 10000 and M = 100. Increasing the EA gain to compensate for the gain loss (due to lower value of M), brings the pole of the EA much lower in frequency leading to poor phase margin.

converter input - inherently a low-impedance power supply. The remaining stages within the driver (which do not sink large currents) are to be supplied from an internal medium-voltage supply line, denoted VDDMV in Fig. 2, whose impedance has a negligible impact on the driver performance.

Section II presents the proposed SC DC-DC converter topology, detailing the circuit implementation of its key functional blocks: the OTA, the high bandwidth power mirror, and the driver with two supply lines. Small signal analysis highlights the enlarged bandwidth of the new power mirror. These blocks were used to implement an SC convertor for automotive applications in a 130nm BCD technology. The sizing strategy, as well as simulation and measurement results, are presented in Section III. The performance of the resulting convertor is compared against state-of-the-art in Section IV, which also presents the main conclusions drawn from this work.

II. Proposed Power Supply With Two Modes of Operation: "SC Converter" and "Linear Regulation"

A. Design Options for the Power Current Mirror

The key design parameter for the power current mirror implemented by transistors M1-M2, is the current gain, denoted M in Fig. 2. The values usually considered for M range from tens-hundreds to several thousands. Fig. 3 presents the loop gain of the SC DC-DC converter shown in Fig. 2 for two values of the current mirror gain: M = 10000 and M = 100.

Let us analyze in detail the extreme design choices:

i). Choose a large value for M, of several thousands. In this case the power mirror has to do the heavy lifting (high current multiplication) while the OTA is required to only provide a small-value current signal. This approach avoids having large transistors in the signal path within the OTA and results in a minimum number of low frequency poles: one at the output of the SC converter and one given by the large parasitic capacitance in the gate of the power mirror. Straightforward dominant pole frequency compensation is achieved by imposing a large enough output decoupling capacitor such that the unity-gain frequency of the feedback loop, f_{0dB}, is smaller than the frequency of the pole introduced by the power mirror. This case is illustrated by the blue plots in Fig. 3.

ii). Set the value of M in the range of tens to hundreds. If the OTA_EA remains the same as in the previous case the resulting loop gain drops to unacceptable low levels. This case is illustrated in Fig. 3 by the red-line plots.

The gain of the error amplifier has to be increased to compensate for the loop gain loss, but this means the OTA_EA has to provide a far larger output current than in the previous case. The size of transistor M1 has to be larger, as the aspect ratio of M2 remains unchanged, set by the required ON resistance of SW_VBAT and the maximum output current provided by the SC converter.

The larger transconductance of transistor M1 helps reduce the impedance at the gate of the power mirror, thereby pushing the corresponding pole to higher frequencies than in the previous case. However, a larger OTA output stage yields a considerably larger parasitic capacitance pushing the pole of the OTA to lower frequencies. Thus, these two poles will be located at relatively close frequencies. This case is illustrated in Fig. 3 by the green-line plots. Ensuring the stability of this loop – which also comprises a third pole associated with the output node of the converter - while maintaining a large unity-gain frequency can be quite challenging.

One can use a very large output capacitor to push the unity-gain frequency below the two non-dominant poles. This ensures the system stability but the resulting bandwidth is similar to the one yielded by the large-M case, and the system responses to load and line transients are similarly slow.

B. Topology of the Proposed SC DC-DC Converter With an Additional "Linear Regulation" Operation Mode

The architecture of the proposed SC DC-DC converter is shown in Fig. 4. The four switches – SW1 to SW4 – at the core of the converter are enclosed within a negative feedback loop formed by the resistive divider R1 & R2 and transconductance error amplifier (OTA). While SW2-4 are voltage-controlled, SW1 is connected in a current-mirror fashion that enables its control by the current-output error amplifier – denoted OTA EA in Fig. 4.

For several functional block within the SC converter presented here this work proposes circuit solutions significantly different from the conventional ones. They are highlighted in Fig. 4 by dashed rectangles, and help improve the overall performance of the converter. First, SW1 is implemented by a current mirror with a larger bandwidth and higher slew rate than a regular mirror. This improves the speed of the regulation loop but also – as it will be shown in the following – it allows for the use of a smaller output capacitor than the conventional design, without diminishing the transient performance.

Second, a proposed dual supply driver is used to drive the remaining switches. Design time and circuit complexity are reduced by using same driver for SW2-SW4. Furthermore, Fig. 4.a. shows that the driver is connected capacitively to the

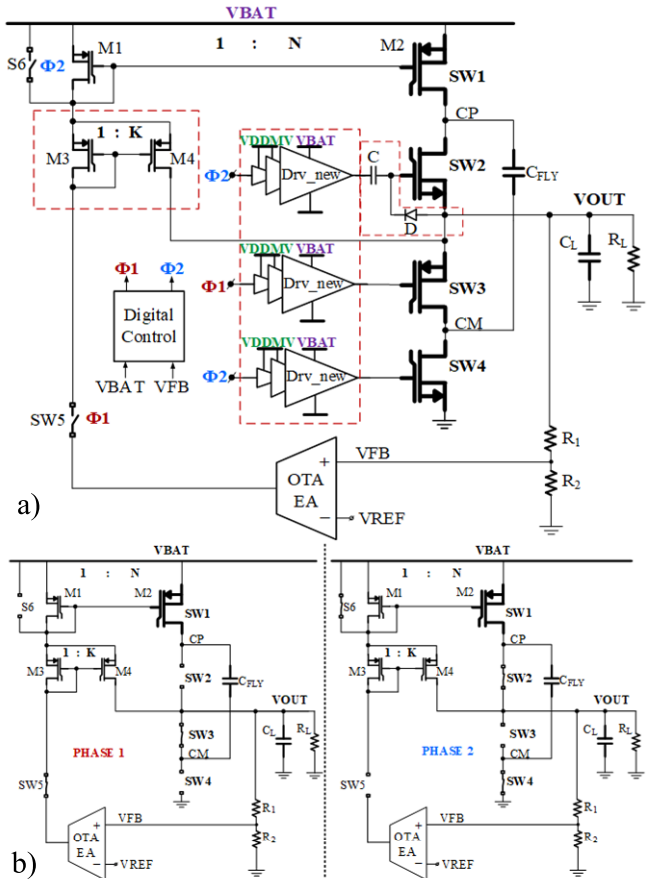

Fig. 4. a) Architecture of the proposed SC DC-DC converter. The dashed-line rectangles highlight the main differences with respect to the conventional architecture shown in Fig. 2, b) equivalent circuit for each phase of operation.

gate of SW2, by using a capacitor-diode network; this enables the use of NMOS transistor to implement SW2, instead of the bulkier PMOS transistor used in conventional designs.

The Digital Control block can switch the converter between two operating modes: "SC converter" and "Linear Regulator".

In "SC converter" mode the circuit switches between two phases of operation, similarly to the conventional SC converter shown in Fig. 2:

- when phase 1 is active, switches 1, 3 & 5 are on, placing CFLY in series with the output - see Fig. 4.a. Thus, CFLY gets charged by the Power Current Mirror.
- when phase 2 is active, switches 2, 4 & 6 are on, disconnecting CFLY from the Power Current mirror and placing it in parallel with the output - see Fig. 4b. Thus, charge from CFLY is transfer to COUT.

The output voltage is regulated during phase 1, during which the feedback loop controls the current that charges the CFLY.

No additional circuitry is necessary to implement the "Linear Regulation" mode, as this topology inherently comprises a voltage-regulation feedback loop. To implement this mode of operation, one only needs to keep the voltage-regulation feedback loop always active. This can be achieved by inhibiting the digital controls that disable it when in phase 2 of the "SC converter" mode of operation. Thus, the power mirror is shorted to VOUT by SW2 and the flying

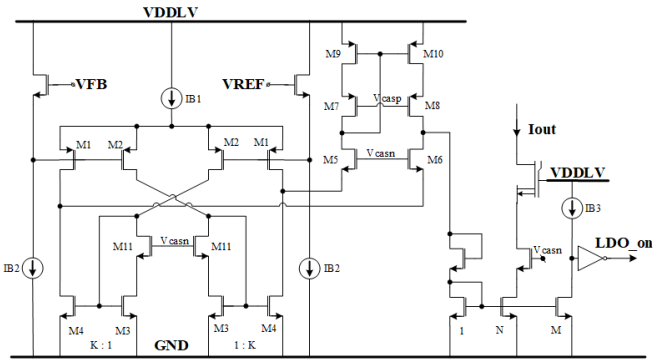

Fig. 5. Transistor level implementation of the transconductance error amplifier, denoted OTA EA in Fig. 4.

capacitor is connected in parallel with CL, by holding SW4 in the ON state.

Two scenarios trigger the converter to enter continuous regulation mode: (1) the input supply voltage is lower than the minimum required for proper operation, (2) the load current demand is small. The first scenario is detected by monitoring the input supply line. In this case, the "Linear Regulation" mode extends the input voltage range of the converter for which the output is regulated. The second scenario is detected by sensing the output current. This is achieved by adding a secondary output to the current mirror comprising the OTA EA output stage, as illustrated in Fig. 8. The current in this secondary output resembles a fraction of the total final load current. In this case, switching from the "SC converter" mode to the "Linear Regulation" mode improves efficiency, which at small loads is mainly determined by switching losses. Note that in "Linear Regulation" operation mode the output voltage is ripple-free.

To avoid large output voltage overshoots during the charging phase of the "SC converter" mode or the continuous regulation of the "Linear Regulator" mode, the Digital Control also monitors the output voltage VOUT. In case of an overshoot larger than a set value, the Digital Control block will bring the converter to phase 2 by switching OFF the power mirror and connecting CFLY in parallel with CL. This allows the output to discharge back to its nominal value at which point the converter resumes its normal operation.

C. Proposed High Bandwidth Power Mirror

1) Schematic: The bottleneck for designing the power mirror is the large parasitic capacitance given by the gate of SW1: one needs to obtain a large current multiplication without introducing large time constants in the signal path to the gate of SW1.

To address this challenge, we propose the current mirror in Fig. 6.b). One notices that a second auxiliary current mirror (M3-M4) is introduced in the input signal path of the main current mirror (M1-M2). The advantage of employing this arrangement is twofold.

First, it achieves high overall gains by cascade multiplication.

$$Gain_{CM\_proposed} = \frac{Iout}{Iin} = N\,(K+1) + K \qquad (1)$$

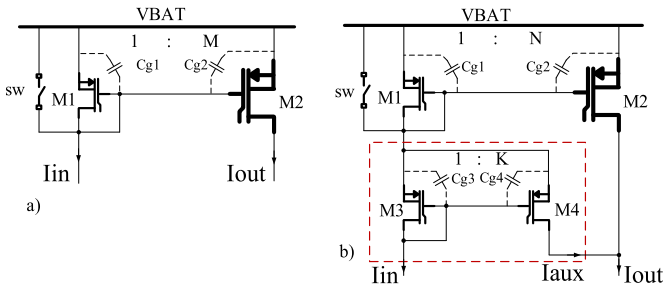

Fig. 6. Schematic of the conventional (a) and proposed (b) power mirror. The additional current mirror within the dashed-line rectangle amplifies the current available to charge the large parasitic capacitance of the power switch, improving both bandwidth and speed.

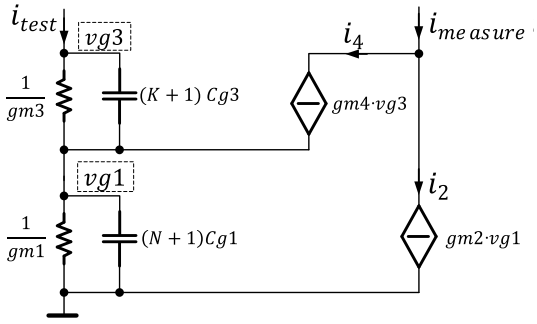

Fig. 7. Small signal equivalent model for the improved power mirror shown in Fig. 6 b).

For the same overall multiplication factor as the conventional one in Fig. 6.a), the size of M1 is larger than its counterpart. This leads to lower impedance in the gate of the power mirror which in turn leads to larger bandwidth and higher speed.

Second, it does not introduce large time constants in the signal path. The auxiliary current mirror, while introducing a second parasitic capacitance, is much smaller than that of the main power mirror. It needs to ensure only a pre-multiplication of the signal. Moreover, one notices that the current charging the gate of the auxiliary current mirror is also charging (multiplied by a factor of $K+1$) the gate of the power mirror. This translates to a faster charging time compared with the conventional mirror. Most importantly, all these benefits are obtained for free - with zero increase in ground current consumption: the extra current through M1 is diverted to the output, not to the ground. This structure occupies more die area than the conventional one. By careful design, one can obtain a reasonably small acceptable area overhead.

Another possible limitation of the proposed power mirror is the need for larger voltage headroom at the output to ensure that M2 and M4 operate in saturation. To avoid this, while operating in the "SC converter" mode, the auxiliary output can be connected directly to the output of the SC converter - as shown in Fig. 4.a - thus bypassing the switching core. However, the power transfer through this auxiliary path is not optimum, thus the SC converter efficiency is degraded. The trade-off between bandwidth enlargement and converter efficiency is given by the percentage of the load current that the auxiliary current mirror delivers to the output: a larger current yields a larger bandwidth but diminishes the power efficiency.

2) Small Signal Analysis: Let us analyze the case for which the gain of the proposed current mirror is set to be equal with the gain of the conventional current mirror:

$$M = N\,(K+1) + K \tag{2}$$

Since the size of the power switch M2 is the same in both implementations, the equality in (2) implies that M1 in Fig. 6a) and M3 in Fig. 6b) are of equal sizes:

$$\begin{bmatrix} gm3 \\ Cg3 \end{bmatrix}_{proposed} = \begin{bmatrix} gm1^* \\ Cg1^* \end{bmatrix}_{conventional} \tag{3}$$

Assuming that all transistors are biased at the same DC OP, then the following equivalences are true:

$$gm1 = gm3\,(K+1) \quad Cg1 = Cg3(K+1) \tag{4}$$

Using the equivalent small signal model shown in Fig. 7, the transfer function for the improved power mirror is given by:

$$T = \frac{i_{test}}{i_{measure}} = Gain_{CM\_proposed}\frac{1+\frac{s}{\omega z}}{\left(1+\frac{s}{\omega dp}\right)\left(1+\frac{s}{\omega ndp}\right)} \tag{5}$$

in which $\omega z = \frac{gm3}{Cg3}\frac{N(K+1)+K}{N(2K+1)+K}$, $\omega dp = \frac{gm3}{(N+1)Cg3}$ and $\omega ndp = \frac{gm3}{(K+1)Cg3}$.

For the same multiplication factor, the conventional current mirror exhibits a dominant pole at $\omega dp^* = \frac{gm1^*}{(M+1)Cg1^*}$.

Given (2) and (3), the dominant pole is pushed up in frequency by a factor given by:

$$\frac{\omega dp}{\omega dp^*} = \frac{M+1}{N+1} = K+1 \tag{6}$$

This result highlights that the increase in bandwidth and speed is proportional to the gain of the auxiliary current mirror shown in Fig. 6b).

D. Proposed Versatile Driver With Two Supply Lines

The previous paragraph presented a circuit for driving SW1. Let us now present a new driver for the other switches within the SC converter shown in Fig. 4, SW2-SW4.

The proposed driver has two supply inputs – a low-voltage, low-power one, generated internally, and a high-voltage, high-power one, connected directly to the input supply of the converter. This concept ensures that the power demands for the driver supply circuit are greatly reduced and the speed of the driver is not degraded. Such a solution is made possible by the circuit in Fig. 8. It facilitates the employment of two supply lines by using a symmetrical NMOS output stage instead of the conventional complementary PMOS-NMOS pair. The first stage and the following chains of inverters are connected to the low power, internally generated, VDDMV line. The last stage, by having an HV NMOS (M1), allows the drain to be connected to an external high voltage power source. In this case, to avoid using multiple external power supplies, we chose to connect it to the existing input

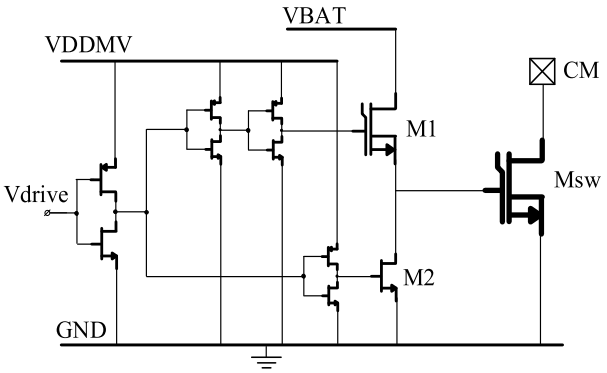

Fig. 8. Schematic of the proposed switch driver. Only the input stage is supplied by the internal VDDMV line, while the output stage is connected directly to the input voltage VBAT.

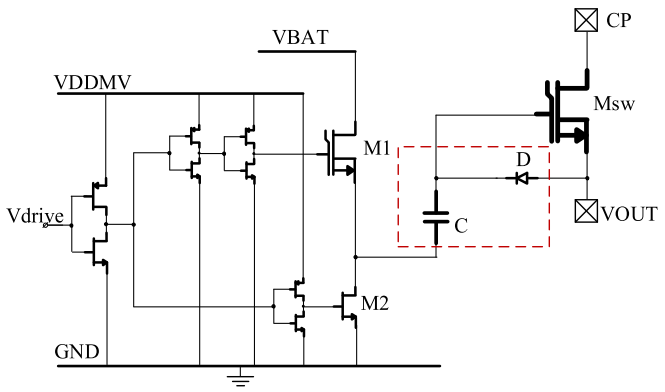

Fig. 9. By using the capacitive coupling depicted in the dashed-line rectangle the driver shown in Fig. 8 can be used to control floating switches, such as the switch denoted SW2 in Fig. 4.

power supply line (VBAT) of the SC converter. One notices that the source of M1 cannot exceed the value of the internal supply line, VDDMV, being limited to VDDMV-Vth. Thus, the gate of Msw can be brought up to a level close to, but not over, VDDMV, which is large enough to ensure it is fully turned on, while avoiding SOA violations. If available, M1 should be implemented with native transistors (Vth = 0). This will allow the gate of Msw to be brought even closer to VDDMV.

This circuit is used to drive SW3 & SW4 as shown in Fig. 4. One notices that the position of SW2 increases the complexity of its driver circuit. In the case of a PMOS switch, the gate would be referenced to the high voltage floating node CP. This would require either the use of a floating driver bootstrapped to CP or the employment of a capacitively coupling circuit to transfer the driving signal to the PMOS gate, as in [18]. In the case of an NMOS switch, the gate would be referenced to the output voltage VOUT. This requires a floating driver to switch the gate between VOUT and (VOUT+VGSn) or a different capacitively coupling circuit between the ground connected driver output and the gate of the switch.

A floating driver has the advantage that it allows the employment of an NMOS type switch. This is desirable since the NMOS has a lower Ron than a PMOS for the same area. On the other hand, a capacitive link between the driver and the switch provides the benefit of employing an already existing driver, like the one designed for SW3 & SW4.

In the following we propose a circuit arrangement that facilitates the link between a ground connected driver and an NMOS floating switch, thereby putting together the best from both worlds. The circuit shown in Fig. 9 consists of a capacitor – to transfer the driver output signal to the gate of the NMOS switch – and a diode - to provide a path for recharging the capacitor up to the voltage of the SC converter output during the OFF state of the switch. This simple solution reduces the SC converter design effort because it enables the use of an already existing driver - Fig. 8.

III. Design and Integration of an Automotive SC DC-DC Converter With Two Modes of Operation

A. SC Converter Requirements

The proposed SC converter was implemented in a 130nm BCD technology for the following requirements: regulated output voltage VOUT = 5V for the automotive input voltage range of VIN = 8V-28V [19], with a current capability, IL, from 100μA to 200mA and the load capacitance, CL, taking values as low as 1μF, and 500kHz switching frequency. The output voltage ripple should be maintained below 50mV. The power efficiency should not fall below 25% while its max value should exceed 80%. The output voltage undershoot ($-\Delta$Vout) and overshoot ($+\Delta$Vout) caused by line and load transients should be maintain within 10% of the nominal VOUT value. Finally, the SC converter must fulfill these requirements over the full automotive temperature range: from −40C to 150C.

B. Sizing Strategy

1) The Power Mirror: The following paragraphs will detail the necessary steps for sizing the proposed power mirror, optimized for power efficiency. To begin with, one needs as input data the values for the maximum OTA output current (I_{OTA_MAX}) and maximum value of the load current, I_{L_MAX}.

Step 1: Use (1) to compute the required gain of the power current mirror gain, as follows:

$$Gain_{PCM} = \frac{I_{L\_MAX}}{I_{OTA\_MAX}} \tag{7}$$

Step 2: Set the percentage of the total output current that should be delivered by the auxiliary current mirror as follows:

$$I_{AUX} = \frac{p}{100} I_{L\_MAX} \tag{8}$$

Step 3: From (8) compute K as follows:

$$K = \frac{p \cdot Gain_{CM\_proposed}}{100} \tag{9}$$

Step 4: From II-C.2) and III-B.2) find K and N.

In our case, the current mirror gain resulted in a value of ∼3000. For power efficiency reasons we chose I_{AUX} to be 1% of I_{L_MAX}. The larger the value for p, the less efficient the converter is. This yielded the following values for the first iteration step in sizing the current mirror: $K = 30$ and $N = 96$.

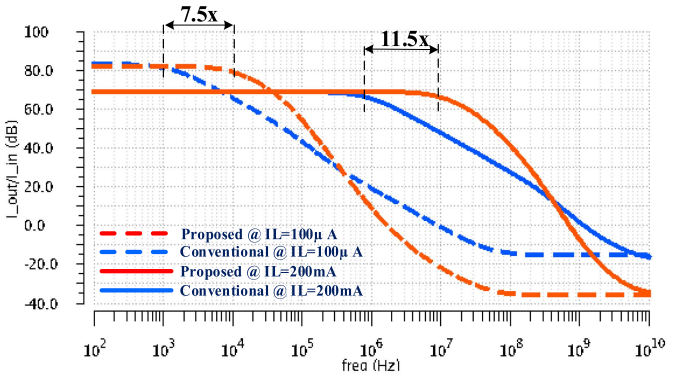

Fig. 10. Frequency characteristics of the proposed current mirror and its conventional counterpart – see Fig. 6 - for extreme values of the load current: IL = 100μA and 200mA.

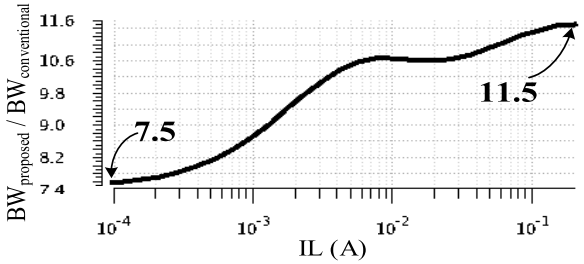

Fig. 11. The ratio between the −3B bandwidth of the proposed and the conventional current mirrors over the entire range of IL values.

2) The Flying Capacitor: For an output voltage drop of 40mV at the maximum load current of 200mA, the nominal impedance R_{NOM} is:

$$R_{NOM} = \frac{V_{out,drop}}{IL_{max}} = \frac{40mV}{200mA} = 0.2\Omega \tag{10}$$

The methodology described in [20] for open loop converters indicates that an optimal design is obtained by sizing the capacitors such that Z_{SSL} equals $\frac{R_{NOM}}{\sqrt{2}}$ at maximum switching frequency. It follows that $C_{FLY} = \frac{\sqrt{2}}{4 f_{sw} R_{NOM}}$. With the switching frequency set to 500kHz by design requirements the value of C_{FLY} resulted in 3.5μF.

However, in our case the converter operates in open-loop only half of the time - during the discharging phase-, while during the charging phase it operates in closed-loop. Thus, the C_{FLY} value was further optimized by iterative simulations and was eventually reduced to 1μF.

C. Simulation Results

1) Proposed High Bandwidth Power Mirror: This subsection presents results obtained by performing AC and transient simulations on both current mirrors shown in Fig. 6, designed with similar transistor sizes for same overall current gain. This provides a direct performance comparison between the conventional and proposed high-bandwidth current mirrors.

Fig. 10 shows the results yielded by AC analyses performed on the two current mirrors. Over the entire range of load currents, the bandwidth of the proposed power mirror is more than seven times wider than the bandwidth of the conventional mirror; at 200mA the BW extension reaches 11.5×.

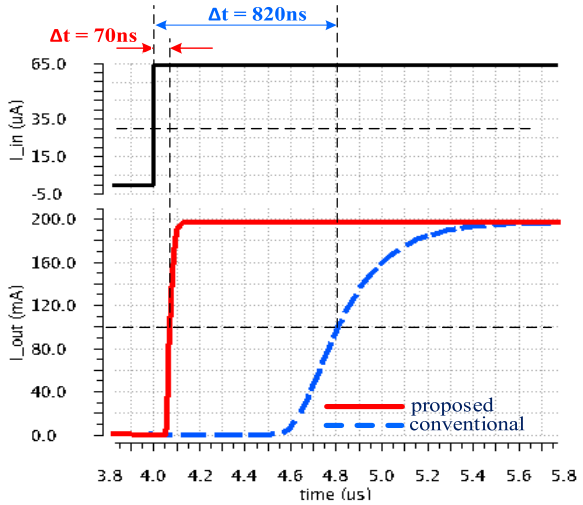

Fig. 12. Response of the proposed and conventional power mirrors to a steep increase of the current applied to their inputs: from 0 to 65μA corresponding to IL rising from zero to the maximum value of 200mA.

This result validates the expectations brought forth by the small-signal analysis performed in Section II.C.

Fig. 12 presents the response of the conventional and proposed current mirrors to an input current step. For this, the current applied to their inputs jumped from 0 to 65μA in 1ns.

One notices that for the conventional current mirror, the output current reaches 50% of its maximum value only after 820ns. Due to its preamplification stage, the proposed power mirror can reach the same output current level in only 70ns. This is equivalent to an 11.7× improvement in speed.

The following paragraphs will discuss the results for the entire SC-DCDC converter.

2) Frequency Characteristics of the Converter Loop Gain: The bandwidth enhancement brought forth by the proposed current mirror also impacts the frequency response of the Loop Gain of the entire SC-DCDC converter. Fig. 13 shows the frequency characteristics of the SC converter for CL = 1μ and two extreme values of the load current: IL = 100μA and 200mA. One notices that the phase margin obtained with the proposed current mirror is greater than 70 degrees over the entire current load range, while for the conventional current mirror the phase margin is only 30 degrees.

3) Starting-up the SC DC-DC Converter: The start-up behavior of the SC converter is shown in Fig. 14. The converter exhibits a clean start-up – no switching noise & no output overshoot – by operating in "Linear Regulation" mode and in current limitation. After the output capacitor is charged, an internal current limit allows normal "Linear Regulation" operation. During this operation mode, the output is regulated to its nominal value of 5V set by the internal resistive divider and the reference voltage. When VBAT reaches 11V the Digital Control switches from "Linear Regulation" to "SC converter" allowing the converter to regulate the output at maximum power efficiency.

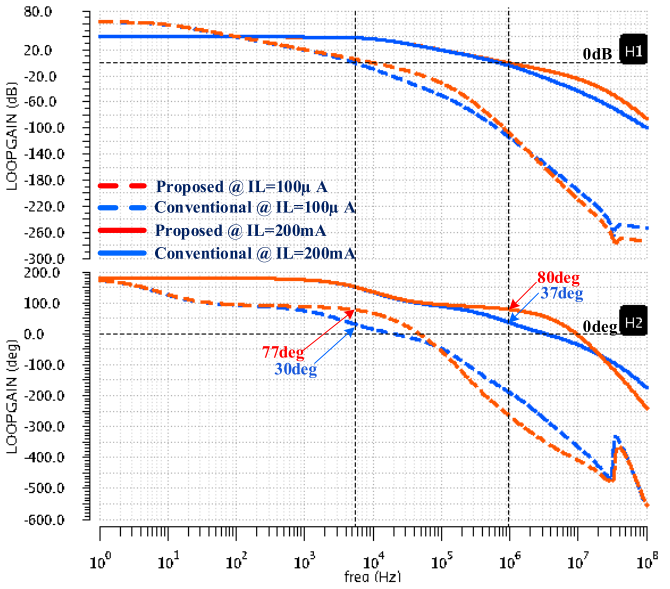

Fig. 13. Loop Gain Frequency characteristics for two versions of the SC converter implemented with proposed current mirror and its conventional counterpart: CL = 1μ and two extreme values of the load current: IL = 100μA and 200mA.

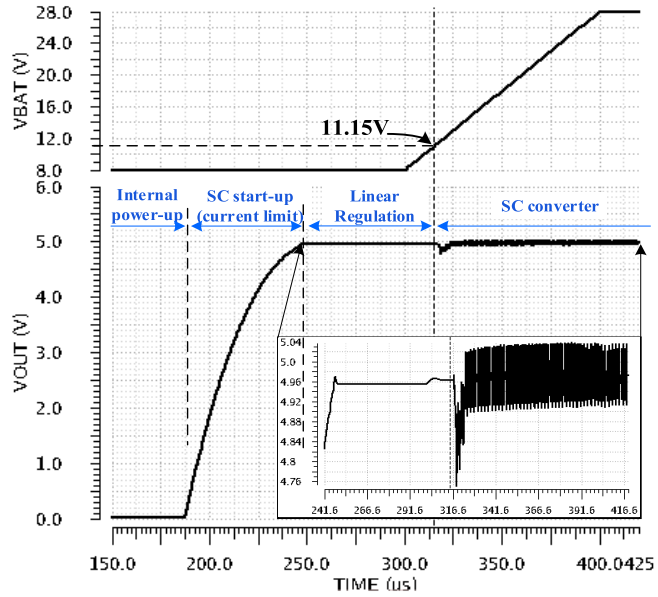

Fig. 14. Transient start-up behavior.

4) Operation in the "SC Converter" Mode: During steady state operation in "SC converter" mode the converter will sink current from the VBAT supply line only in the charging phase (phase 1). As such, the converter is equivalent to a pulsating load current for the battery supply rail. To ensure minimum perturbance of the VBAT line, the designer must limit the slope and peak value of the current drawn from the power input, without significantly reducing the speed of the converter. To achieve this delicate trade-off, the OTA maximum output current together with the gain of the Power Mirror were adjusted such that the SC converter draws an input current for which the slope and peak value are 6.1A/μs and 312mA, respectively - Fig. 15. These values directly impact the output voltage ripple of the converter.

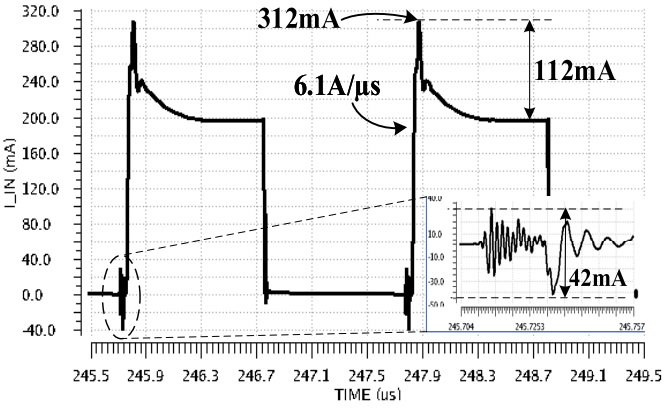

Fig. 15. Input current drawn from the battery supply of the SC converter for IL = 200mA and CL = 1μF.

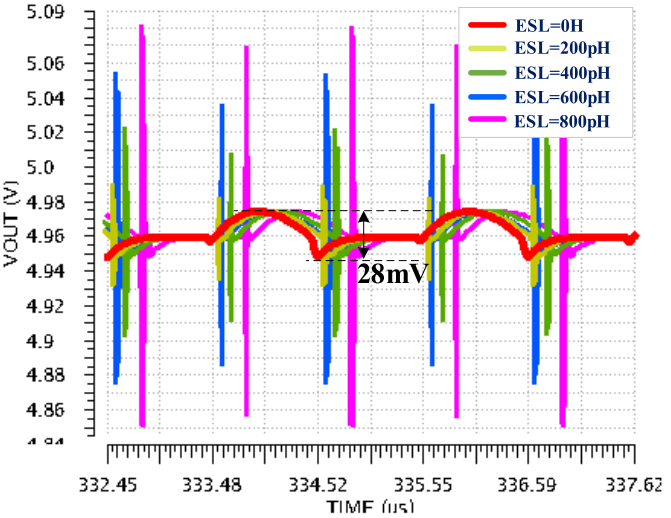

Fig. 16. SC converter output voltage ripple and glitches for different ESL values of CFLY and CL @ VBAT = 12V, CL = 1μF, IL = 200mA.

TABLE II
MAGNITUDE OF THE SC OUTPUT GLITCH FOR DIFFERENT ESL VALUES OF CFLY AND CL

ESL	Vout_pk2pk (CL=1µF)	Vout_pk2pk (CL=10µF)
0	28mV	3.4mV
200pH	61mV	58 mV
400pH	123mV	118 mV
600pH	182mV	174 mV
800pH	234mV	226 mV

The converter generates the highest output voltage ripple for maximum load current (200mA) and minimum load capacitance (CL = 1μF). In these conditions, the output ripple is 28mV, Fig. 16, while for CL = 10μF the output ripple is down to 3.2mV, Fig. 17.

The simulation testbench includes an inductor placed in series with each capacitor to model the impact of the ESL and that of PCB parasitics. The ESL causes large voltage glitches to appear at the output, several times larger than the output ripple intrinsic to the operation of the SC converter, as shown in Table II. These values can be reduced by careful

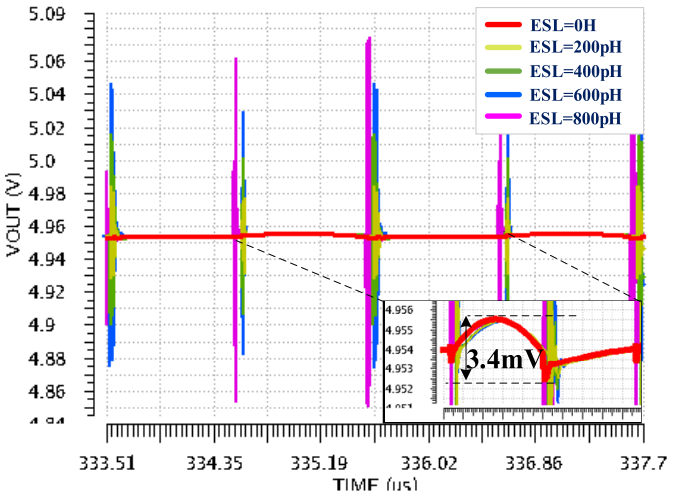

Fig. 17. SC converter output voltage ripple and glitches for different ESL values of CFLY and CL @ VBAT = 12V, CL = 10μF, IL = 200mA.

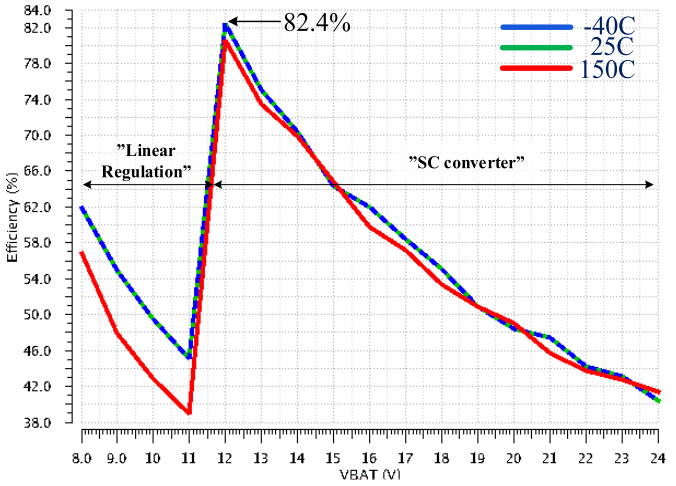

Fig. 18. Simulated power efficiency of the SC converter for IL = 200mA at three temperatures: −40C, 25C and 150C.

layout of the test board and by employing capacitors with very small ESL. Finding a solution that eliminates the ESL induced voltage ringing is not an easy endeavor and it is beyond the scope of this paper – which is to propose improvements for several key building blocks of an SC-DCDC converter.

Fig. 18 presents the power efficiency of the converter as a function of the supply voltage, VBAT, for IL = 200mA simulated at the minimum, typical and maximum values of the automotive temperature range. The proposed circuit achieves a maximum efficiency of 82.4% at VBAT = 12V for two temperatures: −40C and 25C. At 150C the efficiency is only slightly lower, 81%.

D. Silicon Implementation and Measurement Results

The circuit shown in Fig. 4 was implemented as a stand-alone integrated circuit and was assembled in a 14-pin surface mount package. Fig. 19 illustrates the floorplan of the converter, highlighting the main building blocks. All the analog blocks were placed in the lower-left corner, away from

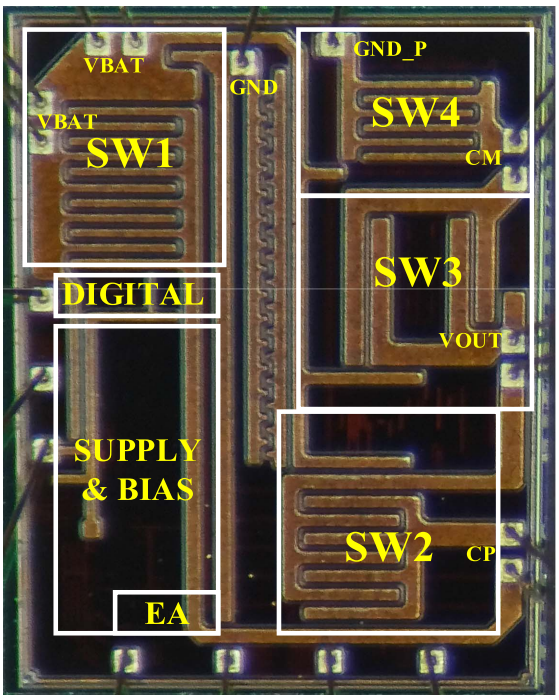

Fig. 19. Chip micrograph of the proposed SC converter.

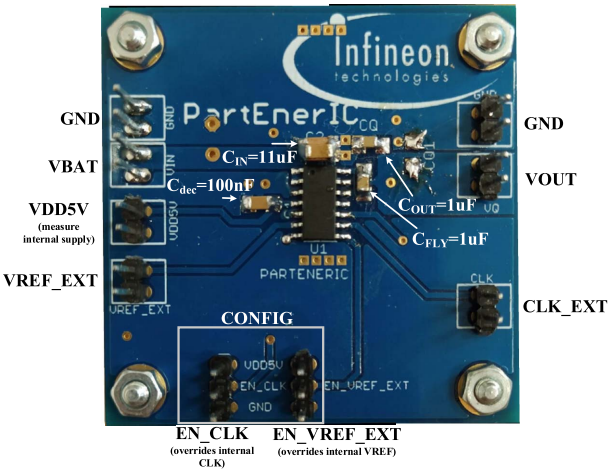

Fig. 20. Test board employed for conducting all measurements.

the noisy digital ones that occupy the rest of the chip. The output signal of the OTA EA is a current, less sensitive to coupling noise than a voltage signal. By placing this block furthest from the digital area – to avoid substrate noise – the long signal routing of its output current to the SW1 (the Power Mirror) will not impact the converter performance.

The Digital Control was placed approximately in the center of the chip, to facilitate the routing of the control signals to all switches. Finally, having each switch close to the IO pads facilitates the routing of power metals.

The test board employed for the test & characterization of the integrated circuit is shown in Fig. 20. One notices that all capacitors were placed as close as possible to the IC pins. Besides the main functional pins (VBAT, VOUT, GND), the board provides several test pins. A voltage applied to the "VREF_EXT" pin overrides the on-chip voltage reference

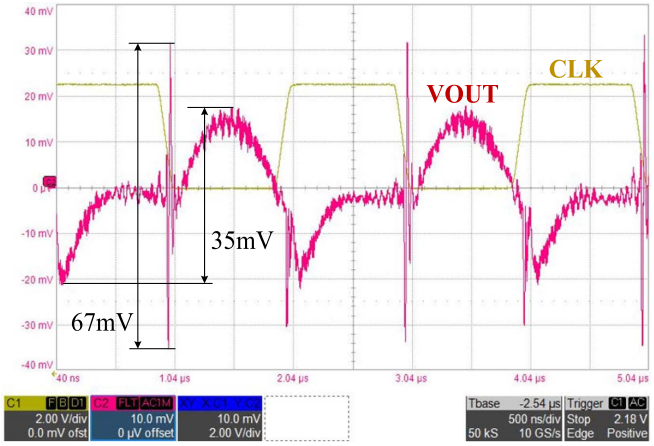

Fig. 21. SC output voltage ripple for VBAT = 12V, CL = 1μF and IL = 200mA.

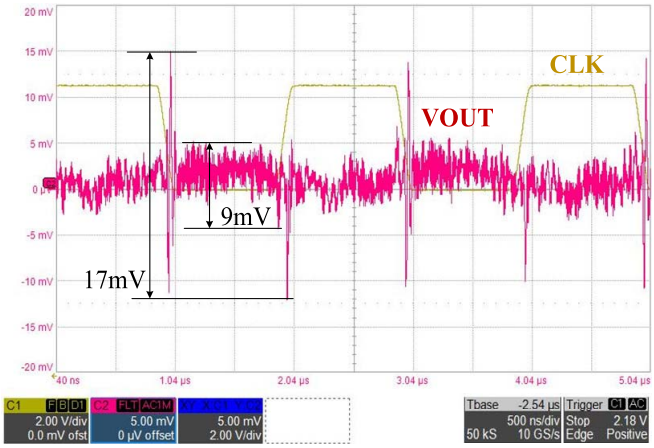

Fig. 22. SC output voltage ripple for VBAT = 12V, CL = 10μF and IL = 200mA.

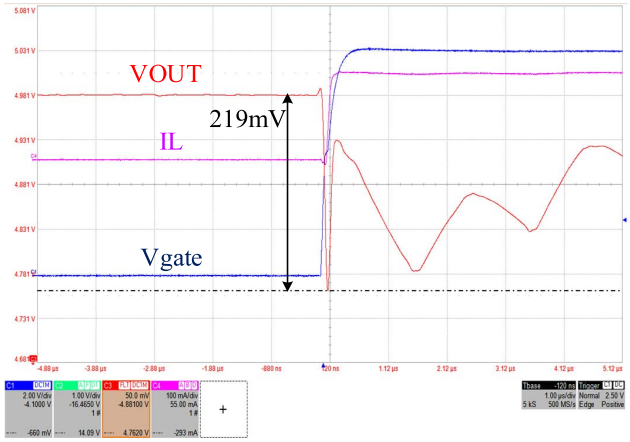

Fig. 23. SC DC-DC response to a positive IL step, from 100 μA to 200mA in 300ns. Vgate is the control voltage applied to the NMOS switch that implements the load jump. VBAT = 13.5V, CL = 1 μF.

when "EN_VREF_EXT"is set to "high". A digital clock applied to the "CLK_EXT" will pin will override the on-chip 500kHz oscillator, when "EN_CLK" is "high".

The DC performance of the converter is summarized by Table III, which shows side-by-side simulation and

TABLE III
SC DC LINE & LOAD REGULATION AT THREE TEMPERATURES

Temp.	DC Line Reg. [µV/V]		DC Load Reg. [µV/mA]	
	sim.	measure	sim.	measure
-40C	260	310	120	160
25C	260	134	180	205
150C	434	280	315	305

TABLE IV
MEASURED SC CONVERTER OUTPUT VOLTAGE UNDERSHOOT ($-\Delta$VOUT) & OVERSHOOT ($+\Delta$VOUT)

	VBAT=13.5V IL=100µA to 200mA, trise = tfall = 300ns			
	CL=1µF		CL=10µF	
T[C]	-ΔVout[mV]	+ΔVout [mV]	-ΔVout[mV]	+ΔVout [mV]
-40	193	291	258	331
25	219	256	318	211
150	238	264	300	376

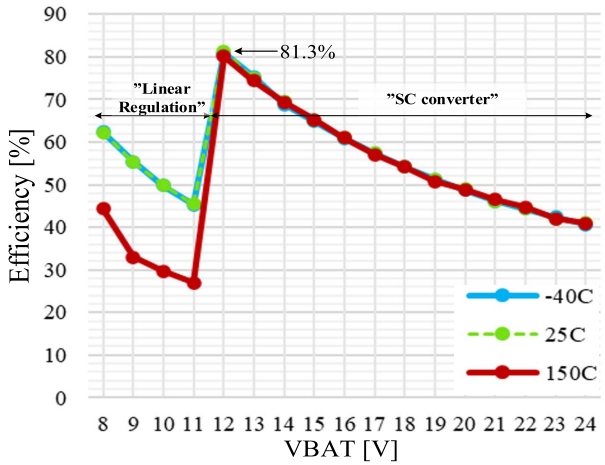

Fig. 24. Measured SC-DCDC efficiency for IL = 200mA at three temperatures: −40°C, 25°C & 150°C.

measurement results for the DC line & load regulation parameters over the entire automotive temperature range.

The output voltage ripple of the converter was measured at maximum load current for two values of CL. For CL = 1μF, the converter exhibits a voltage ripple of 35mV close to the value predicted by simulation results. For CL = 10μF the output voltage ripple is reduced to 9mV, slightly larger than predicted by simulations. The transient performance of the SC converter was analyzed by measuring the output voltage undershoot ($-\Delta$Vout) and overshoot ($+\Delta$Vout) caused by the following load step: IL jumping from 100μA to 200mA and back, in 300ns. Table IV summarizes these results for three temperatures encompassing the full automotive range. One notices that, for CL = 1μF, the output voltage variations are within 6% of the output voltage nominal value. For larger CL vales the converter loop bandwidth is diminished, leading to larger undershoot and overshoot values. Thus, for CL = 10μF, these values are within 7.5% of the nominal VOUT = 5V. The measurements presented in Figs. 21–23 are in line with the corresponding simulation results.

Fig. 24 presents the power efficiency of the converter for IL = 200mA as a function of the supply voltage VBAT,

TABLE V
PERFORMANCE COMPARISON SC IMPLEMENTATIONS WITH CONTROLLED CHARGING CURRENT

Parameters	[1]	[3]	[5]	[6]	[7]	[10]	[11]	[22]	[21]	This work
Year	2016	2012	2017	2014	2012	2013	2015	2020	2021	**2021**
CMOS [µm]	0.065	0.040	0.18	0.055	0.35	–	–	0.028	0.25 HV	**0.13**
Conversion Type	Step-down	Step-down	Step-down	Step-down	Step-down	Step-down & Step-up	Step-down	Step-down	Step-down	**Step-down**
Regulation technique	I_{CHARGE} control	I_{CHARGE} control	I_{CHARGE} control	I_{CHARGE} control	I_{CHARGE} control	I_{CHARGE} control	I_{CHARGE} control	PFM	PFM	I_{CHARGE} control
Input Voltage range [V]	2.4-2.6	3-3.6	1.8	3.3 – 3.6	2.7-5	2.7 - 38	1.8 – 6.5	1.9 – 6.3	3 – 4.3	**8-28**
Output Voltage [V]	1	0.95	1	1	1.8	2.5 - 5	3.3, 1.8, 1.5	0.9	1.8	**5**
IOUT [mA]	30m	300m	130m	250m	200m	250m	250m	500m	12m	**200m**
CFLY [F]	0.54n	0.1µ	1µ	0.1µ x 2	1µ	1µ	1µ x 2	470n x 4	2n	**1µ**
CL [F]	0.26n	1µ	2.2µ	1µ	10µ	4µ	4.7µ [a] 22µ [b]			**1µ**
Fsw [Hz]	90M	100k – 6M	1.8k – 270k	500k – 4M	16-500k	450k	800k		4M – 32M	**500k**
DC Load Reg. [mV/mA]	0.2	–	0.02	0.086	–	0.2	–			**0.205**
DC Line Reg. [mV/V]	–	–		3.91	–	–	–			**0.134**
–Vout [mV] (Load jump Undershoot)	195m [e]	150m	–	–	100m	–	–	290m	200m [e]	**219m**
+Vout [mV] (Load jump Overshoot)	195m [e]	100m	–	–	70m	–	–			**256m**
IL_{MIN} – IL_{MAX}	1mA – 31mA	30mA – 140mA	10mA – 100mA	10mA – 250mA	10mA – 100mA	–	–	20mA – 200mA	50µ – 10m	**0.1mA – 200mA**
Efficiency [%]	80.3 [c] 76.2 [d]	>72	83.3	90	87	81	90	85	83	**81.3**
ΔVout Ripple [mV]	2	30	<0.5	<30	<8	20*	50** 45***		50 [e]	**35 @ CL=1µ 9 @ CL=10µ**

*for CL=10µF, **CL=10µF & IL=150mA, ***CL=2x10µF & IL=250mA
a) IOUT<150m, b) for IOUT >150m, c) only SC, d) SC+LDO, e) estimated from figure,

measured at the minimum, typical and maximum values of the automotive temperature range. The maximum efficiency of 81.3% was obtained for VBAT = 12V, the first measurement point after the converter has switched from "Linear Regulation" mode to "SC converter" mode. As VBAT increases the power efficiency decreases. For lower values of VBAT the circuit operated in "Linear Regulation" mode, so the power efficiency is inevitably far lower, with the minimum value about 26%. High temperatures lead to large leakage currents and larger MOS transistor resistance. As such, the larger resistance of the pass transistor (SW1) leads to increased power losses when operated in "Linear Regulation" mode. Thus, at 150°C, the efficiency drops in the VBAT voltage range of 8V-11V.

These measurements are in good correlation with the simulations results shown in Fig. 18 and demonstrate that the circuit meets the design requirements set in Section III.A.

IV. COMPARISON WITH STATE-OF-THE-ART & CONCLUSION

A. Comparison With State-of-the-Art

The goals set for the circuit topology and implementation solutions proposed in this paper were i). to improve the transient response of the SC DC-DC converter and ii). to enlarge the range of CL values for which the feedback regulation loop of the converter is stable. The main features and parameters of the integrated converter presented in Section III are listed in the last column of Table V, alongside corresponding data for nine SC converters reported previously. Most of the converters chosen for this comparison regulate the output voltage by controlling the charging current of CFLY, similarly to the proposed converter. Two papers with regulation based on Pulse Frequency Modulation (PFM), were also included, [21] & [22].

The proposed converter can operate over a large input voltage range, from 8V to 28V, second only to [10]. From this supply it can deliver a maximum output power of 1W – ILmax = 200mA at a regulated output voltage VOUT = 5V – second only to the converter reported in [10].

The proposed converter exhibits the widest IL operating range of all converters listed in Table V, from 200mA down to 0.1mA.

An apparent weakness of the proposed converter is the relatively large voltage undershoots and overshoots caused at the converter output by load jumps. However, a fair comparison based on these parameters is not possible because the test conditions vary widely and some references do not give

enough data. The voltage undershoot and overshoot depend on the amplitude and slope of the load jump, as well as on the output capacitor value. Of the nine papers referenced in Table V only [1] gives the value of the slope of the load jump. Note that the ratio between the maximum and minimum load current values considered for the proposed converter is very large: $IL_{MAX}/IL_{MIN} = 2000$, that is 10 to over 400 times larger than the other converters considered here.

Let us now focus the comparative analysis on converters that can operate with CL value of 10μF. The proposed converter exhibits the second best lowest voltage ripple: 1mV larger than [7], 11mV and 41mV smaller than [10] and [11], respectively.

B. Summary and Conclusion

This paper introduced improvements to the topology and circuit implementation needed to develop SC DC-DC converters for automotive applications.

Circuit improvements focused on two functional blocks essential to implementing a high-performance SC converter with controlled charging current: the power mirror that regulates the charging current of the flying capacitor and the switch driver.

First, the paper has shown that the bandwidth and transient response of the power mirror can be improved by employing an auxiliary current mirror, inserted in the input signal path of the main one. The auxiliary current mirror takes in the current provided by the transconductance error amplifier (OTA_EA) and supplies a gain-up version of it to the power mirror. This effectively amplifies the current available to charge the large parasitic capacitance of the power switch, yielding significantly larger bandwidth and faster transient response.

Second, it has shown a way to avoid the need of a power supply with fast response to load transients required by the conventional switch drivers. The idea is to power the core of the driver from an internal supply line with low-voltage and ordinary performance, while the output stage of the driver, which has to charge the large gate of the switch, is powered directly from the SC converter main input voltage. In this way, the current demand from the internal supply lines is reduced significantly. Moreover, this driver can be used for all voltage-controlled switches within an SC DC-DC converter, including the floating one(s). For the latter, a dedicated capacitive coupling arrangement was devised.

The main improvement at system-level was the introduction of a "Linear Regulator" mode of operation, whereby the power mirror is turned into a pass transistor and switching is disabled. Thus, the circuit operates as a linear regulator, able to maintain the output voltage at the wanted level even when the supply voltage drops to levels so low as to make switched-mode operation impossible.

The improvements described above were used to design and integrate in a 130nm BCD technology an automotive SC DC-DC converter. Simulation and measurement results presented in the paper demonstrate that it meets all design requirements: it provides a regulated 5V output voltage with less than 50mV ripple, for load currents up to 200mA, over a wide ranges of input voltage (from 8V to 28V) and temperature (from -40C to $+150$C) required by automotive applications. Moreover, the output voltage undershoot/ overshoot are maintained within 5.1% of the nominal output voltage for current load jump ratios as high as $IL_{MAX}/IL_{MIN} = 2000$.

The peak efficiency of the converter is 81.3% and is obtained for the typical battery voltage level, 12V.

The effectiveness of solutions proposed here for the SC DC-DC topology and circuit implementation was demonstrated:

- by using the "Linear Regulator" mode the input voltage range was extended down to 8V, while the switched-mode operation requires a minimum level of 11.5V.

- the improved power mirror has a bandwidth 11.5 times wider, and an $11.7\times$ faster transient response, than the conventional mirror. This helped reduce the minimum output capacitance the converter is stable for to 1μF. Even more importantly, it had a massive positive impact on the convertor transient performance: with only 1μF of output capacitance, the variations of the output voltage to load current steps as fast as 300ns remained within 5.1% of the nominal value. The output voltage ripple is reduced to 9mV when the output capacitance was increased to 10μF, less than half the ripple reported for converters that operate at similarly large input voltages and switching frequency and load capacitance.

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