A 529-μW Fractional-N All-Digital PLL Using TDC Gain Auto-Calibration and an Inverse-Class-F DCO in 65-nm CMOS

Peng Chen, *Member, IEEE*, Xi Meng, *Student Member, IEEE*, Jun Yin, *Member, IEEE*, Pui-In Mak, *Fellow, IEEE*, Rui P. Martins, *Fellow, IEEE*, and Robert Bogdan Staszewski, *Fellow, IEEE*

***Abstract*— This paper presents an ultra-lower-power (ULP) digital-to-time-converter (DTC)-assisted fractional-N all-digital phase-locked loop (ADPLL) suitable for IoT applications. A proposed hybrid time-to-digital converter (TDC) extends the vernier-TDC input range with little power overhead in order to overcome the stability issue in the conventional architectures. The hybrid TDC also facilitates a background gain calibration to achieve a stable in-band phase noise insensitive to process, voltage, and temperature (PVT) variations. The implementation of a buffer-cascaded DTC simplifies the design complexity of the fractional-N operation. The ADPLL also features a 200 μW low-phase-noise inverse-class-F (class-F^{-1}) digitally controlled oscillator (DCO) without the need of two-dimensional (2-D) capacitor tuning for frequency alignment of the fundamental and 2nd-harmonic. Fabricated in 65-nm CMOS, the ULP ADPLL prototype achieves 868 fs_{rms} jitter in a fractional-N channel when consuming only 529 μW, corresponding to a figure-of-merit (FoM) of −244 dB.**

***Index Terms*— ADPLL, Bluetooth LE (BLE), DCO, fractional-N PLL, phase noise (PN), TDC, DTC, inverse-class-F, low power, the IoT.**

Manuscript received February 15, 2021; revised May 4, 2021 and June 5, 2021; accepted June 23, 2021. Date of publication July 26, 2021; date of current version January 10, 2022. This work was supported in part by the Science Foundation Ireland under Grant 14/RP/I2921, in part by the Science and Technology Development Fund, Macau, under Grant 0044/2019/A1 and Grant SKL-AMSV(UM)-2020-2022, in part by the University of Macau under Grant MYRG2018-00220-AMSV, and in part by the National Science Center, Poland, under Contract UMO-2017/27/B/ST7/01217. This article was recommended by Associate Editor M. Onabajo. *(Peng Chen and Xi Meng contributed equally to this work.) (Corresponding author: Peng Chen.)*

Peng Chen was with the State-Key Laboratory of Analog and Mixed-Signal VLSI, Department of ECE, Faculty of Science and Technology, University of Macau, Taipa, Macau, and also with the School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, D04 V1W8 Ireland. He is now with Wuxi Grandmicro, Wuxi 214191, China (e-mail: peng.chen.1@ucdconnect.ie).

Xi Meng, Jun Yin, and Pui-In Mak are with the State-Key Laboratory of Analog and Mixed-Signal VLSI, Department of ECE, Faculty of Science and Technology, University of Macau, Taipa, Macau (e-mail: junyin@umac.mo).

Rui P. Martins is with the State-Key Laboratory of Analog and Mixed-Signal VLSI, Department of ECE, Faculty of Science and Technology, University of Macau, Taipa, Macau, on leave from the Instituto Superior Técnico, Universidade de Lisboa, 1649-004 Lisboa, Portugal.

Robert Bogdan Staszewski is with the School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, D04 V1W8 Ireland, and also with the Department of Measurement and Instrumentation, University of Science and Technology, 30-059 Krakow, Poland (e-mail: robert.staszewski@ucd.ie).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2021.3094094.

Digital Object Identifier 10.1109/TCSI.2021.3094094

I. Introduction

RECENT years have witnessed the rapid development of internet-of-things (IoT) underpinned by ultra-low power (ULP) short-range radios that can secure long battery life or can be directly powered by energy-harvesting sources. Bluetooth low energy (BLE) is currently the most popular IoT standard. A frequency synthesizer is one of the most power-hungry blocks in a typical BLE radio since it needs to be active both during the data reception and transmission [1]–[3]. Consequently, it is critical to minimize its power consumption while ensuring its stability and maintaining good phase noise (PN) with low spurious emissions.

Recent works in [4]–[16] have successfully demonstrated the advantages of fractional-N ADPLLs over their analog counterparts in reducing the power consumption while maintaining a competitive performance. By employing a digital-to-time converter (DTC)-assisted architecture proposed in [4] in order to narrow the phase error between the reference and the DCO output clocks, the input range of the following time-to-digital converter (TDC) can be substantially reduced, thus drastically improving the latter's power consumption and linearity. Since the DTC needs to generate a wide delay range covering the full oscillator period and to maintain good linearity to minimize fractional spurs, a relatively sizable power consumption is still typically required. Diverse techniques have been proposed to reduce the power and DTC nonlinearity in recent publications [17]–[20]. As a baseline, the DTC-TDC-based ADPLL in [4] achieved a worst-case fractional spur of −37 dBc and rms jitter of 1.71 ps while consuming 860 μW. Reference [5] proposed a phase dithering technique to scramble the DTC's integral nonlinearity (INL) and an extra reset operation inside the DTC to suppress the DTC memory effect. As a result, the worst-case fractional spur was reduced to −56 dBc with an rms jitter of 1.98 ps, while burning 670 μW. To further improve the INL of the DTC, a DAC-based constant-slope DTC architecture can be considered [6], [17], [21], [22]. In [6], the ADPLL using an isolated DAC-based constant-slope DTC with sub-1 ps INL achieves a worst-case fractional spur of −56 dBc and rms jitter of 0.53 ps, while consuming 980 μW, resulting in an excellent FoM of −246 dB. However, the DTC consumes a relatively large power of 142 μW, limited by its architecture. It also needs an additional bias pin for the current mirror.

After properly locking of a DTC-TDC-based ADPLL, its TDC's input detection range needs to theoretically cover only the quantization and thermal noise. Thus, its range and power consumption could be greatly lowered. However, the TDCs used in [4], [5] still cover a wide input range of around half the DCO period to help with shortening the settling time. This is because the narrow-range TDC may produce out-of-range detection values and exhibit a bang-bang behavior when the ADPLL first tries to lock. The need for a wide-range TDC to speed up the settling time in turn nullifies the power advantage offered by the DTC-assisted ADPLL architecture. In [5], a higher absolute digital value is assigned when the TDC output is out-of-range in order to reduce the settling time. However, that method exhibits a potential loop stability issue at a large loop bandwidth, as will be detailed in Section II. Moreover, what has not been appropriately addressed yet in [4]–[6] is that the TDC gain variation against PVT can induce variations in loop bandwidth and jitter. Unfortunately, the TDC gain variation cannot be detected and corrected together with the DTC gain calibration in the prior-art architectures. Hence, it is worthwhile to explore a solution that would automatically calibrate the TDC gain in the background.

On the DCO side, its PN is expected to deteriorate severely as its drawn power is reduced, thereby limiting the jitter performance of the ADPLL. A 2.4 GHz complementary class-B DCO in [6] achieves PN of −110 dBc/Hz at 1 MHz offset when consuming 210 μW, corresponding to a rather inferior FoM of 185 dB. Compared with the state-of-the-art LC VCOs that can achieve a high FoM of up to 197 dB [23]–[29], there is still plenty of room to improve the DCO PN at low power consumption. Furthermore, even though the oscillators using waveform-shaping techniques [24]–[28] can achieve high FoMs by exploiting the multiple-resonance properties provided by high-order LC tanks which rely on a precise alignment between the tank resonance frequencies and the harmonics of the fundamental resonance. In case of misalignment between the tank resonance frequencies, the optimal PN and FoM performance cannot be maintained. Thus, the existing oscillators using waveform-shaping techniques require independent tuning of multiple capacitor banks to guarantee the alignment between the resonance frequencies, which makes their performance sensitive to the PVT variations when integrated into a PLL.

In this work, we propose a hybrid TDC that extends the input range of a vernier-TDC with little power overhead by reusing one of its two delay chains as a flash-TDC. The hybrid architecture also permits a background gain calibration scheme, guaranteeing a constant TDC resolution over PVT variations. In contrast to the previous complex DTC designs, a conventional buffer-cascaded DTC is chosen to speed up the design process and satisfy the BLE standard for fractional spur requirements. Furthermore, a 200 μW class-F^{-1} DCO free of the 2nd-harmonic tuning is proposed to achieve a peak FoM of 196 dB at 1 MHz offset. The proposed DCO utilizes a transformer tank that automatically aligns the tank's 2nd-resonance with the 2nd-harmonic frequency, thus avoiding the multi-dimensional capacitor tuning required in the existing waveform-shaping oscillators.

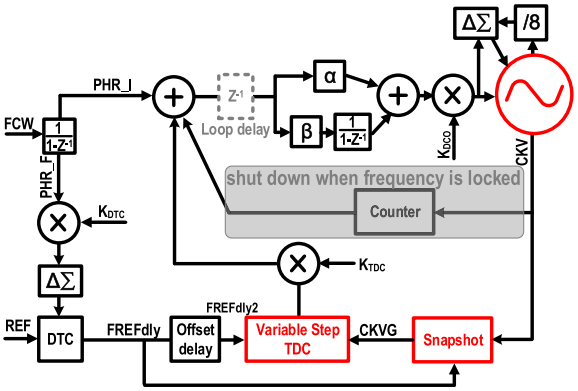


Fig. 1. Block-level system diagram of the proposed ADPLL based on a DTC-TDC phase prediction/detection and CKV counter.

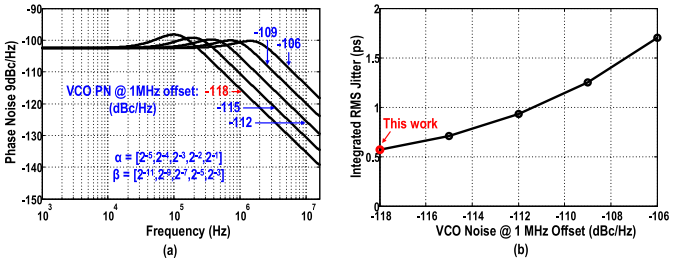


Fig. 2. (a) Optimum PLL PN with fixed noise on the reference path but different oscillator noise levels. The PLL bandwidth is adjusted in each case to achieve the minimum jitter. (b) Integrated PLL jitter versus oscillator noise level.

Figure 1 shows the top-level block diagram of the implemented ADPLL. The red blocks highlight the novel contributions of this work. Generally, the phase detection part consists of an integer path and a fractional path. The former is made up of a *reset-free* counter. The integer path is also (rather imprecisely) referred to as frequency locked-loop (FLL) in some publications, and it can be shut down after the frequency gets locked in order to stop unnecessarily burning power. For the fractional-N phase locking, the output from the combined DTC and TDC is used. With the help of phase prediction [30], a delayed version of the reference signal, i.e., FREF_{dly} is generated and its rising edge is aligned with the rising edge of the DCO output, CKV.

Various oscillators for BLE PLLs appear in the recent works [4]–[6], [31], [32]. Generally, jitter optimization can be achieved through minimizing the reference path noise *and/or* oscillator noise. This work chooses the latter option. Figure 2(a) plots the PN profile by applying various oscillators with different noise performance in the same ADPLL architecture of Fig. 1. To simplify the analysis, flicker noise upconversion in the oscillator, oscillator's quantization noise and flicker noise in the DTC are all ignored. The DTC's thermal noise floor is −155 dBc/Hz clocked at 32 MHz. The TDC with resolution of 7 ps is adopted for the model. By selecting the optimal bandwidth for the lowest jitter in each case, the total integrated rms jitter versus the oscillator performance is plotted in Fig. 2(b). It can be concluded that when the in-band PN is kept constant at around −103 dBc/Hz, by reducing the oscillator PN from −106 dBc/Hz to −118 dBc/Hz at 1 MHz offset, the integrated rms jitter can drop from 1.7 ps to 0.6 ps.

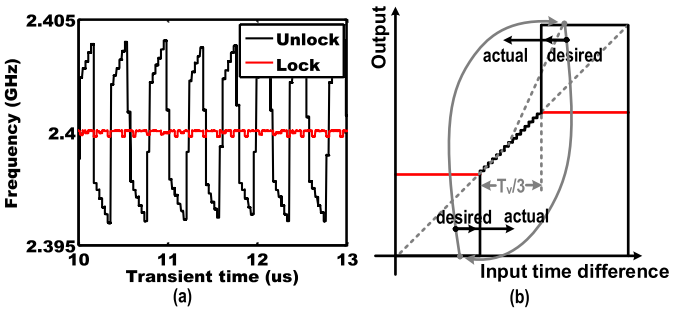


Fig. 3. Potential loop stability issue in face of a TDC out-of-range gain increase (black curves) when a wide loop bandwidth is employed: (a) PLL output frequency over time; (b) transfer function of TDC.

The rest of the paper is organized as follows. Section II introduces the hybrid TDC architecture and its calibration. The DTC with snapshot circuitry is described in Section III. Section IV presents the class-F^{-1} DCO free of the 2^{nd}-harmonic tuning. Experimental results are given in Section V.

II. Hybrid TDC

A. Stability Issue With Narrow-Range TDC

A design trade-off exists between the TDC range and settling time in the DTC-assisted ADPLL architecture. References. [5], [31] proposed enlarging the absolute values of TDC output when the input time difference is beyond the TDC detection range. That helps speeding up the settling behavior because the loop gain is also enlarged when the TDC input is out-of-range. However, that approach can exhibit an issue of loop stability when a wider loop bandwidth is employed. As Fig. 3(a) shows, when the normal loop bandwidth is comparable to the maximum allowable bandwidth of the PLL ($\sim$1/10 of reference frequency, [33]), enlarging the TDC output codes when out-of-range will reduce the loop phase margin, which can result in the PLL going out of lock. This can happen even when the FLL is always on, and it is independent of the TDC architecture.

To demonstrate this scenario, we examine the example below. Firstly, when optimizing the loop stability, the TDC transfer function should be centered in the middle of the phase detection window with the help of a tunable offset delay, as shown in Fig. 3(b). In this example, the TDC detection range covers 1/3 of the DCO period, T_v. The initial input time difference is assumed as $(1/6+\delta)T_V$ where δ is a vanishably small value. Then, the ideal TDC output corresponds to a time difference of $T_V/6$ as the red transfer function illustrates. However, with the transfer function of the enlarged out-of-range gain, as the black curve shows in Fig. 3(b), the TDC output corresponds to a time difference of $T_V/2$ which is $3\times$ larger than the desired value. The desired feedback force 'gently' drives the phase difference towards zero while the actual force is three times of the desired value in this example. The phase difference is over-pushed to the opposite direction, making the loop difficult to settle. From another perspective, the instant loop bandwidth is three times larger, resulting in an over-correction of the DCO frequency and the phase error. Therefore, the phase detection can manifest a bang-bang behavior, making it harder for the phase error to fall into the linear TDC detection range.

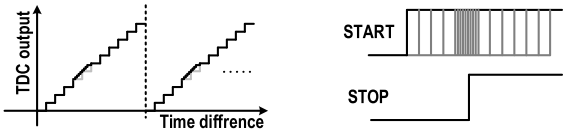


Fig. 4. Proposed idea of the TDC transfer function.

The behavioral model simulation confirms that the PLL cannot lock in this scenario of enlarging the TDC output code as per the black line indicated in Fig. 3(a), in which the bandwidth equals half of the maximum value. Otherwise, the PLL can still lock (red curve) although a long settling time is needed. It can be inferred that when the phase difference is out of the TDC range, it is better to add some coarse quantization steps to ease the trade-off between the settling time and stability.

It is noted that the trajectories in Fig. 3(a) are only for illustration purposes of Fig. 3(b). The actual phase error trajectory will be much more complex than just bouncing between the two levels. Increasing the TDC out-of-range gain is still helpful to overcome cycle slipping when small frequency disturbance occurs in the case of narrow loop bandwidth.

B. Proposed Hybrid TDC

To alleviate the above issue, the quantized phase error fed into the digital loop filter should be close to the actual phase error [34]. For the DTC-assisted ADPLL architecture, most of the delay stages in the TDC are not used when the loop is eventually locked [4]. Therefore, considering that the coarse quantization steps added beyond the fine TDC range are only utilized during the settling process, the coarse TDC's linearity and resolution requirements can be greatly relaxed. Figure 4 illustrates the concept of the TDC transfer function in this hybrid architecture. Coarse quantization steps extend the measurement range of the fine TDC. The wrapped phase generated by the snapshot circuit replicates the TDC transfer function along the x-axis at an interval of one oscillator period.

Figure 5(a) illustrates the schematic of the proposed hybrid TDC that embeds the above-mentioned coarse quantization function into a vernier TDC. The coarse quantization is realized by the flash TDC, which reuses the 'slow' path of the vernier TDC to save area and power. Specifically, during the TDC quantization, the first four delay stages in the slow path are re-used as an offset delay for the START signal. The vernier TDC highlighted in yellow contains eight unit stages, forming the fine 3-bit TDC quantization part. Regarding the coarse quantization, the flash TDC highlighted in gray is made up of twelve (4+8) slow stages and flip-flops. The last eight slow delay stages are shared with the vernier TDC. Therefore, the twelve thermometer codes from the flash TDC flip-flops represent the coarse quantization information. By adopting such an arrangement, the fine steps generated by the vernier TDC can be placed around the middle of the phase detection window, while the coarse steps generated by the flash TDC extend on both of its sides.

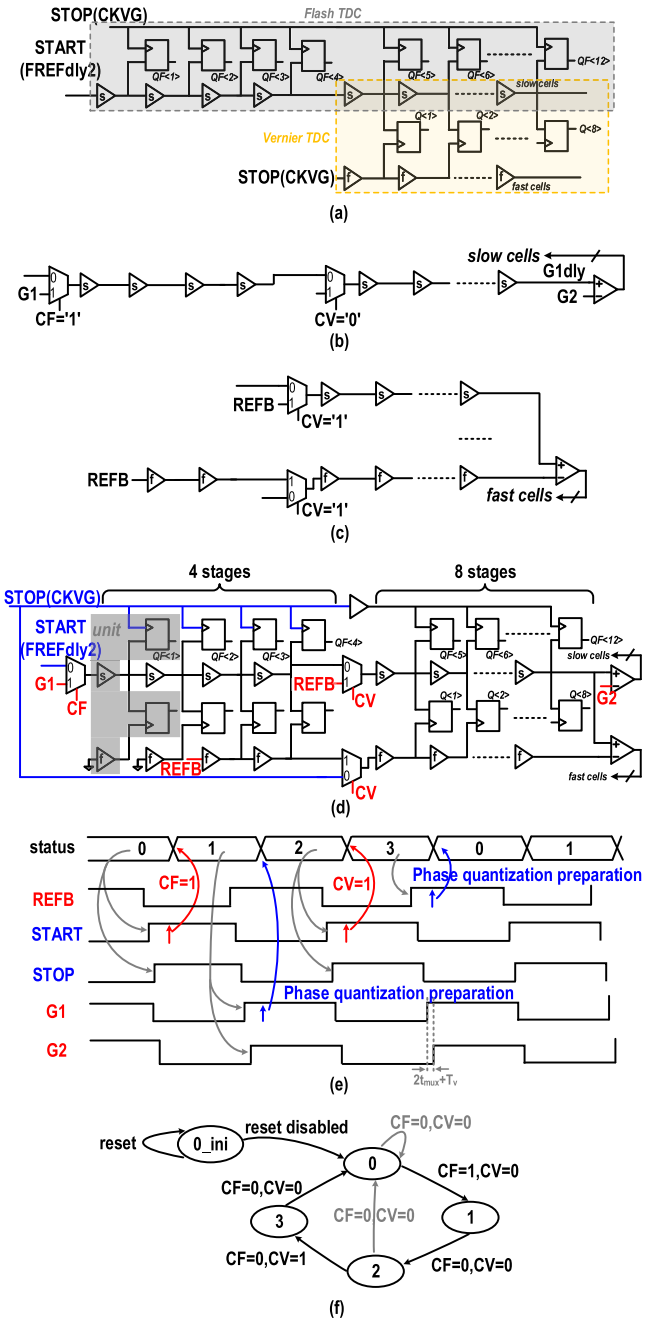


Fig. 5. Hybrid TDC: (a) effective cells in the TDC quantization mode, (b) effective cells in the flash TDC calibration mode, (c) effective cells in the vernier TDC calibration mode, (d) entire TDC schematic, (e) state transition of background TDC gain calibration, and (f) its state diagram.

C. TDC Gain Calibration

It is well known that the DTC gain K_{DTC} can be calibrated with the help of an LMS algorithm by correlating the detected phase error with the accumulated fractional value of the frequency control word PHR_F [4], [5], [35]. However, the calibration of the TDC gain K_{TDC} is difficult to perform by utilizing the current phase error information. When the ADPLL is locked, the integer phase error path always outputs zero and so the TDC gain parameter can be merged with the digital loop filter coefficients. Thus, the loop bandwidth can be affected by an error in the TDC gain. Alternatively, the TDC gain can be used to control the loop bandwidth [5]. In the applications where the bandwidth needs a precise control, the TDC gain should be calibrated. This would also benefit a fixed in-band noise floor if the in-band noise is determined by the TDC quantization error.

This architecture also facilitates the gain calibration of the vernier TDC. The target of the calibration is to match the total delay of the twelve slow stages with one oscillator period T_v; for simplicity, it is termed here a flash TDC calibration. Furthermore, the eight 'slow' stages and ten 'fast' (i.e. fine resolution) stages are expected to have the same delay, which is termed a vernier TDC calibration. The relationships can be expressed as follows:

$$12\Delta_s = T_v, \quad 8\Delta_s = 10\Delta_f$$
$$\Delta_{\mathrm{res}} = \Delta_s - \Delta_f = \frac{1}{60}T_v \tag{1}$$

where Δ_s and Δ_f denote the unit delay of slow and fast stages. Δ_{res} denotes the vernier TDC resolution. After the calibration, it is fixed to $\frac{1}{60}T_v$. To make the unit delay tunable, both slow (coarse) and fast (fine) stages are controlled by 6-bit variable loading capacitances. As Fig. 5(b) shows, in the flash TDC calibration mode, G1 rising edge is preset to lead G2 by $T_v + 2t_{\mathrm{mux}}$, where t_{mux} denotes the transition time through MUX. Consequently, $\mathrm{G1_{dly}}$ rising edge and G2 rising edge are expected to be aligned, generating an averaged value of zero from the comparator output if the comparator outputs are coded as '+1' and '−1'. Such averaged digital codes are intended to control the load capacitance of the slow stage. In the preset condition, the averaged zero comparator output will leave the loading of the slow stages untouched since (1) is satisfied. When the unit delay of the slow stage changes with PVT, the averaged comparator output can track this out and tune the loading of slow stages in an opposite direction. The vernier TDC calibration shown in Fig. 5(c) works using a similar principle. The two TDC calibration loops of flash and vernier TDC are intrinsically delay-locked loops (DLL).

The TDC phase detection mode works alternately with the gain calibration mode. Schematic of the entire TDC is shown in Fig. 5(d). In the phase detection mode, control signal CV for the vernier TDC calibration mode is disabled allowing START and STOP to propagate through the last eight stages and produce eight thermometer outputs. As for the coarse quantization, control signal CF for the flash TDC calibration is also disabled, allowing START signal to propagate through the first four stages.

This background calibration is carried out at the falling edge of the reference signal, reserving its rising edge for the conventional phase detection. The two calibration modes also work alternately. A finite state machine is adopted for the working mode shift, as shown by the timing diagram in Fig. 5(e) and the state diagram in Fig. 5(f).

In state *0* and *2*, the TDC works in the phase detection mode. After START signal rising edge passes all the slow delay units, it triggers the state switching, yielding CV = 1 or CF = 1. The phase detection information is not affected by the state switching since the TDC output thermometer codes would have already been stored in the flip-flops. In state *1*,

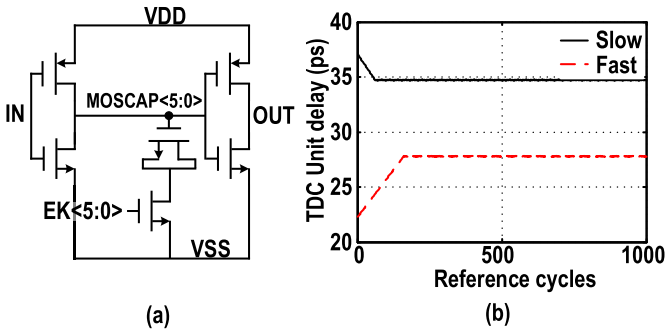


Fig. 6. (a) TDC slow/fast unit cell schematic, (b) TDC calibration settling behavior.

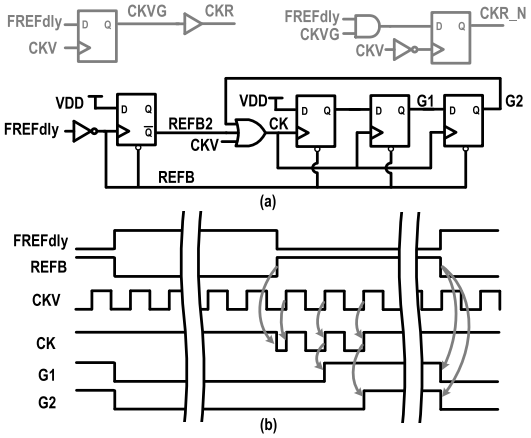


Fig. 7. Signal generation for TDC calibration in the snapshot.

the flash TDC calibration mode is enabled, yielding CV = 0 and CF = 1. After G1 propagates to the output of the last slow stage, state *2* is triggered entering the normal TDC phase detection state.

Similarly, in state *3*, vernier TDC calibration is achieved. After state *3*, the TDC working state enters *0*, starting another round of phase detection and calibration. It can be seen that since the calibrations work at the falling edges of START and STOP, the phase error information is still updated every reference cycle.

The schematic of the TDC fast and slow unit cells is shown in Fig. 6(a). Assuming the slow and fast delays suffer from random variations, its calibration settling behavior is plotted in Fig. 6(b).

The TDC gain calibration signals (G1 and G2) are generated by the circuit shown in Fig. 7(a). The rising edge difference between G1 and G2 is one DCO period. Before sending them to the TDC, G2 is delayed by extra two dummy muxes (not shown). Both G1 and G2's falling edges are reset by REFB's falling edge in preparation for the next cycle calibration. CK drives three flip-flops rather than two. Its waveform has three rising edges every reference period. The motivation is that when the PLL is in lock, the first rising edge could be in a meta-stable condition, deteriorating the timing information. The outputs from the second and third flip-flops are more stable, constraining the flash TDC range steadily. Since the high-frequency clock CKV only feeds into the *3OR* gate, G1 and G2 generation circuit consumes limited power.

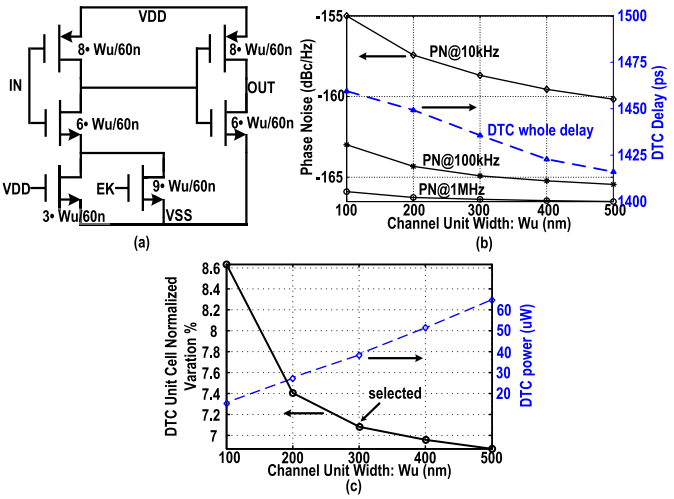


Fig. 8. (a) Schematic of the DTC unit cell. (b) Simulated overall PN and delay for different unit width W_u of transistors. (c) Simulated Monte-Carlo mismatch of the DTC unit cell across W_u.

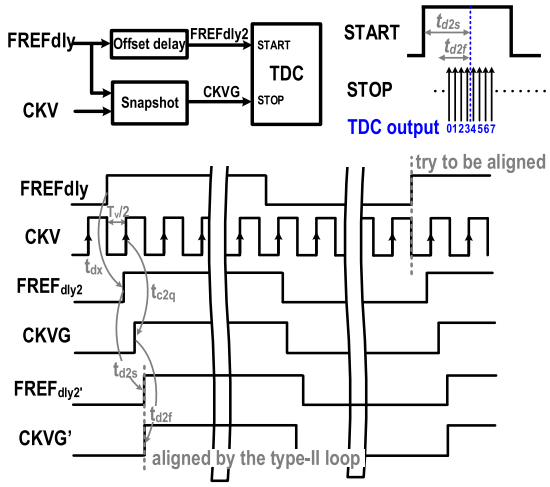


Fig. 9. Snapshot phase alignment.

III. DTC and Snapshot Circuit

A buffer-cascaded DTC is a conventional way to realize the controllable delay. We have demonstrated that a $\Delta\Sigma$ dithering approach in generating digital control codes for the DTC can effectively suppress the DTC quantization induced spurs [35]. However, this would not substantially help suppressing the spurs caused by the DTC nonlinearity. The nonlinearity of the buffer-based DTC mainly comes from the device mismatches. Larger sizes are adopted to reduce the statistical mismatch. A 4$\times$ power consumption can be traded for reducing the mismatch by only 2$\times$. The spur performance can be roughly improved by 6 dB.

Figure 8(a) shows the schematic of the DTC unit cell. Binary-valued EK signal is used to control the DTC unit delay by varying the discharging resistance in the first inverter. Figure 8(b) shows the PN and delay of the whole DTC chain across different W_u unit width values. Figure 8(c) plots the simulated Monte-Carlo mismatch. The overall DTC delay does not change dramatically when changing the transistor channel widths. The noise and process mismatch performance

inclines to be stable when the channel unit width is >300 nm. To balance the power consumption versus mismatch, a channel unit width of 300 nm is ultimately chosen.

The DCO output CKV is clock-gated at the reference rate before being fed into the TDC in order to save power by avoiding redundant transitions. The clock gated output must obviously retain the DCO rising edge information for phase detection. This is implemented by sampling the delayed reference signal FREF_{dly} with CKV in the snapshot block, as shown in Fig. 9. The sampling delay from CKV to CKVG, which is made up of a typical flip-flop clock-to-Q delay and the delay from several buffers connecting the snapshot block and TDC, is denoted as t_{c2q}. The sampled output (CKVG) is always behind FREF_{dly}. Therefore, we cannot directly feed FREF_{dly} into the TDC due to the fact that the TDC inputs are expected to have, on average, zero time difference when the PLL is locked in a type-II mode. An offset delay block is used to provide this extra delay, retarding FREF_{dly} to $\text{FREF}_{\text{dly2}}$ by t_{dx}. In [36], the above extra delay was also implemented by a DTC. However, most DTCs suffer from a constant offset delay which is usually at the same level as the DTC tuning range. Part of the constant offset also needs to be compensated in the CKVG path by inserting extra buffers. Those operations bring in unnecessary noise and power consumption before the critical signals are quantized by the TDC. Consequently, we desire the shortest offset delay, which can be roughly compensated without degrading the loop stability [37]. To overcome the PVT variations, but also for test purposes, a coarse tunable offset delay is adopted in this work. It features a large tuning range with a small constant offset but very coarse resolution.

The offset value calculation is illustrated in Fig. 9. CKVG and $\text{FREF}_{\text{dly2}}$ are the two inputs to the TDC. A 3-bit vernier TDC in this work is taken as an example. When the PLL is locked in type-II, the stop signal (CKVG) will catch the start signal's ($\text{FREF}_{\text{dly2}}$) rising edge at the 4th/5th unit stage, producing a decoded TDC output of 3 or 4. Inside the vernier TDC, CKVG goes through the fast delay cells and is delayed by t_{d2f} as CKVG′ to reach the 4th/5th unit stage. $\text{FREF}_{\text{dly2}}$ goes through the slow delay cells and is delayed by t_{d2s} as $\text{FREF}_{\text{dly2}'}$ to reach the 4th/5th unit stage. CKVG′ and $\text{FREF}_{\text{dly2}'}$ are forced aligned by the loop. t_{dx} denotes the offset delay to be calculated. It is desired that the TDC transfer function falls right in the middle of its detection window, as shown in Fig. 3(b). It corresponds to the scenario in which the CKV falling edge is aligned with the FREF_{dly} rising edge. This way, the CKV clock gating can stay far away from the metastability condition. In this case, the offset delay is expressed as

$$t_{dx} = T_v/2 + t_{c2q} + t_{d2f} - t_{d2s} \tag{2}$$

Based on post-layout simulations, it is 180 ps. The offset delay is made up of three different delay lines with MUX to select the appropriate one. The whole delay for the three paths is 110 ps, 180 ps and 270 ps, respectively.

IV. Digitally Controlled Oscillator

The class-F^{-1} oscillator in [26] maps the low (ω_L) and high (ω_H) resonant frequencies of the transformer tank to the fundamental (ω_{LO}) and 2nd-harmonic ($2\omega_{\text{LO}}$) frequencies of the oscillator, as illustrated in Fig. 10, which can effectively suppress the noise contribution from the negative g_m transistors. According to [24], [38], [39], [45], ω_L and ω_H can be expressed as

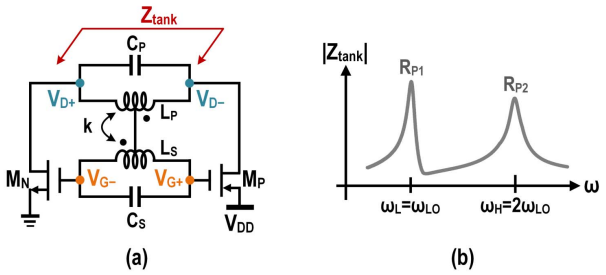


Fig. 10. Class-F^{-1} oscillator: (a) simplified schematic, and (b) amplitude of the tank impedance.

$$\begin{aligned}\omega_{L,H}^2 &= \frac{1+\xi \mp \sqrt{(1+\xi)^2 - 4\xi(1-k^2)}}{2(1-k^2)} \cdot \omega_2^2 \\ &= \Omega_{L,H}^2(\xi, k) \cdot \omega_2^2\end{aligned} \tag{3}$$

where k is the coupling coefficient, $\xi = L_S C_S / L_P C_P$ and $\omega_2 = 1/\sqrt{L_S C_S}$. To guarantee $\omega_H/\omega_L = 2$, the transformer tank needs to satisfy [26]:

$$16\xi^2 + (100k^2 - 68)\xi + 16 = 0 \tag{4}$$

Under the constrain of (4), the $\Omega_{H,L}$ in (3) can be simplified as,

$$\Omega_H = 2\Omega_L = \sqrt{\frac{5\xi}{1+\xi}} \tag{5}$$

Ref. [26] demonstrates that the high-Q impedance peaks at ω_{LO} and $2\omega_{\text{LO}}$ can be obtained by choosing a small k of 0.38 and a large ξ of 3, which enlarges 2nd-harmonic voltage and extends the flat span where the impulse sensitivity function (ISF) is minimum. Together with a high voltage gain from V_D to V_G provided by the transformer [Fig. 10(a)], the noise contributions from the negative g_m transistors are effectively suppressed. However, the PN and FoM of the class-F^{-1} oscillator heavily rely on the accurate alignment between ω_H and $2\omega_{\text{LO}}$. In [26], since a loosely coupled transformer with $k = 0.38$ and $\xi = 3$ is employed, ω_L mainly depends on C_S, while ω_H mainly depends on C_P. Thus, when the oscillation frequency ω_{LO} is tuned by varying C_S, ω_H stays mostly unmoved and deviates from the 2nd-harmonic frequency ($2\omega_{\text{LO}}$) of the oscillator. To align ω_H with $2\omega_{\text{LO}}$, C_P also needs to be appropriately changed. When implemented in a PLL, this 2-D capacitor tuning scheme is difficult to realize automatically. On the other hand, if we pre-design the C_S/C_P ratio through simulations for different frequencies, the performance of the class-F^{-1} oscillator will be sensitive to the process variation of the capacitors. According to Monte Carlo simulations, the 3σ capacitance variation of a 100-fF metal-oxide-metal (MOM) capacitor is ±15% in this 65 nm CMOS technology, which can cause a ξ variation from −26% to +35%. As illustrated by the simulation results in [26], if the C_S/C_P ratio deviates from the optimal value by 20%, the FoM

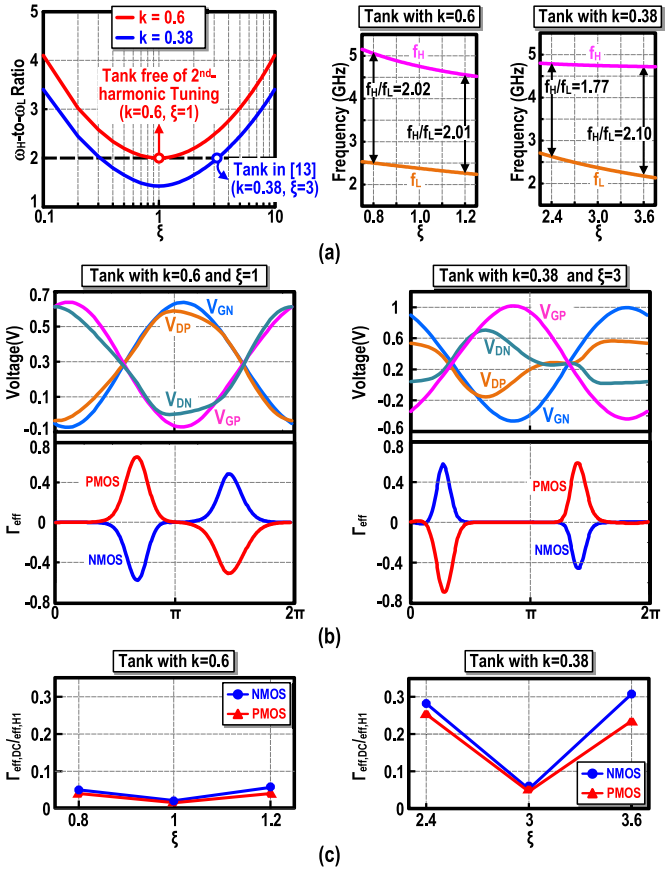


Fig. 11. (a) Relationship between ω_H/ω_L and ξ at different k. (b) Simulated voltage waveforms, effective ISFs of the NMOS and PMOS transistors. (c) $\Gamma_{\text{eff,DC}}/\Gamma_{\text{eff,H1}}$ for the class-F^{-1} oscillators using transformer tanks with $k = 0.6$ and 0.38.

at 100 kHz and 10 MHz will suffer from a considerable degradation of 6.7 and 3 dB, respectively, which is mainly caused by a large variation of the ω_H/ω_L ratio.

To avoid this troublesome 2-D capacitor tuning, it is preferred that both ω_L and ω_H can be simultaneously tuned when only C_S (or C_P) is changed. Intuitively, to make both ω_L and ω_H strongly dependent on C_S (or C_P), a tightly coupled transformer with a maximized k should be employed. Furthermore, if both ω_L and ω_H strongly depend on C_S, they must also strongly depend on C_P since the magnetic coupling between the primary and secondary coils is bidirectional, which implies choosing ξ close to 1. These assertions are also supported by theoretical analysis. Among all solutions of (4), the maximum k is 0.6, and the corresponding ξ is 1. As depicted in Fig. 11(a), when choosing $k = 0.38$ and $\xi = 3$, ω_H/ω_L will deviate from 2 by $+5/-7\%$ if ξ or C_s/C_p experiences a $\pm 20\%$ variation. To make ω_H/ω_L insensitive to the ξ variation, we can consider to use the transformer with $k = 0.6$ and $\xi = 1$. In this case, ω_H/ω_L only changes by $+1\%$ when ξ experiences the same $\pm 20\%$ variation. This insight inspires the development of a transformer tank emancipated from the 2$^{\text{nd}}$-harmonic tuning that can desensitize the PN and FoM from the capacitor mismatch.

Fig. 11(b) compares the simulated voltage waveforms and effective ISFs for the class-F^{-1} oscillators using transformers with $k = 0.6$ and $k = 0.38$. Here, the effective ISF is

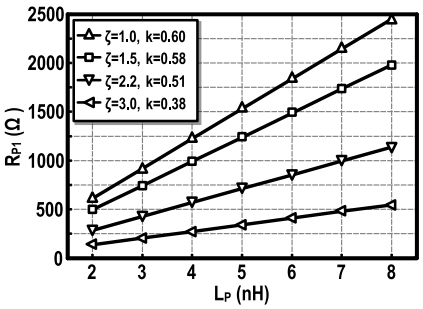


Fig. 12. Relationship between R_{P1} and L_P at different k and ξ ($Q_P = Q_S = 14$ and $\omega_{LO} = 2\pi \times 2.4$ GHz.).

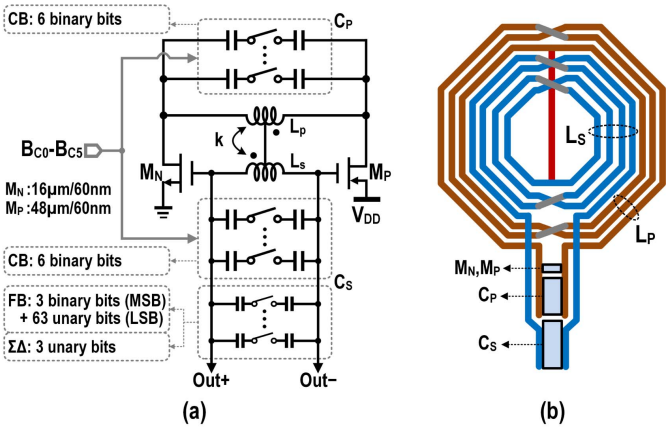


Fig. 13. Detailed schematic (a) and transformer layout (b) of the proposed ULP class-F^{-1} DCO.

defined as $\Gamma_{\text{eff}}(\omega_0\, t) = \Gamma_{\text{MOS}}(\omega_0\, t) \cdot g_m(\omega_0\, t)/g_{\text{m,max}}$, where $\Gamma_{\text{MOS}}(\omega_0\, t)$ and g_m represent the ISF and transconductance of the MOS transistor, respectively. According to [40], the ratio between the $1/f^3$ PN corner and transistor flicker noise corner is proportional to $(\Gamma_{\text{eff,DC}}/\Gamma_{\text{eff,H1}})^2$ where $\Gamma_{\text{eff,DC}}$ and $\Gamma_{\text{eff,H1}}$ are the dc and first harmonic amplitude of Γ_{eff}. Thus, the flicker noise upconversion can be effectively suppressed if $\Gamma_{\text{eff,DC}}$ is close to zero. Fig. 11(b) indicates that the Γ_{eff} waveform is symmetric and so $\Gamma_{\text{eff,DC}}$ is small for the class-F^{-1} oscillators using both tanks when $\omega_H/\omega_L = 2$. This consequently verifies that the 2$^{\text{nd}}$-harmonic resonance helps to suppress the flicker noise upconversion, resulting in a low $1/f^3$ PN corner. Fig. 11(c) plots the calculated $\Gamma_{\text{eff,DC}}/\Gamma_{\text{eff,H1}}$ of the NMOS and PMOS transistors versus ξ. When ξ deviates from the optimal values by $\pm 20\%$, $\Gamma_{\text{eff,DC}}/\Gamma_{\text{eff,H1}}$ soars to 0.31 when using the tank with $k = 0.3$, while it is still suppressed to lower than 0.06 when $k = 0.6$. Therefore, the ISF analysis confirms that the $1/f^3$ PN corner is insensitive to ξ variation when using the tank with $k = 0.6$.

To secure a low power consumption, the tank's parallel impedance R_{P1} at ω_{LO} needs to be maximized. Under the constrain of (4), R_{P1} can be obtained as

$$R_{P1} = \frac{16\omega_{LO} L_P Q_P}{25} \cdot \frac{(1+\xi)^2 \cdot (4-\xi)}{4\xi^2(\frac{Q_P}{Q_S}) - \xi(1+\frac{Q_P}{Q_S}) + 4} \quad (6)$$

At a certain oscillation frequency ω_{LO}, R_{P1} only depends on L_P, ξ, Q_P, and Q_P/Q_S. Assuming $Q_P = Q_S = 14$

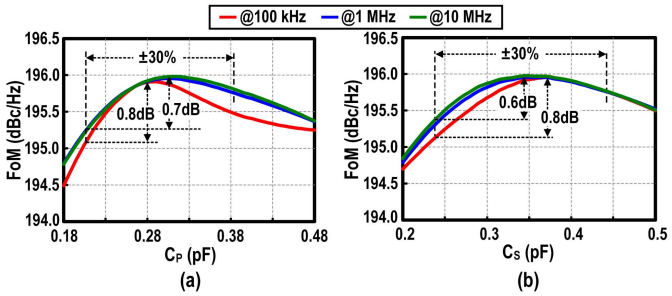


Fig. 14. Simulated FoMs against capacitor variations of (a) C_P and (b) C_S.

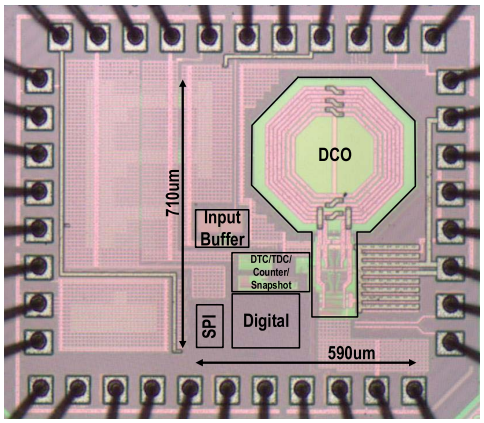


Fig. 15. Chip microphotograph of the proposed ULP ADPLL.

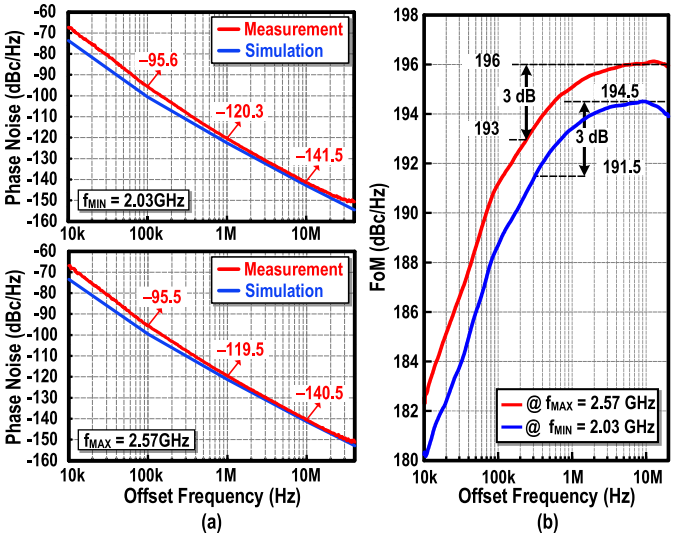


Fig. 16. (a) Simulated and measured PN profiles, and (b) measured $1/f^3$ PN corners of the DCO at $f_{\mathrm{MIN}} = 2.03\,\mathrm{GHz}$ and $f_{\mathrm{MAX}} = 2.57\,\mathrm{GHz}$.

for simplicity, Fig.12 shows that choosing a large L_P and a small ξ helps to enlarge R_{P1}. Thus, our transformer tank employing a minimum ξ of 1 not only desensitizes ω_H/ω_L from the capacitor mismatch but also secures the lowest power consumption.

Furthermore, for the resonance at ω_{LO}, the quality factor Q_1 of the transformer tank can be larger than Q_P and Q_S since the magnetic flux coupled from L_S increases the magnetic energy stored in the tank. According to [38], the transformer tank

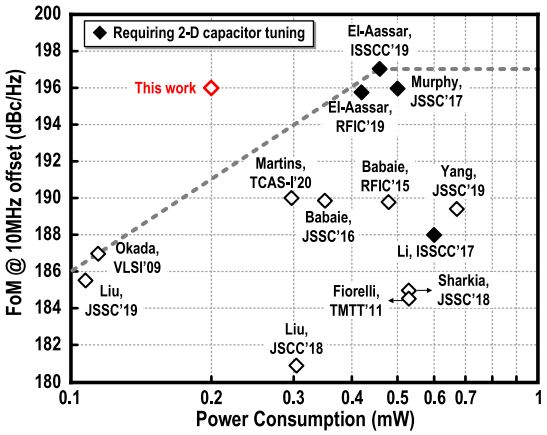


Fig. 17. FoM comparison with state-of-the-art low-power LC oscillators. The oscillator FoM is defined in Table I.

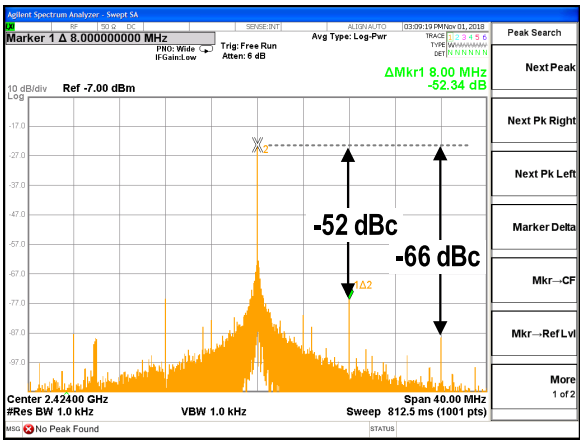


Fig. 18. Measured fractional & reference spurs at one BLE channel.

with large k can benefit from the high Q_1/Q_P ratio. Since our tank uses the peak k of 0.6 to guarantee $\omega_H/\omega_L = 2$, Q_1 is maximized. On the other hand, as pointed out by [26], using the large k and small ξ tends to reduce the tank's quality factor Q_2 at $2\omega_{LO}$ and the voltage gain from V_D to V_G. As a result, the noise contributions from the negative g_m transistors increase, degrading the FoM of the class-F^{-1} oscillator. Fortunately, the enhanced Q_1 mitigates the PN degradation due to the reduced Q_2 and the voltage gain. Therefore, a high peak FoM can still be maintained in the ULP class-F^{-1} oscillator with the natural 2$^{\mathrm{nd}}$-harmonic alignment.

Fig. 13(a) depicts the detailed schematic of the proposed class-F^{-1} DCO. Two identical switched-capacitor (SC) banks for coarse frequency tuning (CB) are implemented at both primary and secondary coils and are controlled by the same digital bits ($B_{C0}-B_{C5}$). Since the DCO performance is insensitive to the capacitor mismatch between C_P and C_S, the SC banks for the fine frequency tuning (FB) and $\Sigma\Delta$ modulation are only placed in the secondary coil for a simple and compact layout. We tailor a 3-to-4-turn transformer with $L_P = 7\,\mathrm{nH}$ and $L_S = 8\,\mathrm{nH}$ to maintain high Q-factors for both coils ($Q_P = 14.5$ and $Q_S = 16.6$), as shown in Fig. 13(b). This tightly-coupled transformer ($k = 0.6$) also saves the die area compared with the designs in [25] and [26]

TABLE I

PERFORMANCE SUMMARY AND COMPARISON OF THE PROPOSED DCO WITH STATE-OF-THE-ART

		RFIC15 [41] Babaie	JSSC17 [25] Murphy	JSSC19 [32] Liu	ISSCC19 [27] Aassar		RFIC19 [28] Aassar		TCAS-I20 [42] Martins		This Work	
Topology		Switching Current Source	CMOS CM Resonance	Stacked-gm	Folded, 4-Winding xfmr		CMOS 4-Port xfmr Resonator		CMOS Class-B/C Hybrid-Mode		Class-F^{-1} + xfmr Tank Free of 2nd -Harmonic Tuning	
2-D Capacitor Tuning?		No	Yes	No	Yes		Yes		No		**No**	
Supply (V)		0.5	0.7	0.45	0.1		0.35		0.8		0.55	
Freq. Range (GHz)		4.0-5.03 (22.2%)	4.7-5.4 (13.8%)	2.1-3.1 (38.5%)	4.15-4.97 (18%)		4.06-4.96 (20%)		4.2-5.1 (19%)		2.03-2.57 (23.8%)	
Freq. (GHz)		5.03	5.3	2.46	4.15	4.97	4.06	4.96	4.2	5.1	2.03	2.57
Power (uW)		470	500	107	540	460	440	420	349	297	**205**	**183**
PN (dBc/Hz)	100k	-85.1	-92*	NA	-91.3	-92.3	-93.1	-91.6	-84.3	-86.1	-95.6	-95.5
	10M	-132.7*	-138*	-128	-133	-136.5	-136	-137.8	-126.7	-130.6	-141.5	-140.5
FoM** (dBc/Hz)	100k	182.4	189.5	NA	186.4	189.6	189	189.2	181.3	185.4	**188.6**	**191**
	10M	190	195.5	185.5	188	193.7	192	192.5	183.7	190.0	**194.5**	**196**
$1/f^3$ corner (kHz)		250-420	200	NA	50-180		100-250		70	150	300	250
Freq. Pushing (MHz/V)		17	NA	NA	40		80		-12	-91	56	27
CMOS Tech. (nm)		40	28	65	22 FDSOI		22 FDSOI		65		65	
Core Area (mm^2)		0.14	0.18	0.25	0.27		0.19		0.165		0.22	

*Estimated from the PN plot. **$\mathrm{FoM} = \mathrm{PN} - 20\log_{10}(\omega_{\mathrm{LO}}/\Delta\omega) + 10\log_{10}(P_{\mathrm{DC}}/1\mathrm{mW})$

TABLE II

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ULP ADPLLS

	ISSCC14 [4] Chillara	ISSCC17 [5] He	JSSC18 [6] Liu	JSSC19 [32] Liu	JSSC18 [43] Pourmousavian	This Work
CMOS Process (nm)	40	40	65	65	28	65
Reference (MHz)	32	NA	52	10	40	32
Frequency Range (GHz)	2.1-2.7	1.8-2.5	2.0-2.8	2.1-3.1	2.1-2.6	1.9-2.6
Power (mW)	0.86	0.67	0.98	0.27	1.6	0.53
Jitter (ps)	1.71	1.98	0.53	2.8	0.86	0.87
Integration BW	1k-100M	10k-10M	10k-10M	1k-40M	10k-10M	10k-10M
Frac. Spur (dBc)	-38	-56	-56	-52	-57	-50
Ref. Spur (dBc)	-70*	-62	-72	NA	-78	-66
FoM (dB)	-236	-236	-246	-237	-239	-244
Area (mm^2)	0.20	0.18	0.60**	0.25	0.33	0.42

*Estimated from the author's Master thesis [44].
**Estimated from the chip photo.

that use loosely-coupled transformers ($k < 0.4$). Simulation results in Fig. 14 verify that the class-F^{-1} oscillator with the natural 2nd-harmonic alignment can maintain a high peak FoM of 196 dB. Even when C_P or C_S changes by $\pm 30\%$ from its optimal value, the FoM degradation is <0.8 dB (<0.7 dB) at the 100 kHz (10 MHz) offset frequency.

V. MEASUREMENT RESULTS

The presented ultra-low-power ADPLL was implemented in 65-nm bulk CMOS. The chip photo is shown in Fig. 15. The core area is 0.42 mm^2.

The open-loop performance was measured by Agilent E5052B Signal Source Analyzer. The sizes of the g_m transistors in the DCO are 16 μm/0.06 μm (NMOS) and 48 μm/0.06 μm (PMOS). The measured PN at 2.03 GHz (f_{MIN}) and 2.57 GHz (f_{MAX}) when $V_{\mathrm{DD}} = 0.55$ V is shown in Fig. 16. The corresponding FoM at 10 MHz offset slightly drops from 196 dB (f_{MAX}) to 194.5 dB (f_{MIN}) due to the extra tank loss from the SCAs when more switches are turned on. The measured $1/f^3$ PN corners are 250 kHz (f_{MAX}) and 300 kHz (f_{MIN}). Fig. 16(a) also compares the measured PN with the simulated one. The discrepancy at the low offset frequencies is likely due to the flicker noise of the transistor in the triode region not being accurately modeled. We also measured PN and FoM performance across the frequency tuning range as well as its power consumption and $1/f^3$ PN corner over 5 samples. The chip-to-chip variation of the FoM between the 100 kHz to 10MHz offsets is <1 dB, and the worst-case $1/f^3$ PN corner is <400 kHz. The frequency pushing is <4 MHz/V at f_{MIN} and <44 MHz/V at f_{MAX} when

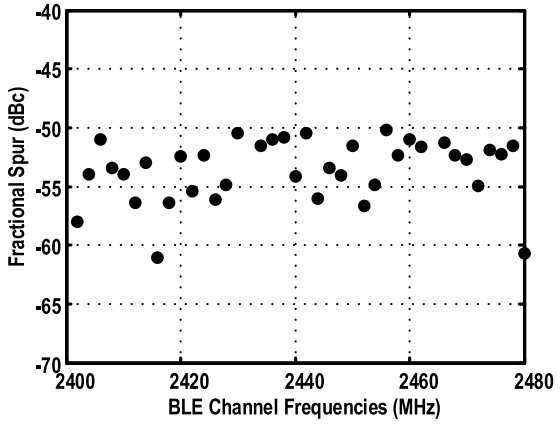


Fig. 19. Measured fractional spurs at BLE channels.

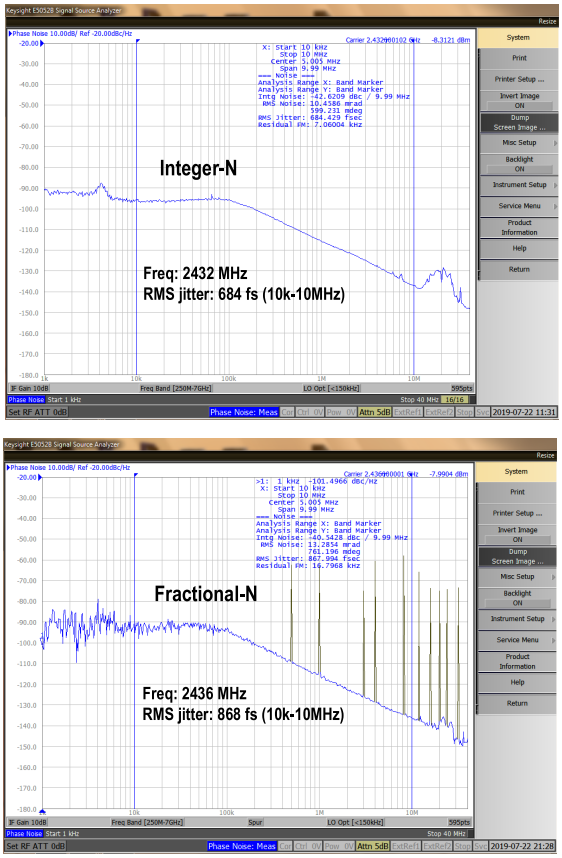


Fig. 20. Measured PN plots at integer & fractional channels.

V_{DD} changes from 0.55 to 0.65 V. This verifies the robustness of the proposed oscillator that is free from the 2nd-harmonic tuning. Benchmarked with other recently reported low-power VCOs and DCOs shown in Fig. 17 and Table I, our class-F^{-1} DCO retains a high peak FoM of 196 dB with a low power consumption of 200 μW without the need of the complicated 2-D capacitor tuning.

The closed-loop measurements cover the spectrum and PN. A 32 MHz reference signal is used. The measured reference and fractional spurs at one BLE channel are shown in Fig. 18. Without the power-hungry IIR filters, the spur performance

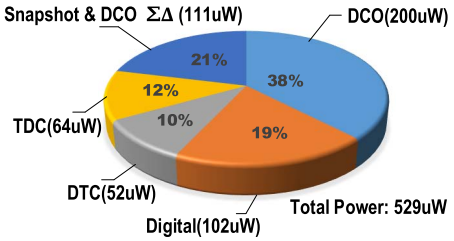


Fig. 21. Measured power breakdown of the proposed ADPLL.

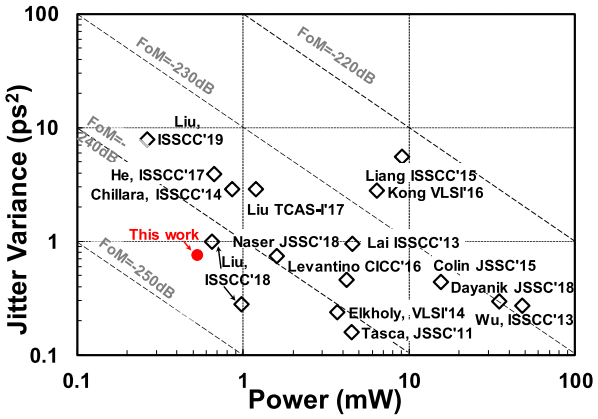


Fig. 22. FoM comparison with state-of-the-art fractional-N ADPLLs.

still satisfies the BLE requirements. Sweeping all BLE channels from 2400 to 2480 MHz, the fractional spur at 2 MHz offset is within −50 dBc, as shown in Fig. 19.

The measured PN [1] of the integer-N and fractional-N channels are plotted in Fig. 20. Integrated from 10 kHz to 10 MHz, the rms jitter in an integer-N mode is 684 fs, corresponding to an FoM of -246 dB. The integrated jitter in a fractional-N mode is 868 fs, corresponding to an FoM of −244 dB. The in-band noise floor is a bit higher than expected, degraded by the reference signal quality and supply noise of the phase detection blocks.

The detailed power consumption of each building block is shown in Fig. 21. The total power consumption is 529 μW with analog and digital blocks operating at 0.9 V, and the DCO operating at 0.6 V.

The FoM comparison is surveyed in Fig. 22. It indicates a competitive performance of the proposed design among the ultra-low-power ADPLLs.

VI. Conclusion

This work demonstrated a sub-mW DTC-assisted ADPLL featuring an ultra-lower-power fractional-N operation for BLE applications. The proposed hybrid architecture of flash- and vernier- TDC extends the input range of the vernier-TDC with little power overhead. The function-reuse TDC also facilitates the background gain calibration scheme to obtain a stable bandwidth insensitive to the PVT variations. The ADPLL

[1]The noise peaking around 20 MHz in the PN appears randomly and the root reason is not very clear. We suspect this could be due to WiFi or cellular interference.

features a low-phase-noise 200 μW inverse-class-F DCO without requiring 2-D capacitor tuning. Fabricated in 65-nm CMOS, the ULP ADPLL prototype achieves sub-1 ps_{rms} jitter while consuming 529 μW, corresponding to a figure-of-merit of -244 dB.

ACKNOWLEDGMENT

The authors would like to thank Haidong Yi and Wei-Han Yu for the layout and measurement assistance, Lianbo Wu and Zhirui Zong for the technical discussions.

REFERENCES

[1] M. Babaie *et al.*, "A fully integrated Bluetooth low-energy transmitter in 28 nm CMOS with 36% system efficiency at 3 dBm," *IEEE J. Solid State Circuits*, vol. 51, no. 7, pp. 1547–1565, Jul. 2016.

[2] S. Yang, J. Yin, H. Yi, W.-H. Yu, P.-I. Mak, and R. P. Martins, "A 0.2-V energy-harvesting BLE transmitter with a micropower manager achieving 25% system efficiency at 0-dBm output and 5.2-nW sleep power in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1351–1362, May 2019.

[3] F. W. Kuo *et al.*, "A 0.5 V 1.6 mW 2.4 GHz fractional-N all-digital PLL for Bluetooth LE with PVT-insensitive TDC using switched-capacitor doubler in 28-nm CMOS," in *Proc. IEEE Symp. VLSI Circuits (VLSIC)*, Jun. 2017, pp. 178–179.

[4] V. K. Chillara *et al.*, "9.8 An 860μW 2.1-to-2.7GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth smart and ZigBee) applications," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2014, pp. 172–173.

[5] Y. He *et al.*, "24.7 A 673μW 1.8-to-2.5GHz dividerless fractional-N digital PLL with an inherent frequency-capture capability and a phase-dithering spur mitigation for IoT applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 420–421.

[6] H. Liu *et al.*, "A sub-mW fractional-N ADPLL with FOM of –246 dB for IoT applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3540–3552, Dec. 2018.

[7] X. Gao *et al.*, "9.4 A 28nm CMOS digital fractional-N PLL with –245.5dB FOM and a frequency tripler for 802.11abgn/AC radio," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 166–167.

[8] X. Gao *et al.*, "A 2.7-to-4.3GHz, 0.16 ps_{rms}-jitter, -246.8dB-FoM, digital fractional-N sampling PLL in 28nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2016, pp. 174–175.

[9] S. Levantino, G. Marzin, and C. Samori, "An adaptive pre-distortion technique to mitigate the DTC nonlinearity in digital PLLs," *J. Solid-State Circuits*, vol. 49, no. 8, p. 1762–1772, Aug. 2014.

[10] A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly, and P. K. Hanumolu, "A 3.7 mW low-noise wide-bandwidth 4.5 GHz digital fractional-N PLL using time amplifier-based TDC," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 867–881, Apr. 2015.

[11] C.-W. Yao *et al.*, "A 14-nm 0.14-ps_{rms} fractional-N digital PLL with a 0.2-ps resolution adc-assisted coarse/fine-conversion chopping TDC and TDC nonlinearity calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3446–3457, Dec. 2017.

[12] W.-S. Chang, P.-C. Huang, and T.-C. Lee, "A fractional-N divider-less phase-locked loop with a subsampling phase detector," *IEEE J. Solid State Circuits*, vol. 49, no. 12, p. 2964–2975, Dec. 2014.

[13] R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*, 1st ed. New York, NY, USA: Wiley, 2006.

[14] H. Afzal, R. Abedi, R. Kananizadeh, P. Heydari, and O. Momeni, "An mm-Wave scalable PLL-coupled array for phased-array applications in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 2, pp. 1439–1452, Feb. 2021.

[15] N. Markulic *et al.*, "A DTC-based subsampling PLL capable of self-calibrated fractional synthesis and two-point modulation," *IEEE J. Solid State Circuits*, vol. 51, no. 12, pp. 3078–3092, Dec. 2016.

[16] T. Siriburanon *et al.*, "A low-power low-noise mm-Wave subsampling PLL using dual-step-mixing ILFD and tail-coupling quadrature injection-locked oscillator for IEEE 802.11ad," *IEEE J. Solid State Circuits*, vol. 51, no. 5, p. 1246–1260, May 2016.

[17] P. Chen, F. Zhang, Z. Zong, H. Zheng, T. Siriburanon, and R. B. Staszewski, "A 15-μW, 103-fs step, 5-bit capacitor-DAC-based constant-slope digital-to-time converter in 28nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2017, pp. 93–96.

[18] C.-R. Ho *et al.*, "A fractional-N DPLL with calibration-free multi-phase injection-locked TDC and adaptive single-tone spur cancellation scheme," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 8, pp. 1111–1122, Aug. 2016.

[19] C.-R. Ho and M. S.-W. Chen, "A digital PLL with feedforward multi-tone spur cancellation loop achieving <-73dBc fractional spur and <-110dBc reference spur in 65nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3216–3230, Dec. 2016.

[20] R. Avivi *et al.*, "Adaptive spur cancellation technique in all-digital phase-locked loops," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 11, pp. 1292–1296, Nov. 2017.

[21] J. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink, and B. Nauta, "A high-linearity digital-to-time converter technique: Constant-slope charging," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1412–1423, Jun. 2015.

[22] P. Chen, F. Zhang, Z. Zong, S. Hu, T. Siriburanon, and R. B. Staszewski, "A 31-μW 148-fs step 9-bit capacitor-DAC-based constant-slope digital-to-time converter in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3075–3085, Nov. 2019.

[23] E. Hegazi, H. Sjöland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.

[24] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[25] D. Murphy, H. Darabi, and H. Wu, "Implicit common-mode resonance in LC oscillators," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 812–821, Mar. 2017.

[26] C.-C. Lim, H. Ramiah, J. Yin, P.-I. Mak, and R. P. Martins, "An lnverse-class-F CMOS oscillator with intrinsic-high-Q first harmonic and second harmonic resonances," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3528–3593, Dec. 2018.

[27] O. El-Aassar and G. M. Rebeiz, "26.5 A 0.1-to-0.2 V transformer-based switched-mode folded DCO in 22nm FDSOI with active step-down impedance achieving 197dBc/Hz peak FoM and 40MHz/V frequency pushing," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 416–418.

[28] O. El-Aassar and G. M. Rebeiz, "A 350 mV complementary 4-5 GHz VCO based on a 4-Port transformer resonator with 195.8dBc/Hz peak FOM in 22nm FDSOI," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 159–162.

[29] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

[30] J. Zhuang and R. B. Staszewski, "Gain estimation of a digital-to-time converter for phase-prediction all-digital PLL," in *Proc. Eur. Conf. Circuit Theory Design (ECCTD)*, Sep. 2013, pp. 1–4.

[31] Y.-H. Liu *et al.*, "An ultra-low power 1.7-2.7 GHz fractional-N subsampling digital frequency synthesizer and modulator for IoT applications in 40 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 5, pp. 1094–1105, May 2017.

[32] H. Liu *et al.*, "A 265 μW fractional-N digital PLL with seamless automatic switching subsampling/sampling feedback path and duty-cycled frequency-locked loop in 65nm CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3478–3492, Dec. 2019.

[33] F. Gardner, "Charge-pump phase-lock loops," *IEEE Trans. Commun.*, vol. COM-28, no. 11, pp. 1849–1858, Nov. 1980.

[34] L. Bertulessi, L. Grimaldi, D. Cherniak, C. Samori, and S. Levantino, "A low-phase-noise digital bang-bang PLL with fast lock over a wide lock range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 252–253.

[35] Z. Zong, P. Chen, and R. B. Staszewski, "A low-noise fractional-*N* digital frequency synthesizer with implicit frequency tripling for mm-Wave applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 755–767, Mar. 2019.

[36] Y.-H. Liu, "All-digital-phase-locked-loop having a time-to-digital converter circuit with a dynamically adjustable offset delay," U.S. Patent 9 774 336 B2, Dec. 20, 2015.

[37] Y. Wu, M. Shahmohammadi, Y. Chen, P. Lu, and R. B. Staszewski, "A 3.5–6.8-GHz wide-bandwidth DTC-assisted fractional-N all-digital PLL with a MASH $\Delta\Sigma$-TDC for low in-band phase noise," *J. Solid-State Circuits*, vol. 52, no. 7, pp. 1885–1903, Jul. 2017.

[38] A. Mazzanti and A. Bevilacqua, "On the phase noise performance of transformer-based CMOS differential-pair harmonic oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2334–2341, Sep. 2015.
[39] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 4, pp. 293–297, Apr. 2007.
[40] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
[41] M. Babaie, M. Shahmohammadi, and R. B. Staszewski, "A 0.5 V 0.5 mW switching current source oscillator," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2015, pp. 183–186.
[42] R. Martins *et al.*, "Design of a 4.2-to-5.1 GHz ultralow-power complementary class-B/C hybrid-mode VCO in 65-nm CMOS fully supported by EDA tools," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 11, pp. 3965–3977, Nov. 2020.
[43] N. Pourmousavian *et al.*, "A 0.5-V 1.6-mW 2.4-GHz fractional-N all-digital PLL for Bluetooth LE with PVT-insensitive TDC using switched-capacitor doubler in 28-nm CMOS," *IEEE J. Solid State Circuits*, vol. 53, no. 9, pp. 2572–2583, Sep. 2018.
[44] V. K. Chillara, "An ultra-low-power ADPLL for WPAN applications," M.S. thesis, Dept. Microelectron., Delft Univ. Technol., Delft, The Netherlands, Nov. 2013. [Online]. Available: http://resolver.tudelft.nl/uuid:53911767-cf72-4441-885b-d3dc6b7949d8
[45] M. Shahmohammadi, M. Babaie, and R. B. Staszewski, "Tuning range extension of a transformer-based oscillator through common-mode Colpitts resonance," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 836–846, Apr. 2017.

Peng Chen (Member, IEEE) received the B.Sc. degree in electronics from the Huazhong University of Science and Technology, Wuhan, China, in 2012, the M.Sc. degree in microelectronic from the Delft University of Technology (TU Delft), Delft, The Netherlands, in 2014, and the Ph.D. degree from University College Dublin in 2019.

His M.Sc. thesis was done with the IMEC Holst Center, Eindhoven, The Netherlands. From 2014 to 2015, he worked as a Test Manager with Huawei Technologies, Amsterdam. From 2017 to 2018, he was a Visiting Research Assistant with the University of Macau. From 2019 to 2021, he was a Post-Doctoral Researcher with Lund University. He is currently with Wuxi Grandmicro, China. His research interests include time domain data converters, frequency synthesizers, and wideband receiver.

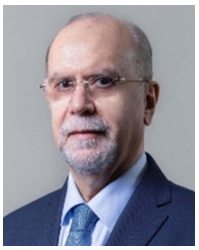
Xi Meng (Student Member, IEEE) received the B.Sc. degree in integrated circuit design and integration system from Xidian University, Xi'an, China, in 2016. She is currently pursuing the Ph.D. degree in electronic and computer engineering with the University of Macau, Taipa, Macau. Her research interests include CMOS analog and RF integrated circuits and systems for wireless applications.

Jun Yin (Member, IEEE) received the B.Sc. and M.Sc. degrees in microelectronics from Peking University, Beijing, China, in 2004 and 2007, respectively, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology (HKUST), Hong Kong, in 2013. He is currently an Associate Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau (UM), Macau. His research interests include the CMOS RF integrated circuits for wireless communications and wireless sensing systems, specializing in the frequency generation and synthesis circuits, including oscillators and PLLs.

Pui-In Mak (Fellow, IEEE) received the Ph.D. degree from the University of Macau (UM), Macau, in 2006.

He is currently a Full Professor with the ECE Department, Faculty of Science and Technology, UM. He is the Associate Director (research) with the Institute of Microelectronics, UM, and the State Key Laboratory of Analog and Mixed-Signal VLSI. His research interests include analog and radio-frequency (RF) circuits and systems for wireless and multidisciplinary innovations.

Dr. Mak was a TPC member of A-SSCC from 2013 to 2016 and in 2019, ESSCIRC from 2016 to 2017, and ISSCC from 2017 to 2019. He has been a fellow of the U.K. Institution of Engineering and Technology (IET) for contributions to engineering research, education, and services, since 2018. Since 2019, he has been also a fellow of the IEEE for contributions to radio-frequency and analog circuits. His involvements with IEEE are a member of Board-of-Governors of the IEEE Circuits and Systems Society from 2009 to 2011, a Senior Editor of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS from 2014 to 2015, and an Editorial Board Member of the IEEE Press from 2014 to 2016. Since 2018, he has been inducting as the Overseas Expert of the Chinese Academy of Sciences. He co-received the DAC/ISSCC Student Paper Award in 2005, the CASS Outstanding Young Author Award in 2010, the National Scientific and Technological Progress Award in 2011, the Best Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS (TCAS-II) from 2012 to 2013, the A-SSCC Distinguished Design Award in 2015, and the ISSCC Silkroad Award in 2016. In 2005, he was decorated with the Honorary Title of Value for Scientific Merits by the Macau Government. In 2016, he was the TPC Vice Co-Chair of ASP-DAC. He was the Chairman of the Distinguished Lecturer Program of the IEEE Circuits and Systems Society from 2018 to 2019. From 2010 to 2011 and from 2014 to 2015, he was an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS (TCAS-II) from 2010 to 2013. He has been an Associate Editor of IEEE JOURNAL OF SOLID-STATE CIRCUITS since 2018 and the IEEE SOLID-STATE CIRCUITS LETTERS since 2017. He is a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2014 to 2015 and the IEEE Solid-State Circuits Society from 2017 to 2018.



Rui P. Martins (Fellow, IEEE) was born in April, 1957. He received the bachelor's, master's, Ph.D., and the Habilitation (for Full-Professor) degrees in electrical engineering and computers from the Department of Electrical and Computer Engineering (DECE), Instituto Superior Técnico (IST), University of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

Since October 1980, he has been with the DECE, IST, University of Lisbon. Since October 1992, has been on leave from the University of Lisbon and with the DECE, Faculty of Science and Technology (FST), University of Macau (UM), Taipa, Macao, where he has been the Chair-Professor, since August 2013. From 1994 to 1997, he was the Dean of FST. Since September 1997, he has been the UM's Vice-Rector. From September 2008 to August 2018, he was a Vice-Rector (research). For the period September 2018–August 2023, he is a Vice-Rector (Global Affairs). Within the scope of his teaching and research activities, he has taught 21 bachelor's and master's courses. In UM, he has supervised (or co-supervised) 26 Ph.D. and 21 master's theses. He has authored or coauthored 8 books, 12 book chapters, 48 patents (38 in USA, 3 in Taiwan, and 7 in China), 628 articles, 263 articles in scientific journals, 365 papers in conference proceedings, and other 69 academic works in a total of 765 publications. He created the Analog and Mixed-Signal VLSI Research Laboratory, UM, in 2003, elevated in January 2011 to State Key Laboratory (SKLAB), China (the 1st in engineering in Macau), being its Founding Director. He was the Founding Chair of UMTEC (UM company) from January 2009 to March 2019, supporting the incubation and creation in 2018 of Digifluidic, the first UM Spin-Off, whose CEO is a SKLAB Ph.D. graduate. He was a Co-Founder of Chipidea Microelectronics, Macau [later Synopsys-Macau], from 2001 to 2002.

Dr. Rui Martins was elected, unanimously, as a Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician working and living in Asia, in July 2010. He was a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, and 2018, the Chair in 2019, and the Vice-Chair in 2021 and 2022; the IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) in 2014; and the IEEE CASS Nominations Committee (2016–2017). He was the Vice-President (2005–2014) and the President (2014–2017) of the Association of Portuguese Speaking Universities (AULP). He received two Macau Government decorations, including the Medal of Professional Merit, Portugal, in 1999, and the Honorary Title of Value, China, in 2001. He was nominated as the Best Associate Editor (2012–2013). He received the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016. He was the Founding Chair of IEEE Macau Section (2003–2005) and IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) (2005–2008) [2009 World Chapter of the Year of IEEE CAS Society (CASS)], the General Chair of IEEE Asia-Pacific Conference on CAS–APCCAS'2008, the Vice-President (VP) Region 10 (Asia, Australia, and Pacific) (2009–2011), and VP-World Regional Activities and Membership of IEEE CASS (2012–2013). He was the General Chair of ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC) in 2016 and the IEEE Asian Solid-State Circuits Conference (A-SSCC) in 2019. He was an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS (2010–2013).

Robert Bogdan Staszewski (Fellow, IEEE) was born in Bialystok, Poland. He received the B.Sc. *(summa cum laude)*, M.Sc., and Ph.D. degrees in electrical engineering from The University of Texas at Dallas, Richardson, TX, USA, in 1991, 1992, and 2002, respectively.

From 1991 to 1995, he was with Alcatel Network Systems, Richardson, involved in SONET cross-connect systems for fiber optics communications. He joined Texas Instruments Incorporated, Dallas, TX, USA, in 1995, where he was elected as a Distinguished Member of Technical Staff (limited to 2% of technical staff). From 1995 to 1999, he was engaged in advanced CMOS read channel development for hard disk drives. In 1999, he co-started the Digital RF Processor (DRP) Group within Texas Instruments with a mission to invent new digitally intensive approaches to traditional RF functions for integrated radios in deeply scaled CMOS technology. He was appointed as a CTO of the DRP Group from 2007 to 2009. In 2009, he joined the Delft University of Technology, Delft, The Netherlands, where he currently holds a guest appointment of a Full Professor (*Antoni van Leeuwenhoek Hoogleraar*). Since 2014, he has been a Full Professor with University College Dublin (UCD), Dublin, Ireland. He is also a Co-Founder of a startup company, Equal1 Labs, with design centers located in Silicon Valley and Dublin, Ireland, aiming to produce single-chip CMOS quantum computers. He has authored or coauthored 5 books, 7 book chapters, 140 journal and 210 conference publications, and holds 200 issued U.S. patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters and receivers, and quantum computers.

Dr. Staszewski was a recipient of the 2012 *IEEE Circuits and Systems* Industrial Pioneer Award. In May 2019, he received the title of a Professor from the President of the Republic of Poland. He was also the TPC Chair of the 2019 European Solid-State Circuits Conference (ESSCIRC), Krakow, Poland.