Generalized Relationship Between Frequency Response and Settling Time of CMOS OTAs: Toward Many-Stage Design

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***Abstract*— The presence of Pole-Zero (*P-Z*) pairs in the open-loop frequency response of CMOS OTAs has always been considered detrimental to the closed-loop operation of OTAs. In this work, a new proposed theory is presented showing how to reduce the impact of such *P-Z* pairs on the settling time of CMOS OTAs - using low-frequency zeros and cascaded-gain stages - consequently revealing un-tapped opportunities for many-stage CMOS OTA design. The proposed theory will be validated and verified through a design example that also demonstrates how the generalized theory unveils opportunities for many-stage OTA design. The presented example is a 2- to 8-stage CMOS OTA based on the TSMC 65 nm CMOS process, verified through simulations (schematic and post-layout) as well as some measurement results.**

***Index Terms*— OTA, cascading, multi-stage, closed-loop, DC gain, frequency compensation, low-frequency zero, pole-zero doublet, pole-zero pair, settling time, unity-gain frequency.**

I. Introduction

OPERATIONAL Transconductance Amplifiers (OTAs) are at the core of analog and mixed-signal circuits. Since the 1960's, enormous works in literature have been devoted to discussing their applications, requirements, limitations and design techniques. However, despite all these efforts, OTAs are still facing challenges when it comes to meeting the design requirements of modern analog applications, such as achieving high DC gain. These challenges are directly related to the reduction in supply voltages (V_{DD}) and transistor dimensions in advanced nano-meter scale CMOS technology nodes.

Accordingly, recent design efforts have been focused on proposing different techniques and topologies to overcome the limitations of scaled-down CMOS technologies on OTA design. These proposed designs in literature can be categorized as belonging to one of the two deep-rooted fundamental approaches [1]: (1) cascoding or stacking of transistors on the top of each other [2]–[4], and (2) cascading multiple stages of OTAs in series [5]–[10]. The cascoding approach is limited by headroom issues related to the maximum allowable supply voltage in the modern scaled-down technologies, while the cascading approach has greatly been limited by stability issues that arise when implementing multi-stage OTAs in closed-loop feedback configurations. Therefore, apart from a single exception of a 5-stage OTA in [5], the maximum number of cascaded OTA stages found in the literature has been limited to 4-stages, as in [6]–[10]. Nonetheless, the design in [5] consumes high power (∼10 mW) and introduces unusual levels of overshoot in the transient response of the system, while the designs in [6]–[10] are only customized for large capacitive loads (i.e., nF-range), making their Frequency Compensation Techniques (FCTs) unsuitable to be systematically expanded to higher stages or for driving small loads. All other conventional FCTs in the literature are only suitable for 2- and 3-stage OTAs as in [11]–[13] and are all based on limiting the frequency range of operation to ensure stability when configurated in closed loop.

More recently however, a scalable design technique was proposed for cascading 2-, 3-, 4-, 5-, and 6-stage CMOS OTAs [14], in which the stability was ensured by positioning all open-loop Pole-Zero (*P-Z*) pairs for the whole system below the unity-gain frequency (ω_t) and above the 3-dB frequency (ω_{3-dB}), without the need for full *P-Z* cancellation.

Interestingly, having open-loop *P-Z* pairs below ω_t creates *P-Z* doublets in closed-loop, as first observed in 1963 [15]. A detailed analysis then followed in [16] investigating the effects of having a *P-Z* doublet on the settling time of a closed-loop amplifier. It was shown that the closed-loop *P-Z* doublet deteriorates the OTA's settling time. The same conclusion was also stated in [17]–[19]. Surprisingly, this impact of *P-Z* doublets was not apparent in [14] and the settling time degradation was barely noticeable. Also, the same can be observed in [20], where the existence of *P-Z* doublets had a minor impact on closed-loop operation.

A closer look at [16]–[19] reveals the following: (1) the analyses of the relationship between frequency response and settling time were restricted to the case of having a single open-loop *P-Z* pair only, making them most relevant for 2-stage OTAs, (2) the analyses were based on CMOS technologies that range from line widths greater than 1 micron [16] down to only 0.35 μm [19], without considering more advanced nano-meter scale technology nodes, (3) cascading gain-stages was not a design goal in these works, especially that such older technology nodes allowed supply voltages greater than 3 V, relaxing the need for a multi-stage design.

Based on the above, this work is proposing a new generalized relationship between frequency response and settling

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time to extend the discussion while having many *P-Z* pairs (or doublets), hence establishing relevance to many-stage design. This will be done by revisiting and building upon earlier efforts. Also, the proposed work is extending the analysis – and its implementation - to more advanced nano-meter scale technology nodes. In order to achieve this, the analysis will begin by identifying the independent parameters that control the relationship, eventually leading up to its generalization based on these parameters. Such a generalization will reveal how to reduce the impact of *P-Z* doublets on settling time - through positioning the OTA zeros at Low Frequencies (*LF*) and increasing their gain - consequently revealing untapped opportunities for many-stage CMOS OTA design.

To verify and validate the proposed theory a design example with 2 to 8 cascaded-gain stages will be presented throughout this work. The presented design example, which is an expansion of the work in [14], is based on a standard TSMC 65 nm CMOS process and is validated through schematic and post-layout simulations as well as some measurement results.

For clarity purposes, from this point and onwards, we shall distinguish between two terms: '*P-Z* pair' and '*P-Z* doublet', where 'pair' will be used for open-loop configurations and 'doublet' will be used for closed-loop configurations.

This paper starts by revisiting the previously reported analysis on the relationship between frequency response and settling time having one *P-Z* pair in Section II. Then this relationship, having one *P-Z* pair, will be studied to overcome the limitations of the previously reported works in Section III, paving the way towards Section IV, in which the relationship will be generalized for *N*-stage OTAs, having (*N*-1) *P-Z* pairs. In Section V, the design example of the 2- to 8-stage CMOS OTA will be introduced. Implementation and validation of the proposed relationships while having one *P-Z* pair and (*N*-1) *P-Z* pairs are presented in Sections VI and VII, respectively. Finally, Section VIII concludes the paper.

II. Revisiting the Previously Reported Analysis on the Relationship Between Frequency Response and Settling Time Having Pole-Zero Pairs

Analyzing the relationship between OTA's frequency response and settling time depends on the relationship between open-loop and closed-loop configurations. Therefore, having an open-loop Transfer Function (*TF*), which can represent the use of a cascading scheme to build multi-stage OTAs is the starting point.

A. Cascading Multi-Stage CMOS OTAs

Figure 1 shows the block diagram and a circuit level realization of an *N*-stage CMOS OTA, which will be used as the analysis and design vehicle throughout this work. As seen in the block diagram of Fig. 1(a), building multi-stage CMOS OTAs requires cascaded-gain stages (to achieve the required gain) and a compensator (to ensure stability and achieve frequency requirements). The cascaded-gain stages can achieve a DC gain ($A_{DC,N}$) of

$$A_{DC,N} = \prod_{i=1}^{N} (A_i), \tag{1}$$

where A_i is the gain provided by the i^{th} gain stage and N is the number of stages. On the other hand, and since this is a CMOS-based OTA, poles and zeros will be part of the OTA's realization. To appropriately control these poles and zeros, a compensator, similar to the one seen in Fig. 1(a), will be used. Usually, in such OTAs, in addition to the 3-dB frequency, each gain stage will produce a *P-Z* Pair. Therefore, the open-loop *TF* takes a bilinear-cascade form; and it can be written as

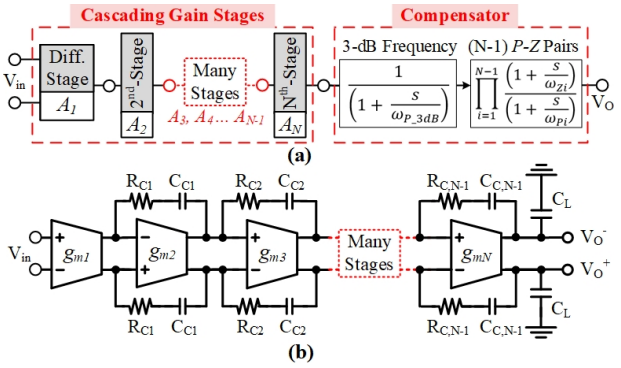

Fig. 1. Cascading *N*-stage CMOS OTA: (a) block diagram having cascaded gain stages and compensator, and (b) circuit level realization of a differential-ended *N*-stage CMOS OTA.

$$A(s) = \frac{A_{DC,N}}{\left(1 + \frac{s}{\omega_{P\_3dB}}\right)} \times \prod_{i=1}^{N-1} \frac{\left(1 + \frac{s}{\omega_{Zi}}\right)}{\left(1 + \frac{s}{\omega_{Pi}}\right)}, \tag{2}$$

where ω_{P_3dB} is the 3-dB frequency, ω_{Pi} and ω_{Zi} are the *P-Z* pairs which are produced by the compensation circuit of each stage. In conventional FCTs, these *P-Z* pairs are either pushed to frequencies much higher than ω_t or positioned at the exact same frequency (below ω_t) to get full *P-Z* cancellation [21]. thus, ω_{P_3dB} will be the only pole below ω_t, and the relationship between frequency response and settling time will follow a single-time constant behavior. However, in this work, a generalized discussion will be introduced, therefore, these *P-Z* pairs will be part of the analysis without being excluded or cancelled.

Before proceeding to the analysis, the block diagram of Fig. 1(a) and its bilinear-cascade *TF* of Eqn. (2) can be realized by using the differential-ended circuit level implementation of Fig. 1(b). The *gm*-blocks will be responsible for achieving the required DC gain, while the R-C compensation networks (which are connected across each stage) will properly place the *P-Z* pairs at the required frequencies.

B. Previously Reported Analysis on the P-Z Pair Impact on Settling Time

The presence of an open-loop *P-Z* pair below ω_t creates a *P-Z* doublet in closed-loop, and such a phenomenon is well-known in the literature and was first discussed in 1963 [15]. However, the presence of closed-loop *P-Z* doublets at that time was discussed as an effect that arises due to an inevitable mismatch between the pole and the zero when trying to achieve *P-Z* cancellation. The leading and the detailed analysis on the effects of having a *P-Z* pair on the settling time of a closed-loop amplifier was first discussed in [16] and [17]. Then, the same discussion and conclusion was also stated in [18], [19]. All these previously reported analyses have discussed this issue while having one *P-Z* pair only.

To realize an open-loop *TF* with a one P-Z pair (i.e., ω_{P1} and ω_{Z1}) and a finite pole (i.e., ω_{P_3dB}), a two-stage OTA

can be used (i.e., $N = 2$). Thus, the *TF* of Eqn. (2) can be written as

$$A(s) = \frac{A_{DC,2}}{\left(1 + \frac{s}{\omega_{P\_3dB}}\right)} \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)}. \quad (3)$$

The analyses in [16]–[19] depend mainly on the open-loop *P-Z* pair separation distance (δ_{OL}), which can be expressed as

$$\delta_{OL} = \omega_{P1} - \omega_{Z1} \quad (4)$$

or as a ratio given by

$$\delta_R = \frac{\omega_{P1}}{\omega_{Z1}}. \quad (5)$$

Based on Eqn. (3) one can show that the *TF* for the unity-gain closed-loop configuration has the following general form

$$G(s) = \frac{A(s)}{1 + A(s)} = \frac{A_{DC,2}}{\left(1 + \frac{s}{\omega_{CL,a}}\right)} \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{CL,b}}\right)} \quad (6)$$

where $\omega_{CL,a}$ is the frequency of the first pole and $\omega_{CL,b}$ is the frequency of the second pole in the closed-loop response.

The closed-loop poles of Eqn. (6) have been shown [16] to be expressible in terms of the open-loop OTA parameters as:

$$\omega_{CL,a} \approx \omega_{t,REF} \quad (7)$$

and

$$\omega_{CL,b} = \omega_{Z1}\left[1 - \frac{\left(1 - \frac{\omega_{P1}}{\omega_{Z1}}\right)}{\left(\frac{\omega_{t,REF}}{\omega_{Z1}} - 1\right)}\right] \approx \omega_{Z1} \quad (8)$$

where they have assumed that the unity-gain frequency is equal to Gain-Bandwidth Product (i.e., $\omega_{t,REF} = A_{DC,2}$ x ω_{P_3dB}).

Correspondingly, the closed-loop step response to an input step of magnitude V_{in} can be written as follows [16]

$$V_{OUT}(t) = V_{in}\left[1 - k_1 e^{-t\omega_{t,REF}} + k_2 e^{-t\omega_{Z1}}\right] \quad (9)$$

where

$$k_1 = 1 + \frac{\delta_{OL}}{\omega_{t,REF}}, \quad (10)$$

and

$$k_2 = 1 - k_1 = -\frac{\delta_{OL}}{\omega_{t,REF}}. \quad (11)$$

From Eqn. (9) we see that the step response consists of two time-dependent parts: one involving $\omega_{t,REF}$ and the other ω_{Z1}. Each term is weighted by separate coefficients k_1 and k_2 that are also dependent on δ_{OL}.

Although the *TF* of Eqn. (3) has two finite poles, the settling time will be affected by the distance between ω_{P1} and ω_{Z1} only, while the distance between ω_{P_3dB} and ω_{Z1} has no impact. The reason is that once the OTA is constructed in unity-gain closed-loop configuration, ω_{P1} will move towards ω_{Z1}, and ω_{P_3dB} will move towards ω_t. Consequently, the OTA step response will not be affected by the ratio $\omega_{Z1}/\omega_{P\_3dB}$.

As seen in Eqn. (9) and (11), the slow settling component residual (i.e., $V_{in}k_2$) depends on the critical ratio [($V_{in}\delta_{OL}$) /$\omega_{t,REF}$]. This ratio can be made small if the numerator is small or the denominator is large, or both simultaneously. Under such conditions, k_1 is very close to unity and k_2 is very close to zero. In the past, [16] suggested that a small frequency difference between the *P-Z* pair is necessary to achieve a small value for k_2 as it relates to the slow settling component. As this requires tight control over the *P-Z* pair position, it is generally considered impractical. Also, it was concluded that positioning the *P-Z* pair at low frequencies will produce a slower time response with smaller amplitude compared to positioning the *P-Z* pair at high frequencies. Thus, the closed-loop *P-Z* doublet deteriorates the OTA's settling time [16]–[19].

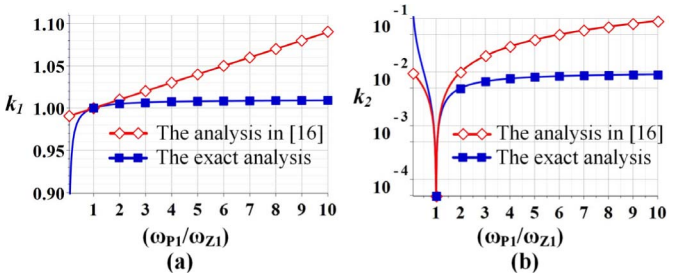

Fig. 2. The difference between the previously reported analysis and the proposed exact analysis for step response coefficients:(a) k_1, and (b) k_2.

However, the previous open-loop *P-Z* pair-based analysis is associated with some limitations. First, while deriving the closed-loop poles (i.e., $\omega_{CL,a}$ and $\omega_{CL,b}$), it has been assumed that $\omega_{t,REF} = (A_{DC,2}$ x $\omega_{P\_3dB})$. This is not accurate, where the open-loop *P-Z* pair is below the unity-gain frequency, thus, the exact unity-gain frequency ($\Omega_{t,REF}$) should be expressed as

$$\Omega_{t,REF} = A_{DC,2} \times \omega_{P\_3dB} \times \frac{\omega_{P1}}{\omega_{Z1}} = \omega_{t,REF} \times \delta_R \quad (12)$$

Considering the unity-gain frequency to be $\omega_{t,REF}$ in [16] has hidden the fact that increasing δ_R, by increasing δ_{OL}, will increase the unity-gain frequency, which in turn will reduce the slow settling component residual of Eqn. (11). This can be clearly seen if k_2 in Eqn. (11) is re-written with its exact form (after replacing $\omega_{t,REF}$ by $\Omega_{t,REF}$) as

$$k_2 = -\frac{\delta_{OL}}{\Omega_{t,REF}} = -\frac{\delta_{OL}}{\omega_{t,REF} \times \delta_R} \quad (13)$$

While the exact k_1 of Eqn. (10) can be rewritten as

$$k_1 = 1 + \frac{\delta_{OL}}{\Omega_{t,REF}} = 1 + \frac{\delta_{OL}}{\omega_{t,REF} \times \delta_R}. \quad (14)$$

By simulating Eqs. (10), (11), (13) and (14), Fig. 2(a) and (b) show the hidden behavior of k_2 and k_1, respectively. As depicted form Fig. 2(a) and (b), the results of k_1 and k_2, which have been reported in [16], are accurate only around $\omega_{P1}/\omega_{Z1} = 1$ (i.e., $\delta_R = 1$). Once δ_R goes beyond 2, the slow settling component residuals saturates, as seen in the exact analysis of Fig. 2(b), and no more degradation can be introduced even if δ_{OL} is increased.

In addition to the above-mentioned issue of conducting the analysis while having the open-loop dependent parameter $\omega_{t,REF}$, the analysis in [16] has only considered the case where $\omega_{Z1} \geq \omega_{P1}$, while the case of having ω_{Z1} at low frequencies (below ω_{P1}) has not been investigated.

In the light of these issues, there remains to be a timely need for a generalized analysis using all open-loop independent

parameters to examine the actual impact of having a *P-Z* pair below the unity-gain frequency.

III. Demystifying the Relationship Between Frequency Response and Settling Time Having One Pole-Zero Pair

The proposed analysis in this section will include all open-loop independent parameters of Eqn. (3). However, OTAs are usually required to operate over a large range of frequency conditions. Rather than design a new *TF* for each case, a better approach is to normalize the *TF* to reduce the degree of complexity as discussed in Appendix A.

Based on the results found in Appendix A, the open loop *TF* of Eqn. (3) can be written using the normalized approach (where the "*s*" Laplace variable will be replaced with the normalized "*p*" Laplace variable) as

$$A\,(p) = \frac{A_Z}{p} * \frac{(1+p)}{\left(1+\frac{p}{\omega_P}\right)} \tag{15}$$

where A_Z is the gain at the new position of ω_{Z1} after normalization (i.e., after setting the compensation zero ω_{Z1} at 1 rad/s), and ω_P is the new position of the compensation pole ω_{P1} after this normalization, and it is unitless. Also, the frequency-normalized unity-gain frequency (Ω_t) can be written in terms of the open-loop parameters for all values of ω_P as

$$\Omega_t = A_Z.\omega_P \tag{16}$$

Ultimately, the OTA will be used in a closed-loop configuration where the impact of the open-loop frequency-response parameters will be revealed. Once applying an input step while having the OTA in closed-loop unity configuration, the OTA's settling time can be examined. Therefore, in the next subsections, the close-loop response will be discussed to precisely identify how to control the closed-loop parameters based on the open-loop response. Then, the generalized relationship between frequency response and settling time will be derived after investigating the 2-stage OTA's unity step response having the *P-Z* pair below Ω_t.

A. Analyzing the Closed-Loop Frequency-Response in the Presence of P-Z Doublets

If the open-loop *TF* includes a *P-Z* pair as described by Eqn. (15), then the unity-gain closed-loop *TF*, $T(p)$, (i.e., having unity-feedback factor) would appear as

$$T\,(p) = \frac{(1+p)}{\left(1+\frac{p}{\omega_{CL,1}}\right)\left(1+\frac{p}{\omega_{CL,2}}\right)} \tag{17}$$

where $\omega_{CL,1}$ and $\omega_{CL,2}$ are the poles of the closed-loop configuration after normalization. As $A_Z \gg \omega_P$, $\omega_{CL,1}$ and $\omega_{CL,2}$ will be widely spaced apart. Further, using the quadratic formula for a 2nd-order polynomial, one can find that:

$$\omega_{CL,1} = A_Z\omega_P \approx \Omega_t \tag{18}$$

and

$$\omega_{CL,2} \approx \frac{A_Z}{1+A_Z} + \frac{1}{A_Z\omega_P}. \tag{19}$$

Here one of the poles of the closed-loop system will be located at $A_Z\omega_P$ (i.e., Ω_t) and the other one is located very close to 1 rad/s (i.e., the normalized frequency location of ω_{Z1}). The residual *LF* closed-loop pole ($\omega_{CL,2}$) depends on A_Z, when A_Z is large, and on $1/(A_Z\omega_P)$, when ω_P is very small (i.e., $\omega_P < 1$).

Going forward, the frequency difference between the *P-Z* doublet (i.e., the *LF* closed-loop pole ($\omega_{CL,2}$) and the zero at 1 rad/s) will be denoted with the term δ_{CL}. Assuming the compensation pole can take on values either larger than unity or less than unity, the *closed-loop pole-zero doublet separation distance* (δ_{CL}) can be written as

$$\delta_{CL} = \omega_{CL,2} - 1. \tag{20}$$

By substituting the expression of $\omega_{CL,2}$, seen in Eqn. (19), into Eqn. (20), δ_{CL} can be re-written as

$$\delta_{CL} \approx \frac{1}{A_Z\omega_P} - \frac{1}{A_Z} = \frac{1-\omega_P}{A_Z\omega_P}. \tag{21}$$

For many situations, the compensation pole ω_P is either much greater than unity or much less than unity. As such, the closed loop *P-Z* doublet separation distance can be approximated as

$$\delta_{CL} = \begin{cases} \dfrac{1}{A_Z\omega_P}, & \omega_P \ll 1 \\ -\dfrac{1}{A_Z}, & \omega_P \gg 1. \end{cases} \tag{22}$$

Fig. 3(a) plots the behavior of δ_{CL} (according to Eqn. (21) and (22)) for a sweep of ω_P between 0.01 and 100 rad/s, for different values of A_Z. As depicted form Fig. 3(a), controlling δ_{CL} can be done through two independent parameters: A_Z and ω_P. To reduce δ_{CL} one can target higher A_Z regardless of the value of ω_P. However, the minimum possible value of δ_{CL}, when controlling its value through ω_P, can be achieved when $\omega_P = 1$ rad/s, which is the position of ω_{Z1} after normalization. Nevertheless, the optimum value of δ_{CL} will be determined by the design requirements as will be discussed in Section V. This shows that the open-loop *P-Z* pair separation ratio (i.e., ω_{P1}/ω_{Z1} before normalization and $\omega_P/1$ after normalization) is a parameter that affects δ_{CL} as previously reported in other works [16]–[19]. But what has not been reported previously (due to technology limitations) is that increasing ω_P (i.e., ω_{P1}/ω_{Z1}) beyond certain values (i.e., $\omega_P \geq 10$), will have no effect on δ_{CL}, as seen in Fig. 3(a). Also, the zero gain (A_Z) plays a critical role in controlling the value of δ_{CL}. In the next subsection, these relationships will show how to reduce the effects of having the *P-Z* doublets on the settling time of two-stage OTAs (i.e., when having one *P-Z* pair).

B. The Relationship Between Settling Time and Open-Loop Frequency-Response Parameters

Based on the results found in Eqn. (18), (19) and (22), and as derived in Appendix B, the unit step response can be simplified as

$$y\,(t) = 1 - \left(1+\frac{1-\omega_P}{A_Z\omega_P}\right)e^{-A_Z\omega_P t} + \left(\frac{1-\omega_P}{A_Z\omega_P}\right)e^{-\left(1+\frac{1-\omega_P}{A_Z\omega_P}\right)t} \tag{23}$$

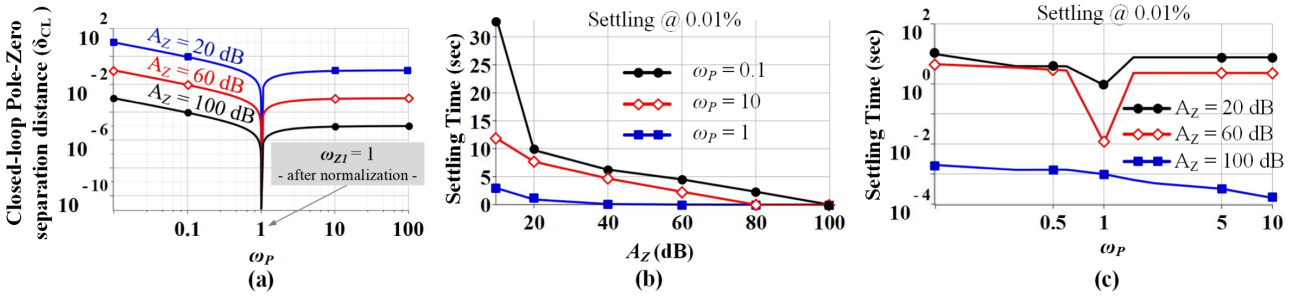

Fig. 3. The proposed theory results having one *P-Z* pair: (a) the closed-loop P-Z separation distance (δ_{CL}) as a function of ω_P for different values of A_Z., (b) settling time as a function of A_Z for different ω_P when the steps settles @ 0.01% of the final value, based on the step-response result of Eqn. (24), and (c) settling time as a function of ω_P for different A_Z when the steps settles @ 0.01% of the final value, based on the step-response result of Eqn. (23).

This expression will hold over a wide range of ω_P and A_Z, regardless of their values. However, Eqn. (23) can be written for different cases of ω_P as follows:

$$y(t) = \begin{cases} 1 - \left(1 - \dfrac{1}{A_Z}\right) e^{-A_Z \omega_P t} \\ \quad - \left(\dfrac{1}{A_Z}\right) e^{-\left(1 - \frac{1}{A_Z}\right)t}, & \omega_P \gg 1 \\ 1 - e^{-A_Z t}, & \omega_P = 1 \\ 1 - \left(1 + \dfrac{1}{A_Z \omega_P}\right) e^{-A_Z \omega_P t} \\ \quad + \left(\dfrac{1}{A_Z \omega_P}\right) e^{-\left(1 + \frac{1}{A_Z \omega_P}\right)t}, & \omega_P \ll 1 \end{cases} \tag{24}$$

Showing such wide range impact of ω_P and A_Z has not been discussed in the previously reported analyses, hence, Eqn. (24) represents the generalized relationship between frequency response and time response having one *P-Z* doublet. It also shows all independent parameters through which one can reduce the impact of the *P-Z* doublet on the step response.

Based on Eqn. (24), Fig. 3(b) shows the settling time as a function of A_Z for different values of ω_P. This figure reports the settling time at 0.01% of the final value, as it is usually the minimum required settling time different applications [16]. As seen in Fig. 3(b), the settling time, when $\omega_P \gg 1$ (i.e., red line), is lower than the settling time when $\omega_P \ll 1$ (i.e., black line). Also, as A_Z reaches 80 dB, the settling time, when $\omega_P \gg 1$, will have almost similar values of having ω_P at 1 (i.e., full *P-Z* cancellation). This impact of high A_Z (i.e., having a *LF* zero) on enhancing the OTA's settling time has not been reported in previous works.

Similarly, and unlike the previously reported works, Fig. 3(c) shows the settling time but this time as a function of ω_P for different values of A_Z. When $A_Z = 100$ dB, the settling time is no longer affected by the open-loop *P-Z* pair separation (i.e., $\omega_P/1$), which suggests that at high A_Z, the response settles to its final value before the impact of *P-Z* doublets starts. Interestingly, for $A_Z = 100$ dB, when increasing ω_P, the response will exhibit faster settling times.

Clearly, some values of A_Z might be hard to achieve practically when cascading 2 or 3 gain-stages. Therefore, one can position ω_P at values near 1 to reduce δ_{CL}, which in return, will reduce the impact of the closed-loop *P-Z* doublet. However, when using many gain-stages ($N \geq 4$), A_{DC} will be larger, and these values for A_Z are easy to achieve if the zero is positioned at *LF*, where A_{DC} is proportional to A_Z.

To conclude this section and clarify the new proposed observations, it is readily apparent from Eqs. (22) and (24) that a higher A_Z forces two things to occur: (1) The coefficient in front of the *LF* term of the unit-step response will reduce in magnitude, and (2) the separation distance between the closed-loop P-Z doublet will also reduce in magnitude. These two things will help reducing the delay caused by the presence of the *P-Z* doublets.

IV. Generalized Relationship Between Frequency Response and Settling Time Having N-1 Pole-Zero Pairs

For *N*-Stage CMOS OTAs the analysis's degree of complexity will increase, where each stage will add a *P-Z* pair. For example, when $N = 3$, the OTA will have two *P-Z* pairs (i.e., ω_{P1}, ω_{Z1}, ω_{P2}, and ω_{Z2}). There are 24 different cases to position and arrange the two *P-Z* pairs. Therefore, to simplify the analysis, one can start with the bilinear *TF* of the normalized N^{th}-order integrator-based OTAs with zero-only compensator. This *TF* is derived in a manner similar to that used with Eqn. (15) in Appendix A, and can be written as

$$A(p) = \frac{A_Z}{p^N} \times (1 + p)^{N-1}. \tag{25}$$

Thus, in the following subsections, the closed-loop analysis and the step response will be discussed based on Eqn. (25). Then, the results will be expanded while having pole-zeros compensator instead of having zeros-only compensator. To the best of the author's knowledge, these proposed analyses with $N > 2$ have not been discussed in literature before.

A. Closed-Loop Analysis Having a Zeros-Only Compensator

Based on Eqn. (25), the unity-gain closed-loop *TF* can be written as

$$T(p) = \frac{A_Z (1 + p)^{N-1}}{p^N + A_Z (1 + p)^{N-1}}. \tag{26}$$

Owing to the nature of the *LHP* zeros located at frequencies of 1 rad/s, all but one of the *N* closed-loop poles will move towards these zeros with individual separation distances of $\delta_{CL,i}$ for $i = 1$ to *N-1*. The N^{th} pole will be positioned essentially at Ω_t.

To illustrate this, consider the closed-loop poles distributions in Table I for the particular case of $A_Z = 80$ dB across orders ranging from 3 to 4. The pole-zero separation distance ($\delta_{CL,i}$) is computed by taking the exact differences between the zero (i.e., zeros frequencies $= -1$ rad/s) and the pole positions in the *p*-plane.

Owing to the presence of the *N-1* coincident zeros in the open-loop response, the *N-1* poles of the closed-loop system will move very close to the same frequency locations as these zeros but will not overlap. In a manner similar to the previous

TABLE I

CLOSED-LOOP POLES DISTRIBUTION AND THE POLE-ZERO SEPARATION DISTANCE ($\delta_{CL,i}$) VERSUS NUMBER OF STAGES (N) FOR ZEROS-ONLY COMPENSATOR WITH $A_Z = 80$ dB (I.E., $\Omega_t = 10^4$ rad/s)

N	closed-loop poles' frequencies (rad/s)				Pole-Zero separation distance ($\delta_{CL,i}$)		
	$\omega_{CL,1}$	$\omega_{CL,2}$	$\omega_{CL,3}$	$\omega_{CL,4}$	$\delta_{CL,1}$	$\delta_{CL,2}$	$\delta_{CL,3}$
3	- 1.0101	-0.99014	- 9997.9	-	0.0101	- 0.00986	-
4	- 1.0495	- 0.97554 + j0.03772	- 0.97554 -j0.03772	- 9996.9	0.04950	- 0.02445 + j0.03772	- 0.02445 - j0.03772

two-stage case (i.e., having one *P-Z* pair), we shall denote the small separation distance between the i^{th}-pole and the i^{th}-zero of the closed-loop system by $\delta_{CL,i}$. The remaining closed-loop pole will appear at frequency Ω_t (where $\Omega_t = A_Z$). Consequently, the closed-loop *TF* can be approximated as

$$T(p) = \frac{(1+p)^{N-1}}{\left(1+\frac{p}{A_Z}\right)\prod_{i=1}^{N-1}\left[1+\frac{p}{(1+\delta_{CL,i})}\right]}. \tag{27}$$

B. Unit Step-Response Having a Zeros-Only Compensator

With the denominator polynomial of the *TF* of Eqn. (27) described in factor form, the step-response can easily be found by converting the *TF* to partial fraction form, then taking the inverse Laplace transform, resulting in

$$y(t) \approx 1 - \prod_{i}^{N-1}\left(1+\delta_{CL,i}\right)e^{-A_Z t} + \sum_{i}^{N-1} k_i e^{-(1+\delta_{CL,i})t}, \tag{28}$$

where the k_i-coefficients are the *LF* frequency exponential term coefficients, and can be approximated as follows:

$$k_i \approx \delta_{CL,i}^{N-1} \times \frac{\prod_{m=1,m\neq i}^{N-1}\left(1+\delta_{CL,m}\right)}{\prod_{m=1,m\neq i}^{N-1}\left(\delta_{CL,i}-\delta_{CL,m}\right)}. \tag{29}$$

In all cases, the need for values for $\delta_{CL,i}$ is readily apparent. While no simple expression of the individual pole-zero separation distances $\delta_{CL,i}$ have yet been found, empirical evidence suggests the following general relationship:

$$\delta_{CL,i} \approx \frac{1}{\sqrt[N-1]{A_Z}}, \quad i = 1 \ldots N-1. \tag{30}$$

While it was shown previously that a single closed-loop *P-Z* separation distance was inversely proportional to A_Z, the above statement suggests that this gain must be spread equally across all *P-Z* combinations. To illustrate this statement, for $A_Z = 80$ dB, $\delta_{CL,1} = 0.010$ at $N = 3$, $\delta_{CL,1} = 0.0464$ at $N = 4$. Scanning the $\delta_{CL,1}$ of Table I that lists $\delta_{CL,i}$ as a function of *TF* order, one can see that the above results correlate quite well with the theory captured by Eqn. (30).

Using the above principle of $\delta_{CL,i}$ suggested by Eqn. (30), the unit-step response of the N^{th}-order closed-loop *TF* can be approximated with the following expression:

$$y(t) \approx 1 - \left(1+\frac{1}{\sqrt[N-1]{A_Z}}\right)e^{-A_Z t} + \sum_{i=1}^{N-1}\frac{1}{\sqrt[N-1]{A_Z}}e^{-\left(\frac{\sqrt[N-1]{A_Z}+1}{\sqrt[N-1]{A_Z}}\right)t}. \tag{31}$$

Fig. 4(a) provides a plot of the exponential terms in the unit step response for the case when the order $N = 5$. As is evident from this plot, all coefficients decrease in magnitude with increasing A_Z. Depending on the order of the *TF*, the contribution of each *LF* exponential term will vary. The lower the order, the smaller its overall contribution.

Fig. 4(b) and (c) shows the impact of increasing A_Z on settling time for different number of *P-Z* pairs (i.e., $N = 2$ to 8) based on Eqn. (31). As seen in Fig. 4(b) and (c), settling time is decreasing as A_Z increases for different percentages of settling time. Again, this implies that the impact of closed-loop *P-Z* separation distances can be highly reduced with higher gain, regardless of how many *P-Z* pairs the OTA might have or what is the exact separation distance between them.

Also, the improvement can be seen by comparing the settling time at 0.01% to the settling time at 1%. This will be fully discussed while comparing the results of Fig. 4(b) and (c) to the circuit realization results in Section VII.

In conclusion, through the appropriate selection of the A_Z parameter in the OTA open-loop response as described by Eqn. (25), *the zeros of the compensator can be placed at low frequency to enhance the performance attributes of the closed-loop system provided that the open-loop gain at a normalized frequency of 1 rad/s is high enough for the given application.*

C. Analysis Having Pole-Zeros' Compensator

The analysis steps of the previous subsections will be followed here again, but with the assumption that an OTA's N-stage open-loop *TF* is described as follows:

$$A(p) = \frac{A_Z}{p^{N-1}} \times \frac{(1+p)^{N-1}}{\left(1+\frac{p}{\omega_P}\right)}, \tag{32}$$

where there are *N-1* poles at DC and one at a frequency of ω_P.

By following the exact steps to derive Eqn. (31), the unit step response takes on the exact same form as the N^{th}-order integrator with zeros-only compensator of Eqn. (31), except that the high-frequency time constant is a product of A_Z and ω_P instead of A_Z. Thus, the unit-step response of the N^{th}-order closed-loop *TF* (Pole-Zeros' compensation) can be approximated with the following expression:

$$y(t) = \begin{cases} 1 - \left(1-\frac{1}{\sqrt[N-1]{A_Z}}\right)e^{-A_Z\omega_P t} \\ \quad - \sum_{i=1}^{N-1}\frac{1}{\sqrt[N-1]{A_Z}}e^{-\left(\frac{\sqrt[N-1]{A_Z}+1}{\sqrt[N-1]{A_Z}}\right)t}, & \omega_P \gg 1 \\ 1 - \left(1+\frac{1}{\sqrt[N-1]{A_Z}}\right)e^{-A_Z\omega_P t} \\ \quad + \sum_{i=1}^{N-1}\frac{1}{\sqrt[N-1]{A_Z}}e^{-\left(\frac{\sqrt[N-1]{A_Z}+1}{\sqrt[N-1]{A_Z}}\right)t}, & \omega_P \ll 1 \end{cases} \tag{33}$$

The same conclusion can be stated here; even if the poles are not at DC, once the zeros are positioned at *LF*s with higher DC gains, the impact of $\delta_{CL,i}$ will become insignificant and the step response will follow the same behavior of Eqn. (33).

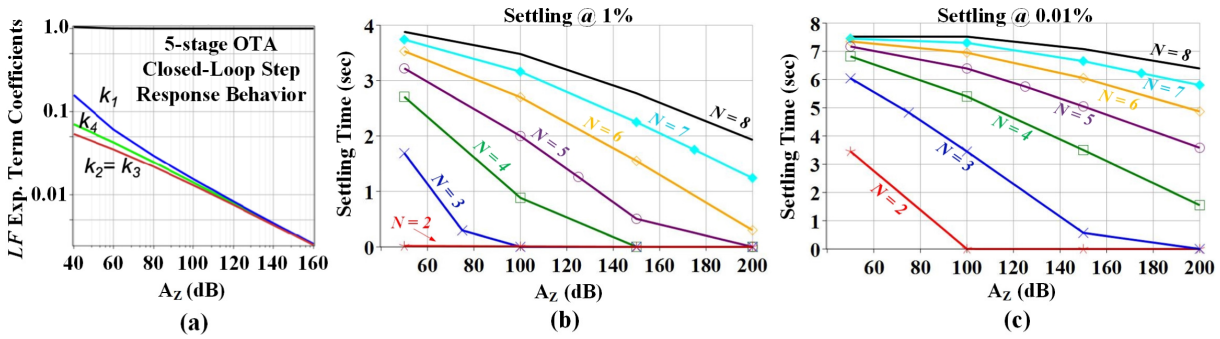

Fig. 4. The proposed theory results having (N-1) P-Z pair: (a) coefficient weights (ki) of LF exponential terms of unit-step response of closed-loop system involving an OTA with Zeros-Only Compensator for 5-stage, (b) the relationship between settling time and A_Z for different numbers of P-Z pairs when settling at 1% of final value, and (c) the relationship between settling time and A_Z for different numbers of P-Z pairs when settling at 0.01% of final value.

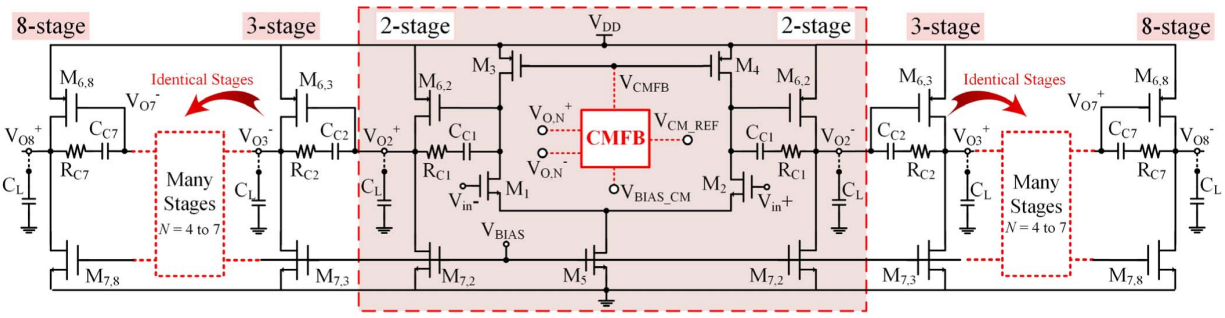

Fig. 5. Transistor level implementation of the 2-stage, 3-stage, 4-stage, 5-stage, 6-stage, 7-stage, and 8-stage CMOS OTAs. All gain stages are identical in transistor aspect ratios. The circuit uses a differential-ended configuration, the stages from 4-to-7 have been omitted for simplicity.

V. The Design Example: A Scalable 2- to 8-Stage CMOS OTAs

The proposed theory suggests that once increasing A_Z (by increasing A_{DC} and/or positioning the zeros at low frequencies) the open-loop P-Z pairs' impact on settling time will be reduced, regardless of open-loop P-Z pairs' numbers or their separation distances (i.e., ω_{P1}/ω_{Z1}). Thus, to verify the proposed theory, one should design an OTA which can provide a wide range of DC gains. At the same time, this OTA should have the capability to create a specific number of P-Z pairs and offers the capability to control their positions.

Figure 5 shows the transistor-level implementation of a differential-ended N-stage CMOS OTA, shown earlier in Fig.1, but here $N = 2$ to 8. This circuit will be used to verify the proposed theory, where it can provide a scalable and a wide range of DC gains (i.e., 50 dB to 200 dB). Also, it can create a P-Z pair whenever a gain stage and its R-C compensation circuit are added. Consequently, this will demonstrate how the generalized theory unveils opportunities for many-stage OTA design. Therefore, before verifying the proposed theory having (N-1) P-Z pairs, the 2- to 8-stage CMOS OTAs design principle will be first introduced, showing how to obtain a scalable A_{DC} and create (N-1) P-Z pairs while maintaining the OTA's stability.

A. Design of the Scalable 2- to 8-Stage CMOS OTAs

The proposed design of the scalable 2- to 8-stage OTA, shown in Fig. 5, consists of a differential stage (i.e. M_1 – M_5), which serves as the 1st stage, followed by seven identical Common Source (CS) gain-stages (the second stage consists of M_6 and M_7 while subsequent stages consist of transistors identical to them). Therefore, the overall $A_{DC,N}$ is the gain of the differential stage multiplied by the gain of each CS stage as expressed earlier in Eqn. (1).

TABLE II
Devices' Sizes of 2- to 8-Stage CMOS OTA of Fig. 5 and Fig. 6(a)

Device	Aspect Ratio	Device	Aspect Ratio
M_1= M_2	2 µm / 1 µm	$M_{6,N}$*	4.8 µm / 455 nm
M_3= M_4	0.6 µm / 130 nm	$M_{7,N}$*	5 µm / 130 nm
M_5	2 µm / 620 nm	M_{C1}	1 µm / 1 µm

* $N = 2$ to 8

The purpose of the proposed architecture is to provide a scalable DC gain in the range of 50 dB to 200 dB to obtain the same range that has been used in the theory as seen in the X-axis of Fig. 4(b) and (c). Therefore, each stage has been designed to achieve an A_{DC} of 25 dB (including the differential input-stage). This pins-down the required sizes of all transistors to meet power consumption and overdrive voltage requirements. Also, this defines the values of the small-signal parameters (i.e., g_m and r_O) of all transistors. The transistor sizes used in this design can be seen in Table II.

Consequently, to obtain an A_{DC} of 50 dB, a designer would select $N = 2$, or in other words, use the 2-stage OTA topology. Likewise, the 3-, 4-, 5-, 6-, 7-, and 8-stage OTA configurations would achieve gains of 75 dB, 100 dB, 125 dB, 150 dB, 175 dB, and 200 dB, respectively. Such high A_{DC}s have many applications; like the high resolution 32-bit Analog-to-Digital Converters [22].

To ensure robustness of biasing voltages, the Common Mode Feedback Circuit of Fig. 6(a), which is based on standard techniques as in [23], has been used.

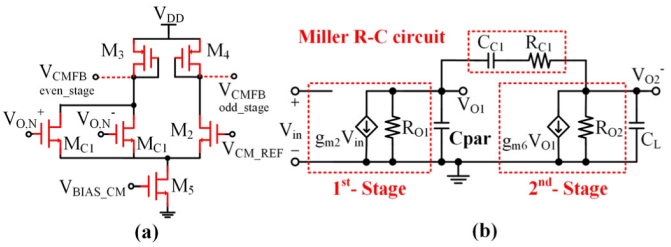

Fig. 6. (a) The Common Mode Feedback circuit of Fig. 5 and (b) single-ended two-stage CMOS OTA's small signal model.

B. Stability and the Open-Loop P-Z Pair Positioning

To ensure the stability of such high gain OTAs, an R-C compensation circuit is connected across each gain stage as shown in Fig. 5. Each R-C compensation circuit will create a *P-Z* pair whenever a new gain stage is added. Thus, the open-loop input-output *TF* takes a bilinear form; and can be written as the *TF* of Eqn. (2). This bilinear *TF* is also similar to the one seen in Eqn. (32), except that Eqn. (32) is a normalized form with *N-1* poles at DC, one pole at a finite frequency and all zeros at 1 rad/s.

Therefore, these compensated poles and zeros will be positioned below ω_t in a certain pattern that ensures the OTAs' stability; by keeping ω_t below the parasitic poles while obtaining a sufficient Phase Margin (PM), which is given by:

$$PM = 180 - \sum_{i=1}^{N-1} \theta_{P,i} + \sum_{i=1}^{N-1} \theta_{Z,i} \tag{34}$$

where $\theta_{P,i}$ is the phase of the i^{th}-pole and $\theta_{Z,i}$ is the phase of the i^{th}-zero. By doing so, the unity-gain frequency is no longer equal to the GBP, but it is now given by

$$\omega_t = A_{DC,N} \times \omega_{P_{3dB}} \times \prod_{i=1}^{N-1} \left(\frac{\omega_{Pi}}{\omega_{Zi}} \right). \tag{35}$$

The ideal positioning of these *P-Z* pairs should follow the *TF* of Eqn. (32). However, apart from the 2-stage OTA, controlling the exact positions of poles and zeros (using the R-C compensation circuit of Fig. 5) is limited due to the coupling between stages and the correlation between the poles and zeros' positions. Therefore, the exact positioning of the *P-Z* pairs cannot be achieved according to Eqn. (32).

Fortunately, the proposed theory suggests that increasing A_Z will reduce the impact of the *P-Z* pairs regardless of their exact numbers or the positions/distances between them. Thus, if one can position the poles and zeros below ω_t, with no specific order, the improvement of having higher gain (i.e., higher number of stages) on settling time can still be seen. This makes the circuit of Fig. 5 suitable to examine this improvement in settling time as will be seen in Section VII.

Consequently, a scalable FCT is proposed here to avoid the complexity of using the exact poles and zeros' equations of 3-, 4-, 5-, 6-, 7-, and 8-stage OTAs. This scalable FCT positions the *P-Z* pairs at frequencies below ω_t, without *P-Z* cancellation, such that

$$\omega_{P\_3dB} < \omega_{z1} < \omega_{\text{P1}} < \ldots < \omega_{zi} < \omega_{Pi} < \omega_t, \tag{36}$$

where this arrangement reduces the coupling between stages and allows positioning the *P-Z* pairs apart from each other.

Accordingly, the proposed FCT avoids such levels of complexity by designing the compensation circuit of the 2-stage OTA first (i.e., $R_{C1,(2-\text{stage.})}$ and $C_{C1,(2-\text{stage.})}$) and then scaling these values for higher stages. These steps are clarified in the following two subsections.

C. The Reference FCT for the 2-Stage OTA

The single-ended two-stage OTA's small-signal model is shown in Fig. 6(b) [24]. From circuit theory, one can identify that the circuit has three poles and one zero. Typically, only two-poles of this circuit are of concern, as the third is assumed to be at a frequency much higher than ω_t. As a result, the frequency locations of the two-poles and the zero are approximated based on some assumptions as follows [23]–[25]:

$$\omega_{P\_3dB} = \frac{1}{g_{m6} R_{O1} R_{O2} C_{C1}} \tag{37}$$

$$\omega_{P1} = \frac{g_{m6} C_{C1}}{C_{Par} C_L + C_{C1} (C_{Par} + C_L)} \approx \frac{g_{m6}}{C_L} \tag{38}$$

$$\omega_{Z1} = -\left(\frac{g_{m6}}{C_{C1}} \right) \frac{1}{(1 - g_{m6} R_{C1})} \tag{39}$$

and the small-signal low-frequency gain is

$$A_{DC} = g_{m2} g_{m6} R_{O1} R_{O2} \tag{40}$$

The third pole $\omega_{P\_parasitic}$ - typically ignored in the analysis - has an important design value in the proposed theory and needs to be considered here. It can be approximated by [23]:

$$\omega_{P\_parasitic} = \frac{1}{C_{Par} R_{C1}} \tag{41}$$

where C_{par} represents the total shunt capacitance to ground on the output node of the first stage of the OTA and it consists of numerous parasitic elements.

The key step in designing the 2-stage OTA is to define the upper limit of ω_t; which is $\omega_{P\_parasitic}$ of Eqn. (41) as there is no design control over this parasitic pole. This upper value will determine the mechanism of scalability for higher stages, as will be discussed shortly. According to Eqn. (35), one can increase ω_t by increasing $A_{DC,N}$ (i.e., for $N = 2$), $\omega_{P\_3dB}, \omega_{P1}$ and reducing ω_{Z1}. However, since $A_{DC,2}$ has already been selected based on the designed-for gain of the system, and ω_{P1} is fixed for a certain C_L (here assumed to be 1 pF), one can increase ω_t by increasing ω_{P_3dB} and decreasing ω_{Z1}. To achieve this at the circuit level, and according to Eqs. (37) and (39), one can start with a minimum value of $C_{C1,(2-\text{stage})}$ that is at least 5 times the maximum parasitic capacitance given by a certain CMOS technology. Then, $R_{C1,(2-\text{stage})}$ ($\sim$ kΩ) is increased in value so that ($\omega_t \leq \omega_{P\_parasitic}$), or until the value of R_{C1} becomes impractical in the given technology. Also, increasing ω_t should be done such that the PM is greater than some desired value. Thus, those design conditions define the limitation on the values of C_{C1} and R_{C1}. Also, this will define the required design value of δ_{CL}, seen in Eqn. (22). At this point the design of the 2-stage OTA is complete and values of $C_{C1,(2-\text{Stage})}$ and $R_{C1,(2-\text{Stage})}$ are shown in Table III. With such small values of C_{C1}, most of the current at the output branch will be used to charge C_L, hence, the step response will settle faster.

D. Scalable FCT for 3-, 4-, 5-, 6-, 7- and 8-Stage OTAs

To design the 3-stage OTA, a new gain-stage is added to the 2-stage OTA as depicted in Fig. 5. Also, to design

TABLE III
COMPONENT VALUES USED IN THE COMPENSATION CIRCUITS FOR THE REALIZATION OF DIFFERENT OTA STAGES

Component / OTA stage	Compensation Capacitors (pF)							Compensation Resistors (KΩ)						
	C_{C1}	C_{C2}	C_{C3}	C_{C4}	C_{C5}	C_{C6}	C_{C7}	R_{C1}	R_{C2}	R_{C3}	R_{C4}	R_{C5}	R_{C6}	R_{C7}
2-stage OTA	0.05	-	-	-	-	-	-	180	-	-	-	-	-	-
3-stage OTA	0.25	0.05	-	-	-	-	-	100	60	-	-	-	-	-
4-stage OTA	0.5	0.25	0.05	-	-	-	-	80	60	50	-	-	-	-
5-Stage OTA	2	0.5	0.25	0.05	-	-	-	60	40	40	60	-	-	-
6-stage OTA	4	2	0.5	0.25	0.05	-	-	40	40	40	40	40	-	-
7-stage OTA	8	4	2	0.5	0.25	0.05	-	40	40	30	30	30	50	-
8-stage OTA	12	8	4	2	0.5	0.25	0.05	40	40	35	35	30	25	20

a 4-stage OTA, two gain-stages are added to the 2-stage OTA, and so on. Each new gain-stage comes with its own compensation circuit. Consequently, a new *P-Z* pair will be added to the *TF* with each new stage as described in Eqn. (2). Also, according to Eqn. (35), ω_t will significantly increase, as $A_{DC,N}$ will also increase. However, this new value of ω_t will most likely exceed the previously defined upper limit of ω_t. Therefore, it would be necessary to re-adjust the value of ω_t by re-positioning the poles and the zeros, according to Eqn. (36), whenever a new stage is added. This can be done by re-sizing the compensation circuit with the addition of each new stage.

Instead of deriving new equations for the poles and zeros for each stage separately, and by knowing that the *P-Z* pairs have an inverse relationship with R_C and C_C, the values which were found for the 2-stage OTA can be scaled to size the compensation circuits of higher OTA stages. Interestingly, since the poles and zeros are positioned according to Eqn. (36) and since the maximum ω_t is defined, the sizes of the R-C compensation circuit components follow a certain pattern in order to position the *P-Z* pairs when a new gain-stage is added. This scalable pattern can be seen in Table III and can be described as follows: whenever a new stage is added, the compensation capacitors of the previous stages are increased in size to decrease the frequency of the poles of the new OTA stage, and hence help in reducing ω_t to its defined upper limit (i.e., lower than the parasitic pole). Since no exact positioning of the *P-Z* pairs is required, the amount of increment in C_Cs of the previous stage is being decided by observing the poles' positions – to make sure that they are at frequencies less than ω_t. Therefore, quantitative patterns are found (by simulations) to increase C_Cs for different stages uniformly. These uniform quantitative patterns of increasing C_Cs can be described by:

$$C_{Ci,(N-stage)} > C_{Ci,[(N-1)-stage]}, \quad 1 \le i \le N-1 \quad (42)$$

and

$$C_{C(i-1),(N-stage)} = C_{C(i-2),[(N-1)-stage]}, \quad 3 \le i \le N \quad (43)$$

Thus, the new compensation capacitor ($C_{C(N-1),(N-stage)}$) is sized to the minimum capacitance value, which was found for the 2-stage OTA (i.e., $C_{C(N-1),(N-stage)} = C_{C1,(2-stage)}$).

Sizing C_Cs according to these patterns will change the poles and zeros positioning (i.e., reducing them) simultaneously, hence, according to Eqn. (35), ω_t might not be reduced to frequencies less than $\omega_{P\_parasitic}$. Also, sizing C_Cs only, might not satisfy the *P-Z* arrangement of Eqn. (36). Therefore, to make sure that $\omega_t \le \omega_{P\_parasitic}$, and to satisfy the arrangement of the poles and zeros according to Eqn. (36), the compensation resistors will be sized according to an opposite pattern of sizing C_Cs; that is: whenever a new stage is added, the compensation resistors of the previous stage are reduced to increase the frequency of the zero of the new OTA stage, and hence reduce ω_t to its defined upper limit (i.e., lower than the parasitic pole). The amount of change in R_Cs of the previous stage is being decided by observing the OTA stability via simulations. In a similar fashion of sizing C_Cs, quantitative patterns are being used to initially size the R_Cs. Therefore, once adding a new stage, the reduction in R_Cs can be described as (i.e., vertical pattern):

$$R_{Ci,(N-stage)} \le R_{Ci,[(N-1)-stage]}, 1 \le i \le N-1 \quad (44)$$

while the new compensation resistor (i.e., $R_{C(N-1),(N-stage)}$) is initially sized according to the following condition (i.e., diagonal pattern)

$$R_{C(N-1),(N-stage)} \le R_{C(N-2),(N-stage)} \quad (45)$$

Table III shows the R_Cs' sizes for the different OTA stages and clarifies these patterns. Apart from $R_{C4,(5-stage)}$ and $R_{C6,(7-stage)}$, which are increased for better PM, all sizes follow from Eqn. (44). Also, apart from $R_{C3,(8-stage)}$ and $R_{C4,(8-stage)}$, which are increased for better PM, all sizes follow from Eqn. (45).

One of the design limitations in the proposed technique is the maximum number of stages one can reach. Once going to $N = 9$, it becomes very challenging to set ω_t below $\omega_{P\_parasitic}$ with the proposed FCT, hence the OTA may lose its stability in closed loop.

E. Simulation Results and Robustness Tests

To verify the proposed 2- to 8-stage OTA design, extensive simulations were conducted (using Cadence) based on the standard 65 nm TSMC CMOS process operating on a $V_{DD} = 1$ V, addressing all possible operation modes of the OTA.

Fig. 7(a) shows the open-loop *AC* response of the 2- to 8-stage CMOS OTAs. Since the proposed OTA is meant for closed-loop operations, a test of its stability under large and small input-signals is shown in Fig. 7(b). These simulations have been conducted for all stages as reported in [14], but, for simplicity, part of these transient responses is being shown here. Apart from the overshoot that can be seen in the step response, the closed-loop operation is stable. Also, a test for design robustness using A_{DC} Monte-Carlo (MC) simulations for the 8-stage CMOS OTA is provided in Fig. 7(c), where the relative percent error of less than 1.5% were obtained. A summary of these results is shown in Table IV.

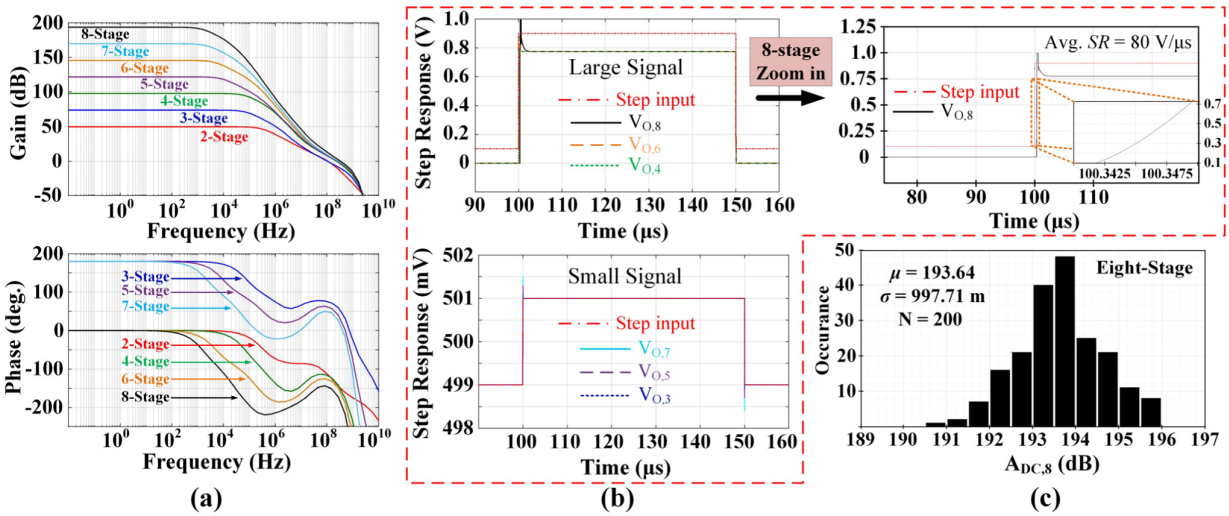

Fig. 7. Simulation results, stability and robustness tests of the proposed OTA design of Fig. 5: (a) the open-loop *AC* response of the 2- to 8-stage OTAs, (b) stability tests, using the closed-loop unity-gain step response of the proposed 4-, 6-, and 8-stage OTAs subject to a large signal of 800 mV (upper part) with a zoom-in at the 8-stage rising edge behavior (to its right side) where it exhibits a Slew-Rate of 80 μV/s, and stability test for 3-, 5-, and 7-stage OTAs subject to a small signal of 2 mV (lower part), and (c) A_{DC} MC simulations for the 8-stage OTAs.

TABLE IV

SUMMARY OF RESULTS AND PERFORMANCE COMPARISON WITH MOST RECENT PUBLISHED WORKS

Reference / Metric	[20] 2003	This Work	[12] 2020	[11] 2020	This work	[7] 2015	[6] 2020	This work	[5] 2016	This work	This work	This work	This work
# of Stages	Two-stages		Three-Stages			Four-Stages			Five-Stages		6-stage	7-stage	8-stage
CMOS process	500nm	65nm	180nm	130nm	65nm	350nm	130nm	65 nm	130nm	65 nm	65 nm	65 nm	65 nm
V_{DD} (V)	2.5	1	0.3	1	1	3	1.2	1	1.2	1	1	1	1
DC gain (dB)	94	50	98.1	72.4	73.7	173	107	97.75	150	121.7	145.7	168	193.6
GBP (MHz)	300	87.7	0.0031	4.23	363.1	2.9	2.75	2807.7	885437	10945.6	84811	442092	6253570
Power (µW)	15800	38.8	0.013	95	66.9	156	175.2	94.9	10200	123	150.9	178.9	206.9
C_L (pF)	12	1	30	90	1	1000	400	1	1	1	1	1	1
ω_t (MHz)	94	128.6	0.0031	4.23	103.7	2.9	2.75	231.8	20	248.1	276.3	215.5	331.3
T_S at 1% (µs)	0.013	0.031	-	0.2	0.173	0.46	0.33	0.069	1.27	1.25	0.295	6.84	0.885
T_S at 0.01%(µs)	0.02	0.08	-	-	0.316	-	-	0.16	-	2.08	0.655	10.45	1.89
FOM_S	0.22	2.26	7.1	4	5.4	18.5	6.2	29.5	86.8	88.98	565.4	2471.1	30225.08
$SIFOM_L$	17.5	72.9	-	20	31	40.2	18.7	427.5	68.3	71.1	1916.6	361.2	34152.6

In order to appreciate the advantages of the presented many-stage OTA design, it is important to compare the results presented here with other recent works that report different designs of multi-stage OTAs. In order to facilitate this comparison, a small signal figure-of-merit (FOM_S) and a large signal figure-of-merit ($SIFOM_L$) are defined as [5]:

$$\text{FOM}_\text{S} = \frac{\text{GBP} \cdot \text{C}_\text{L}}{\text{Power}}, \text{SIFOM}_\text{L} = \frac{\text{GBP} \cdot \text{C}_\text{L}}{T_S \cdot \text{Power}} \tag{46}$$

It is evident from Table IV that the proposed design compares well to recent 2- and 3-stage designs, while outperforming those with 4- and 5-stage. Notably, 6-, 7-, and 8-stage OTAs have not been reported in literature before. Clearly, the 6-, 7-, and 8-stage OTA significantly outperforms all other stages.

VI. VERIFICATION AND VALIDATION OF THE PROPOSED THEORY HAVING ONE POLE-ZERO PAIR

Figure 3 of Section III summarizes the results from the proposed theory with only one *P-Z* pair. Therefore, the following subsections are verifying and validating the results of Fig. 3 by designing the 2-stage OTA (i.e., $N = 2$) of Fig. 5.

TABLE V

DEVICES' SIZES OF THE TWO-STAGE OTA OF FIG. 7 FOR THE PURPOSE OF VERIFYING δ_{CL} WITH $V_{BIAS} = 0.39$ V

Device	Aspect Ratio/size	Device	Aspect Ratio/size		
$M_1 = M_2$	(2 µm / 390 nm)	$M_{6,2}$	(23 µm / 120 nm)		
$M_3 = M_4$	(1.2 µm / 325 nm)	$M_{7,2}$	(15 µm / 240 nm)		
M_5	(4 µm / 520 nm)	C_{C1}	10 pF	R_{C1}	35 KΩ

A. The P-Z Doublet Separation Distance (δ_{CL}) vs. the P-Z Pair Separation Ratio (ω_{P1} / ω_{Z1})

Since the theoretical analysis suggested that changing ω_{P1} and A_Z is the way to control δ_{CL}, the conventional two-stage CMOS OTA of Fig. 5 has been designed to verify and validate this. The initial design has been done without optimization to keep the values flexible as a wide range of values for ω_{P1} is required. Therefore, the initial design has been done by fixing ω_{P_3dB} and ω_{Z1} at 5 KHz and 460 KHz, respectively, (by fixing the values of C_{C1}, R_{C1} and $g_{M6,2}$ (i.e., aspect ratio of $M_{6,2}$) as seen in Table V). Consequently, the performance will be controlled by sweeping ω_{P1}. For A_{DC} of 56.4 dB at $V_{DD} = 1$ V, ω_{P1} has been swept to sweep the ratio

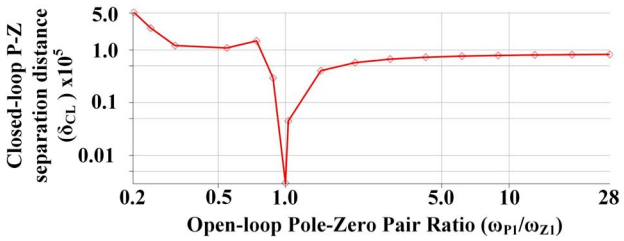

Fig. 8. The closed-loop pole-zero separation distance (δ_{CL}) as a function of (ω_{P1}/ω_{Z1}) to verify part of the theory which is reported in Eqn. (21) and Fig. 3(a).

TABLE VI

DEVICES' SIZES AND RESULTS SUMMARY OF FABRICATED TWO-STAGE CMOS OTA OF FIG. 5 AND FIG. 6(a)

Device	size			Metric	Value
M_1= M_2	2 x (1 µm / 390 nm)			Process	65 nm
M_3= M_4	8 x (0.75 µm / 325 nm)			V_{DD}	1.2 V
M_5	4 x (1.1 µm / 520 nm)			Gain	50.5 dB
$M_{6,2}$	8 x (0.55 µm / 130 nm)			BW	29.8 KHz
$M_{7,2}$	10 x (0.66 µm / 260 nm)			Area	(95 µm x 35 µm)
M_{C1}	1 x (1 µm / 390 nm)			Power	110 µW
C_{C1}	50 fF	C_L	1 pF	V_{CM_REF}	0.53 V

of (ω_{P1}/ω_{Z1}) between 0.2 to 28, by sweeping the value of C_L between (20 pF and 10 nF).

Fig. 8 shows δ_{CL} as a function of (ω_{P1}/ω_{Z1}). The results in Fig. 8 clearly satisfy the claim in Eqn. (21) along with the results seen in Fig. 3(a). Although some values of δ_{CL} are off when (ω_{P1}/ω_{Z1}) < 1, due to the coupling between ω_{P_3dB} and ω_{P1}, the overall behavior verifies the proposed analysis in Section III regarding δ_{CL}.

B. Settling Time vs. LF Zero Gain (A_Z)

Figure 3(b) and (c) of Section III show the settling time as function of A_Z and ω_P (i.e., ω_{P1}/ω_{Z1}), respectively. To validate these relationships, the two-stage OTA of Fig. 5 has been fabricated using standard TSMC 65 nm CMOS process. Fig. 9(a) shows the microphotograph of the fabricated chip. The design parameters of the fabricated chip are shown in Table VI.

Here a wide range of values for A_Z and (ω_{P1}/ω_{Z1}) are required. But, once the circuit is being fabricated, changing circuit parameters becomes challenging. Therefore, controlling the values of A_Z and (ω_{P1}/ω_{Z1}) are limited. Nevertheless, in this experiment setup, we were able to sweep A_Z by sweeping the values of ω_{Z1}. This has been achieved by having an off-chip R_{C1}, as seen in the PCB of Fig. 9 (b), to control the position of ω_{Z1}.

Simulation results of Fig. 10 shows that by sweeping R_{C1} from 20 KΩ to 125 KΩ, A_Z is swept from 0.6 dB to 23 dB, where ω_{Z1} is decreasing form 167 MHz to 25.8 MHz. Once R_{C1} is increased beyond 125 KΩ, the parasitic poles will start to appear next to ω_t.

Since increasing R_{C1} will increase A_Z, then if one increases R_{C1} and observe the settling time, the relationship between A_Z and settling time when having one *P-Z* pair can be revealed. Fig. 11 shows the closed-loop unity-gain step response for schematic and post-layout simulations in Fig. 11(a), and the measurement results in Fig. 11(b) (based on the fabricated chip of Fig. 9) for the minimum and the maximum values

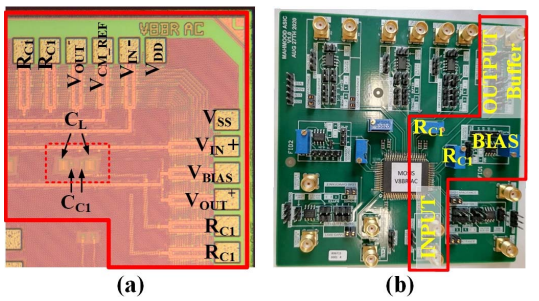

Fig. 9. The fabricated differential-ended two-stage CMOS OTA of Fig. 7: (a) the chip's microphotograph, and (b) the PCB showing off-chip R_{C1} for controlling purposes.

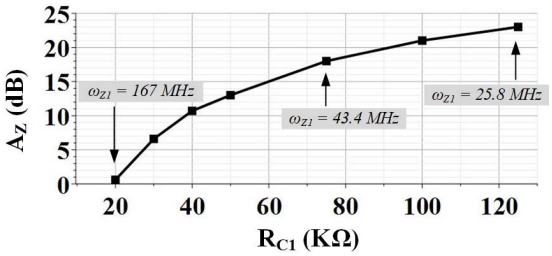

Fig. 10. The low-frequency zero gain (A_Z) as a function of R_{C1}.

of R_{C1}. It is clear from Fig. 11(b) that the step response settles faster when $R_{C1} = 128$ KΩ. Also, Fig. 11(c) shows the design robustness against PVT variations for open-loop (upper part) and closed-loop (lower-part) responses. Based on these PVT simulations, the maximum ω_t was obtained at the Fast-Slow (FS) corner with a value of 191 MHz and a PM of 62°, while the minimum ω_t was obtained at Slow-Slow (SS) corner with a value of 140 MHz and a PM of 52.4°.

Fig. 12 summarizes the relationship between R_{C1} (i.e., the increase in A_Z according to Fig. 10) and the settling time. This figure clearly validates the theory in Fig. 3(b), and it is true for schematic, post layout, and measured results. Also, it is true when the response settles to 1% and 0.01% of the final value.

VII. VERIFICATION OF THE PROPOSED THEORY HAVING N-1 POLE-ZERO PAIRS

Clearly, the circuit of Fig. 5 increases the gain and adds *P-Z* pairs whenever a new stage is added. Thus, sweeping the gain for a specific number of *P-Z* pairs to verify the theory in Fig. 4(b) and (c) is practically challenging. Nevertheless, one can still measure the improvement in settling time by comparing the settling time at 0.01% of the final value to the settling time at 1% for each stage, where this was the main issue of having *P-Z* doublets as stated in [16]. But, in [16], the impact of the *P-Z* doublets has been discussed having only one *P-Z* pair. However, by adding more *P-Z* pairs (when increasing the number of stages) it is important to consider the impact of these extra *P-Z* pairs compared to having one *P-Z* pair. Consequently, the Improvement Metric (*IM*) can be given by

$$IM = \frac{Settlingtime@0.01\%}{Settlingtime@1\%} \times \frac{1}{N-1}. \quad (47)$$

where (N-1) represents the number of *P-Z* pairs/doublets the OTA will have in its frequency range of operation.

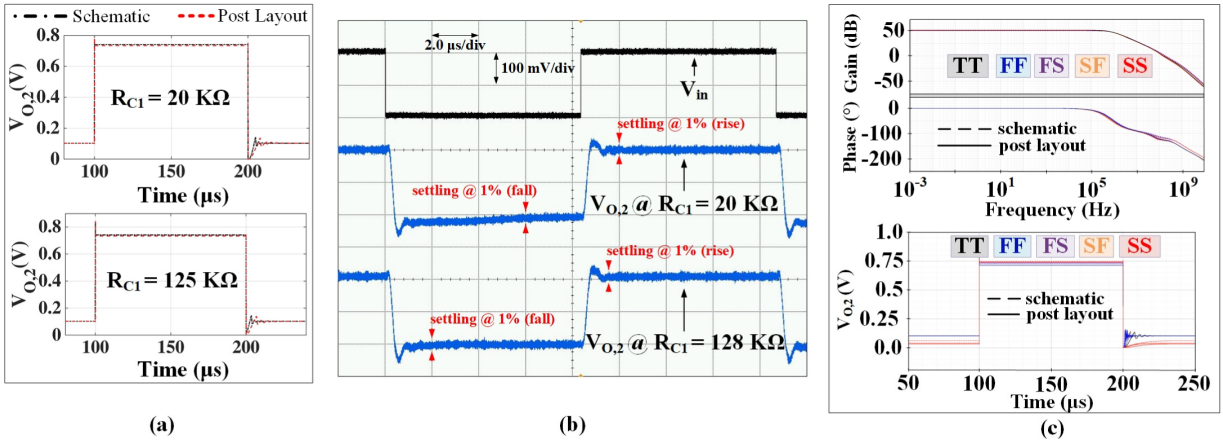

Fig. 11. The closed-loop unity-gain step response results: (a) schematic and post-layout simulations for R_{C1} = 20 KΩ (upper part) and R_{C1} = 128 KΩ (lower part), (b) measured step response when applying a step input of 200 mV for R_{C1} = 20 KΩ and R_{C1} = 128 KΩ, and (c) The open-loop (upper part) and the closed-loop (lower part) responses under different process corners to show the design robustness against PVT variations for both schematic and post-layout simulations and for R_{C1} = 20 KΩ.

TABLE VII

COMPARING THE IMPACT OF GAIN AND NUMBER OF *P-Z* PAIRS ON SETTLING TIME BETWEEN THEORY AND CIRCUIT SIMULATIONS

	Metric	N = 2	N = 3	N = 4	N = 5	N = 6	N = 7	N = 8
Theory -Based on Eqn. (31)-	**Gain: A_Z (dB)**	**50**	**75**	**100**	**125**	**150**	**175**	**200**
	Settling time @ 1% (sec)	0.016	0.297	0.885	1.26	1.55	1.75	1.93
	Settling time @ 0.01% (sec)	3.45	4.83	5.4	5.75	6.05	6.22	6.39
	***IM in settling time* (theory)**	**215.6**	**8.1**	**2.03**	**1.1**	**0.78**	**0.59**	**0.47**
Circuit Realization -Based on Fig. 5-	DC Gain, Settling time (T_S) @ 1%, and Settling time (T_S) @ 0.01% are taken from Table V							
	***IM* in settling time (circuit)**	**2.58**	**0.91**	**0.77**	**0.42**	**0.44**	**0.25**	**0.3**

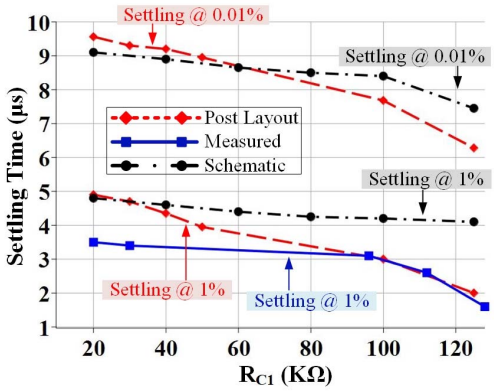

Fig. 12. Settling time behavior when sweeping R_{C1} from 20 KΩ to 125 KΩ (i.e., sweeping A_Z form 0.6 dB to 23 dB) for the case of having one *P-Z* pair.

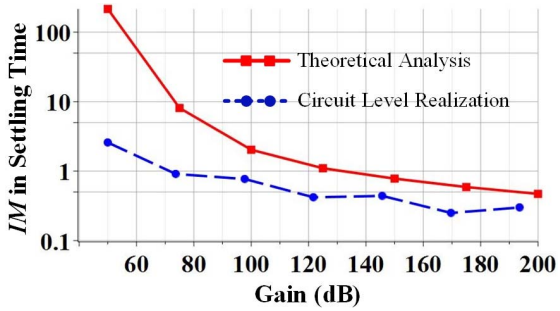

Fig. 13. The Improvement Metric (*IM*) in settling time when increasing the gain for both theory and circuit level realization.

Table VII compares the settling time results which are obtained based on the circuit level simulations with the results which are obtained by the theory in Section V (i.e., Eqn. (31) and Fig. 4). The results are obtained here for the same conditions in both cases: theory and circuit level realization. This means that the gain (i.e., the number of stages N) is almost equal for both cases. Also, the same *P-Z* pairs' numbers are ensured while obtaining the settling time for these two cases.

Fig. 13 shows how *IM* is decreasing when increasing the gain. This is true for both theory and circuit realization; thus, it verifies the proposed theory in Section IV.

However, the decrease in *IM* for the circuit level realization is not uniform compared to the theoretical behavior. The reason is that the distance between all open-loop *P-Z* pairs in theory is 1 rad/s, whereas the distance between the open-loop *P-Z* pairs in the circuit realization of Fig. 5 is not uniform.

Also, it is expected to have the lowest *IM* when $N = 8$, but *IM* for $N = 7$ is slightly lower in the circuit level realization. The reason is the *P-Z* cancellation of the 1st and 2nd *P-Z* pairs in the 7-stage OTA, where $\omega_{P1,7}$ and $\omega_{Z1,7}$ are allocated at -2.288 x10^4, while $\omega_{P2,7}$ and $\omega_{Z2,7}$ are allocated at -1.236×10^6. Thus, two *P-Z* pairs are with almost no impact in the closed-loop operation of the 7-stage OTA.

Finally, increasing the circuit gain while having *LF* zeros is not only important in reducing the impact of *P-Z* pairs on settling time, but it also paves the way to design Many-Stage CMOS OTAs while having many *P-Z* pairs.

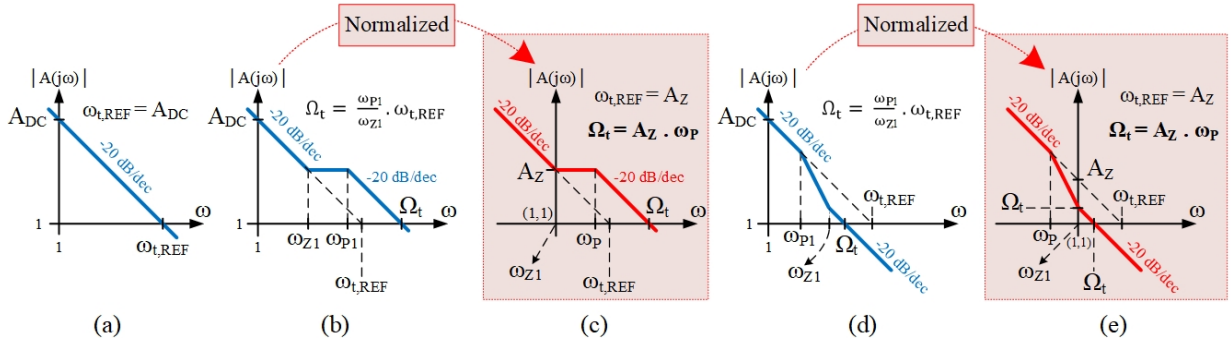

Fig. 14. Integrator-based OTA magnitude response: (a) response with no *P-Z* compensator, (b) response with *P-Z* compensator ($\omega_{Z1} < \omega_{P1}$), (c) frequency normalized response of (b), (d) response with P-Z compensator ($\omega_{P1} < \omega_{Z1}$), and (e) frequency normalized response of (d).

VIII. Conclusion

A new generalized relationship between frequency response and settling time was presented in this work addressing the impact of P-Z pairs/doublets on CMOS OTAs. The proposed theory showed that using low frequency zeros and cascaded-gain stages reduces the impact of *P-Z* pairs on the settling time of CMOS OTAs. Interestingly, it was shown that increasing the number of gain-stages reduces the impact of *P-Z* pairs, while having such *P-Z* pairs helps stabilize the OTA. Consequently, the proposed theory has revealed un-tapped opportunities for the design of Many-stage CMOS OTAs. A design example of a 2- to 8-stage CMOS OTA was presented, in order to validate and verify the proposed theory, where the standard 65 nm TSMC CMOS process was used for the design of the OTA.

Appendix A
Reducing the Transfer Function Complexity of the 2-Stage CMOS OTA

Frequency scaling is a mathematical technique of shifting the poles and zeros of a *TF* to a new location in the complex s-plane, while maintaining the same functional behavior albeit over a different frequency range, i.e.,

$$A\,(p) = A\,(s)|_{s=p/a} \tag{48}$$

In this work, frequency normalization is used to reduce the number of coefficients in the *TF* of Eqn. (3), as this serves to simplify the presentation. However, before performing the normalization on Eqn. (3), and since integrators are ideally at the core of all OTA implementations, lets us consider having a DC pole and a finite pole instead of 2 finite poles. Therefore, the *TF* of Eqn. (3) is now described as an integrator function in the Laplace domain with a DC gain, $A_{DC} = A_1 A_2$, and a *P-Z* pair as follows

$$A\,(s) \approx \frac{A_{DC}}{s} \times \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)} \tag{49}$$

This assumption will have some practical implications at frequencies $< \omega_{P\_3dB}$. However, the proposed theory deals with the *P-Z* pair which are allocated at frequencies $> \omega_{P\_3dB}$, thus, these practical implications will be of no significance.

The magnitude response of an undamped integrator is shown in Fig. 14(a) and can be written with a scale factor A_{DC} as: $\left[A\,(s) = A_{DC}/s\right]$. Here A_{DC} represents the magnitude of the *TF* at 1 rad/s. However, as an alternative perspective, A_{DC} can also be viewed as the frequency at which the magnitude of the *TF* is unity (which will be referred to as $\omega_{t,REF}$) as depicted by Fig. 14(a). Thus, the frequency and magnitude axes intercept points form an isosceles right-angled triangle. By introducing the *P-Z* pair, the *TF* will be written as Eqn. (49).

For the case, 1 rad/s $\leq \omega_{Z1} < \omega_{P1}$, the magnitude of the TF will appear as that shown in Fig. 14(b). The net effect of this *P-Z* arrangement is that $\omega_{t,REF}$ of the compensated OTA increases to Ω_t. Inspecting the plot in Fig. 14(b), one can deduce that

$$\Omega_t = \frac{\omega_{P1}}{\omega_{Z1}} \cdot \omega_{t,REF} = \frac{\omega_{P1}}{\omega_{Z1}} \cdot A_{DC} \tag{50}$$

Clearly, the greater the frequency distance between the *P-Z* pair, the higher the unity-gain frequency achievable.

For the case when 1 rad/s $\leq \omega_{P1} < \omega_{Z1}$, then a different magnitude response appears as shown in Fig. 14(d). In this case Ω_t is less than $\omega_{t,REF}$. Even though $\omega_{P1} < \omega_{Z1}$ the expression for Ω_t is the same as that listed in Eqn. (50).

OTAs are required to operate over a large range of frequency conditions. Rather than design a new TF for each case, a better approach is to normalize the *TF* with respect to 1 rad/s and then translate the *TF* such that the zeros are shifted to a new location. On doing so, the poles of the *TF* are shifted as well. In this work, the frequency normalization was performed by setting ω_{Z1} to 1 rad/s, such as that shown in Fig. 14(c) and (e). Also superimposed on this figure is the frequency-normalized unity-gain frequency Ω_t in terms of the open-loop parameters, where it can be written as in Eqn. (16).

To rewrite the open loop *TF* of Eqn. (49) using the normalized approach, the "*s*" Laplace variable will be replaced with the normalized "*p*" Laplace variable (i.e., $p = s/\omega_{Z1}$). On doing so, Eqn. (49) would be written as in Eqn. (15), where ω_{Z1} is always assumed to be at 1 rad/s and the value A_Z is always the gain of the integrator at $\omega_{Z1} = 1$ rad/s, regardless of the relation between ω_{P1} and ω_{Z1}. The same concept can be generalized for *N*-stages to derive Eqn. (25) and (32).

Appendix B
Derivation of the Unity Step Response

Based on the results found in Eqs. (18), (19) and (22), the closed loop *TF* of Eqn. (17) can be approximated as

$$T\,(p) = \frac{(p+1)}{\left(1 + \frac{p}{A_Z \omega_P}\right)\left(1 + \frac{p}{(1+\delta_{CL})}\right)} \tag{51}$$

Then the unit step response $y(t)$ can be written as

$$y(t) = 1 - \left(\frac{A_Z\omega_P}{A_Z\omega_P - 1 - \delta_{CL}}\right)(1+\delta_{CL})\,e^{-A_Z\omega_P t} + \left(\frac{A_Z\omega_P}{A_Z\omega_P - 1 - \delta_{CL}}\right)\delta_{CL}e^{-(1+\delta_{CL})t} \quad (52)$$

Based to Eqn. (16), and as $A_Z\omega_P \gg 1$, $y(t)$ can be reduced to

$$y(t) \approx 1 - (1+\delta_{CL})\,e^{-A_Z\omega_P t} + \delta_{CL}e^{-(1+\delta_{CL})t} \quad (53)$$

where δ_{CL} is given by Eqn. (21). It is interesting to note that exponential term with a *LF* time constant has a multiplicative term that depends directly on δ_{CL}. From Eqn. (21), δ_{CL} depends on two parameters from the open loop response, A_Z and ω_P.

The unit step response can be simplified by substituting Eqn. (21) into (53) and then written as in Eqn. (23).

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