# Guest Editorial: Special Issue Based on the 12th Edition of the Latin American Symposium on Circuits and Systems

THE Latin American Symposium on Circuits and Systems (LASCAS) is the flagship conference in Latin America (IEEE Regions 9) by the IEEE Circuits and Systems Society (CASS). This conference contributes since more than a decade to its history by reporting the latest research results and innovations across the themes within the scope of the society, including analog, digital, and mixed-signal electronics, signal processing, power electronics, communication theory, sensors, circuit theory, and nonlinear circuits and systems.

The 12th edition was supposed to be held in-person at Arequipa, Peru, but was held virtually on February 22–25, 2021, and received 149 paper submissions. The best papers were evaluated by the technical committees and invited to the Special Issue of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS (TCAS-I). The five articles went through a peer-reviewed process consisting of world-recognized reviewers in related fields. A brief description of the selected articles is as follows.

In [1], Passos *et al*. employ a two-step method with feature space mapping and classification with, first, the body parts segmented through a deep neural network architecture and then, the use of Gait Energy Image to encode the motion of the body parts. They have evaluated their method on three challenging Brazilian sign language datasets.

In [2], Pinheiro *et al*. report a three-stage charge pump with forward body biasing in 28 nm UTBB FD-SOI CMOS, which is appropriate for thermoelectric and photo-voltaic energy harvesting. Taking advantage of the FD-SOI substrate characteristics, the forward-body-biasing (FBB) technique is used in order to improve the switch conductances and shows a maximum efficiency peak of 56% at input voltage of 300 mV and load current of 100 nA.

In [3], Schrape *et al.* demonstrate how a standard non-rad-hard flip-flop can be converted into a rad-hard flip-flop without modifying its internal structure. They present five variants of a triple modular redundancy (TMR) flip-flop. It features differing performance, thus enabling to choose an optimal solution for every sensitive node in the circuit. Several flip-flop designs have been validated on IHP's 130-nm BiCMOS process, by irradiation of custom-designed shift registers.

In [4], Juracy *et al*. reported that a path to enable the deployment of CNNs in energy-constrained devices is adopting hardware accelerators for the inference phase. The authors propose a framework to explore CNNs design space, providing power, performance, and area (PPA) estimations using the system simulator front-end, TensorFlow. The results provide a rich design space exploration, enabling selecting the best set of CNN parameters to meet the design constraints.

In [5], Abich *et al.* investigate the relationship between soft errors and model accuracy with an extensive soft error assessment of the MobileNet model running on an Arm Cortex-M processor. It promotes the use of a register allocation technique (RAT). Results show that RAT gives the best relative performance, memory utilization, and soft error reliability tradeoffs.

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