The Analog Behavior of Pseudo Digital Ring Oscillators Used in VCO ADCs

Jonas Borgmans, Robbe Riem, and Pieter Rombouts, *Senior Member, IEEE*

***Abstract*— In this work, we focus on the three most relevant pseudo-digital ring oscillator circuits for VCO A/D conversion. First, we show that they can be accurately modeled by an equivalent 2-terminal diode-like element. Next, we study the main analog performance figures: the effective oscillation frequency (which affects the quantization noise of a VCO ADC), the input referred noise and the power efficiency both for voltage and current control. We do this both through theoretical modeling as well as through simulations, which are in good agreement with each other. Our study highlights several important independencies: e.g. most performance metrics are independent on the number of VCO stages and the external load capacitance on the VCO nodes. In contrast to these independencies, we identify several important dependencies. In particular, we show that the biasing of the ring has an enormous impact on power efficiency of the ring. This dependency is different for the case of a voltage- or current mode configuration of the ring.**

***Index Terms*— VCO A/D-conversion, ring oscillator, input referred noise, power efficiency.**

I. Introduction

OVER the past years Voltage-Controlled Oscillator (VCO)-based Analog-to-Digital Converters (ADCs) or VCO ADCs have evolved into a viable technology for oversampling A/D conversion. Advantages of this approach include inherent first-order noise shaping, intrinsic anti-aliasing as well as the fact that the circuits are digital-friendly, enabling enhanced design portability and shorter design cycles [1], [2]. The core building block of most of these VCO ADCs is an inverter-based ring oscillator.

We can distinguish three main performance metrics for VCO ADC systems: linearity, noise and power consumption. Linearity issues in VCO ADCs can be tackled by the use of a pseudo-differential setup [3] and by employing proper architectural techniques such as two-stage [4], [5] or feedback based architectures [6]–[12], etc. Circuit-level improvements also exist in prior art [13]–[15] and as a last resort, digital calibration [16]–[20] can be used. In this work we will not address linearity any further. Instead, we will study the electrical behavior with a focus on noise and power efficiency.

Manuscript received November 20, 2020; revised February 2, 2021; accepted April 12, 2021. Date of publication April 23, 2021; date of current version June 4, 2021. This work was supported by the Fund for Scientific Research Flanders (FWO-Vlaanderen), Belgium. This article was recommended by Associate Editor E. Cantatore. *(Corresponding author: Jonas Borgmans.)*

The authors are with the Department of Electronics and Information Systems (ELIS), Ghent University, 9052 Gent, Belgium (e-mail: jonas.borgmans@ugent.be).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2021.3073817.

Digital Object Identifier 10.1109/TCSI.2021.3073817

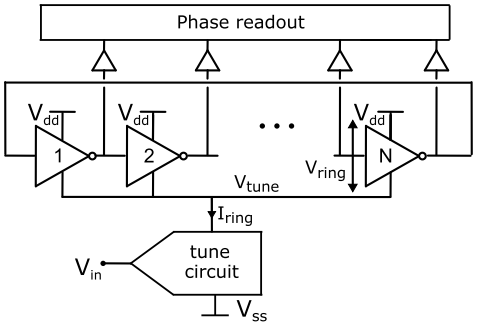

Fig. 1. Simple inverter based ring oscillator VCO with a tune circuit and phase readout for use in a VCO ADC.

There are already numerous publications on the noise in simple CMOS ring oscillators e.g. [21]–[24]. In this work we will build on these results. For this, we will extend the existing analysis on the simple inverter based oscillator to two other important inverter based ring oscillators. Moreover, while prior work focuses on the output phase noise, we will focus on the input referred VCO noise, which allows a much more complete and intuitive analysis of the performance of VCO ADCs. This analysis will allow a comprehensive comparison between the different types of ring oscillators.

To enable this analysis, we will first develop a VCO modeling technique in Section II. In Section III, we delve deeper into the VCO circuits, to obtain intuitive expressions for the delay of our three ring oscillators. Based on these models, we will then analyze the noise in Sections IV and V. The power efficiency is discussed in Section VI and finally, we will conclude the paper in Section VII.

II. VCO Modeling: 2-Terminal Model of Pseudo-Digital Ring Oscillators

A. Constructing the Ring Oscillator

We consider an oscillator as *pseudo-digital* when its core circuit can be constructed with simple digital cells, preferably CMOS inverters. A conceptual schematic of the simplest *pseudo-digital* ring oscillator is shown in Fig. 1. It consists of N unit cells which produce a pseudo-digital output signal (either high or low). These unit cells are connected in a ring, forming a feedback loop such that there is an oscillating solution for the voltages in the circuit. In a VCO ADC application, which is the focus of this work, the output of each unit cell is buffered and routed to a phase readout circuit to obtain the actual digital output signal [1]. Fig. 1

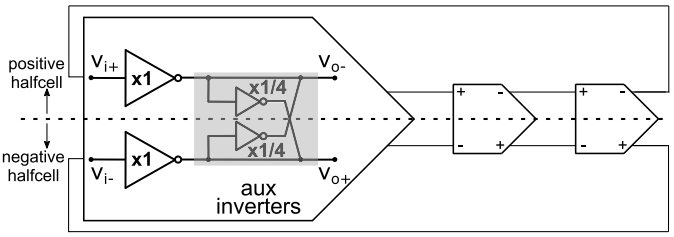

Fig. 2. Three-stage voltage-controlled ring oscillator based on the direct cross-coupled delay cell.

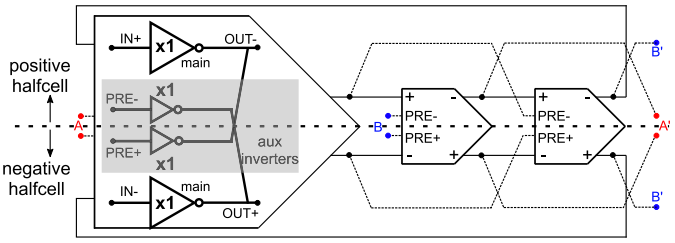

Fig. 3. Three-stage voltage-controlled ring oscillator based on feed-forward cross-coupled delay cells. Note: A-A' and B-B' are implicitly connected.

shows the configuration where the unit elements are inverters. This configuration will be later referred to as the simple ring oscillator or *Simple RO*. Finally, to obtain a voltage control mechanism, a generic tune circuit is added to allow the input voltage V_{in} to control the oscillation frequency. In this work we will make, to a large extent, abstraction of the tune circuit and we will focus on the core ring oscillator circuit instead.

B. Differential Delay Cells

Next to the single-ended unit cell used in the VCO ADC system of Fig. 1, differential unit cells are also frequently used. A very popular differential delay cell used in VCO ADCs is displayed in Fig. 2 [25]. The cell consists of two *main* inverters which form the core signal path. To this, a direct cross-coupling through two (small) *auxiliary* inverters is added. The goal of these auxiliary inverters is to create a balancing mechanism to ensure that both outputs are complimentary, such that the overall cell maintains a differential behavior. In most designs, these auxiliary inverters will be sized significantly smaller than the main inverters. More specifically, a typical sizing for these auxiliary inverters is to size them a quarter of the main inverters [14], [25], [26]. This configuration will be later referred to as the direct cross-coupled case or *Direct CC*.

Recently, an improvement on the established direct cross-coupled delay cell of Fig. 2 was proposed [14], [27]. The core circuit idea is shown in Fig. 3. Again the actual signal path is formed by the *main* inverters. As before, auxiliary inverters are added to create a balancing mechanism. However, now the auxiliary inverters for stage k are driven from the outputs of stage $k-2$ which are fed forward [28]. This cell was studied in [14] and it was shown to have improved performance in terms of frequency, power, noise and robustness. Moreover, the best sizing for the auxiliary inverters is very different from the cell with direct cross-coupling of Fig. 2: now the best sizing is to size the auxiliary inverters with equal strength as the main inverters. This configuration will be later referred to as the feed-forward cross-coupled case or *FF-CC*.

The three ring-oscillators presented above will be the focus of the remainder of this work.

C. Frequency Characteristic

Moving forward with our VCO model, we will now study the frequency characteristic of the three ring oscillators. We will start our analysis with a constant input signal V_{in} such that a fixed oscillator is obtained. For our discussion, we will use a very simple dynamic model for every cell: i.e. every ith cell has a falling edge delay, $\tau_{df,i}$ and a rising edge delay $\tau_{dr,i}$. Then the oscillation period can be written as:

$$T = \sum_{i=1}^{N} (\tau_{df,i} + \tau_{dr,i}) \tag{1}$$

In most practical designs, the unit cells are nominally matched such that the cell delays, $\tau_{df,i}$ and $\tau_{dr,i}$ will be (nearly) equal to their nominal values τ_{df} and τ_{dr}. Now we introduce the average nominal cell delay τ_d:

$$\tau_d = \frac{\tau_{df} + \tau_{dr}}{2} \tag{2}$$

From this we can obtain the associated VCO oscillation frequency $f_{\text{VCO}} = 1/T$. However, from the viewpoint of VCO A/D conversion, a more relevant parameter is the *effective* VCO frequency $f_{\text{eff}} = 2N \cdot f_{\text{VCO}}$. This can be understood by realizing that most contemporary VCO ADCs use multi-phase readouts (as shown in Fig. 1) [29]–[32]. This implies that each transition (rising- and falling edges) in the ring is detected, and these transitions occur at a rate $f_{\text{eff}} = 2N \cdot f_{\text{VCO}}$. Consequently, the VCO ADC quantization noise performance depends only on this effective VCO frequency [31], [32] and not on the actual VCO frequency. With this in mind, we will base the rest of our discussion on f_{eff}:

$$f_{\text{eff}} = \frac{2N}{2N\tau_d} = \frac{1}{\tau_d} \tag{3}$$

Here, f_{eff} is a function of the input signal (through the tune circuit). A crucial observation is that f_{eff} is independent of N, which means that the same SQNR is obtained regardless of the choice of the number N of VCO unit cells [31]. Additionally, the VCO's power consumption (see Section II-D) as well as its input referred white noise (see Section IV) are independent of N. This implies that, on the system level, N is to a large extent an independent design variable.

This important observation should be taken into account with some caution. While N does not affect the core analog performance of the VCO, in an actual VCO ADC the choice of N will substantially affect the performance of the digital readout circuitry (area, power, maximum operating frequency) [1], [33]. In particular, when decreasing N, the actual VCO frequency f_{VCO} increases, which requires the readout circuit to operate at a higher frequency and also to have a higher resolution, which might be unfeasible. Although these aspects are very important in an actual VCO ADC design, they are out of the scope of this study. Remark that some secondary

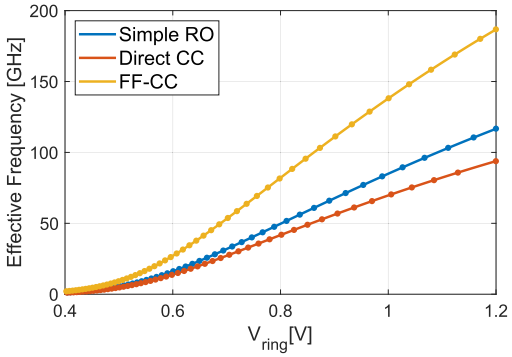

Fig. 4. f_{eff} vs. V_{ring} plots.

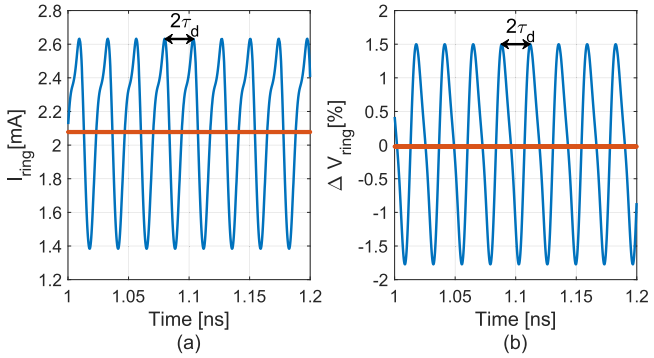

Fig. 5. VCO ripple waveforms for the simple ring oscillator circuit of Fig. 1 for the case of $V_{\text{ring}} = 1$ V: (a) current ripple for voltage control and (b) voltage ripple for current control. The red lines represent the DC component.

analog performance metrics such as e.g. $1/f$ noise also still depend on N.

As mentioned before, to control the oscillation frequency based on the input voltage, some kind of tune circuit is needed. In nearly all cases, this tune circuit is inserted at one of the supply lines of the ring oscillator, either V_{dd} or V_{ss}. Fig. 1 shows a variant where the tune circuit is inserted at the V_{ss} side (so-called *bottom* drive). The tune circuit can take many forms [2]. Some simple, but popular variants are a transconductor (current control), e.g. [3], a voltage buffer (voltage control) [34] or more advanced resistive drive circuits [13], [14]. The goal of the tune circuit is to control the current I_{ring} in the ring or the voltage V_{tune} on the ring. For the operation of the ring oscillator, the actual ring voltage V_{ring} is more relevant than the tune voltage V_{tune}. In the case of bottom drive, we can write:

$$V_{\text{ring}} = V_{dd} - V_{\text{tune}}, \tag{4}$$

and we will use this quantity in what follows. Then the overall VCO tune curve, i.e. effective VCO frequency vs. overall VCO input signal V_{in} (see Fig. 1) can be obtained:

$$f_{\text{eff}}(V_{\text{ring}}(V_{in}))$$

To illustrate this tune curve, we performed simulations in a standard 65 nm CMOS technology. The core inverter used in the delay cell had the following drawn[1] sizing:

$$W_n = 8\ \mu m, \quad W_p = 2 \cdot W_n, \quad L_n = L_p = 60\ nm. \tag{5}$$

A capacitive loading of 8 fF is added to each stage to model a realistic capacitive load due to the phase readout. A simulation result for our three ring oscillators is shown in Fig. 4. Here, it was verified that the curves for different values of N are identical (for $N = 9$, 17, 33, 65 and 129). Note that the same conclusions are valid when the tune circuit is inserted at the V_{dd} side (so-called *top* drive).

Fig. 4 confirms the notoriously non-linear behavior of the ring oscillator, which gets worse when moving closer to the sub-threshold region (where V_{ring} is close to the transistor threshold voltage). The plots in Fig. 4 also showcase the substantial difference between the different delay cells presented here. In terms of quantization noise performance, the highest effective oscillation frequency corresponds to the best case [31], [32]. Clearly, the case of the differential delay cell with feed-forward cross-coupling consistently performs the best, while the circuit with the differential delay cell with direct cross-coupling is the worst.

[1]The actual design is scaled to a gate length of 65 nm.

D. I-V Characteristic

We will now consider the raw electrical behavior of the core ring oscillator. More specifically, we will study the ring's current vs. voltage relationship (I-V characteristic) corresponding to our three delay cells. Before this study however, we must first consider something else. In practice, due to the non-ideal output impedance of the tune circuit, even for a constant input signal V_{in}, there will be a ripple on both the ring voltage as well as the current:

$$V_{\text{ring}}(t) = V_{\text{ring}}(V_{in}) + v_{ripple}(t) \tag{6}$$

$$i_{ring}(t) = I_{\text{ring}}(V_{in}) + i_{ripple}(t) \tag{7}$$

This is illustrated through simulations using the sizing of Eq. (5). The resulting waveforms for the simple oscillator of Fig. 1 are shown in Fig. 5. The two most extreme cases are considered: voltage control in Fig. 5(a) where the voltage ripple is zero and there is only a current ripple, and the reciprocal situation of ideal current control in Fig. 5(b). For the latter case, the current was chosen such that the corresponding DC component of the ring voltage is the same as for the voltage control case (i.e. 1 V). The ripple in both cases has a period of $2\tau_d$ and hence occurs at half the effective VCO frequency $\frac{f_{\text{eff}}}{2}$, see Eq. (3). Fortunately, in a well-designed VCO ADC application this ripple will be very far out of band, as the fundamental encoding error should be minimized [31]. An important observation here is that the current ripple looks exactly the same for different values of N, which we have confirmed through extensive simulations (for $N = 9$, 17, 33, 65 and 129), and by overlaying the ripple plots for these values of N in Fig. 5(a). In contrast, the voltage ripple in the case of an ideal current control configuration is inversely proportional to N. This is due to the fact that the ripple is filtered by the input capacitance, which is roughly equivalent to N times the gate-source capacitance of the device at the tune terminal.

Fig. 6 shows the ripple waveforms for the differential delay elements. Here again, each of the main inverters is sized

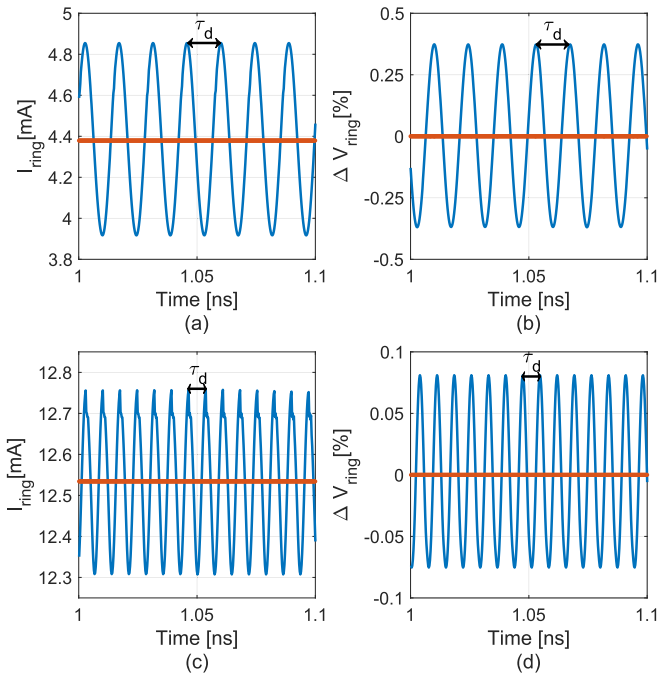

Fig. 6. VCO instantaneous ripple waveforms for ring VCOs based on differential delay elements for the case of $V_{\text{ring}} = 1$ V. Top row: the case of Direct CC of Fig. 2 with (a) the current ripple for voltage control and (b) the voltage ripple for current control. Bottom row: the case of FF-CC of Fig. 3 with (c) the current ripple for voltage control and (d) the voltage ripple for current control. The red lines represent the PSS solution for the value at DC.

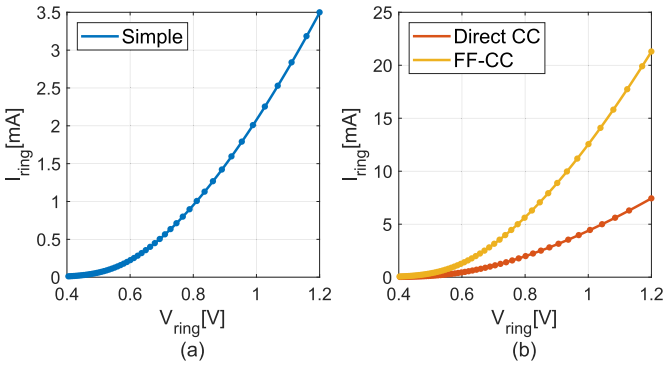

Fig. 7. I_{ring} vs. V_{ring} plot. The continuous curves are obtained with voltage control, the point markers with current control. Left: the simple ring VCO, right: the differential VCOs.

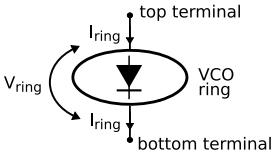

Fig. 8. Interpretation of the ring's I-V characteristic as a diode.

according to Eq. (5). The plots show that for these differential delay cells, the ripples are even smaller. Another important observation is that the ripple frequency is not at half the effective VCO frequency $\frac{f_{\text{eff}}}{2}$, but instead at f_{eff}. This means that this ripple will be even further out of band as in the case of the simple oscillator. The underlying mechanism causing this effect, will be explained below.

Note that in the simulation, the main inverters are sized according to Eq. (5) for each circuit, but that the corresponding current levels are very different. As could already be seen in Fig. 4, we can see that the VCO with feed-forward cross-coupling oscillates (Fig. 6(c)-(d)) much faster (roughly two times) than the one with direct cross-coupling (Fig. 6(a)-(b)). This will be further explained in the next section.

In what follows, we will assume that for all considered circuits, the ripple is at sufficiently high frequency that it can be ignored for the rest of the discussion and from now on we will focus on V_{ring} and I_{ring}. Now it is important to realize that within this approximation (i.e. that the voltage and the current ripple is negligible) V_{ring} and I_{ring} should mutually define each other. This implies that the V_{ring} vs. I_{ring} characteristics should be the same regardless whether they are obtained through voltage or current control. To confirm the validity of this approximation, the simulated V_{ring} vs. I_{ring} characteristic for our three ring oscillators (same sizing as Eq. (5)) is shown in Fig. 7 for both voltage (bold curves) as well as current (point markers) control (obtained through PSS simulations). We have also added point markers to Fig. 4 to indicate the result for a current control configuration. The curves are not strictly identical, but it is clear from the plot that even for the simple VCO (with the largest ripples), the difference is visually not discernible. Intuitively, this can be understood given that for a certain current in the ring, the voltage over the ring will settle toward the corresponding ring voltage needed to drain this current [13]. Again it was confirmed through simulations that for $N = 9$, 17, 33, 65 and 129, the plots are identical, which implies that the VCO power consumption is independent of N. Additionally, we observed that the I-V characteristics were independent of the (external) capacitive load on each VCO node. This implies that the power consumption is independent of this external load capacitance, and will also have other consequences later on.

Because the current control curves are practically identical to the voltage control curves in Fig. 7, the ring oscillator tune curve can be studied either in voltage mode (i.e. study the oscillation frequency as a function of V_{ring}) or in current mode (i.e. study the oscillation frequency as a function of I_{ring}). This is because both tune curves can be converted to each other through the oscillator's V_{ring} vs. I_{ring} characteristic. We will start our analysis with a voltage mode analysis, and adapt it for the current mode case later on.

When observing the ring I-V characteristics in Fig. 7, the similarity with a FET diode with a threshold voltage V_T of around 400 mV is striking. This diode interpretation is shown in Fig. 8 and allows for a strong intuition and simplified reasoning on the ring as an equivalent 2-terminal element, in particular in terms of voltage headroom and power consumption. We reiterate here that this diode-like characteristic is independent of the number of delay cells N in the ring and of the capacitive load on the VCO nodes.

III. VCO Modeling: Unit Cell Delay

To fully grasp the differences between the VCO unit cells, we will now analyze their respective delays on the circuit level.

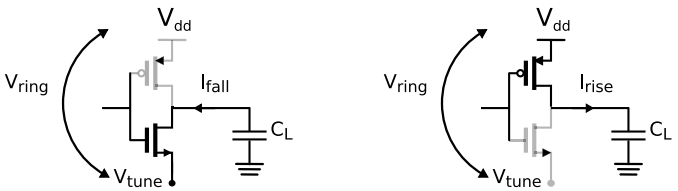

Fig. 9. Switching in a single cell of a simple ring oscillator VCO: (left) falling edge, (right) rising edge.

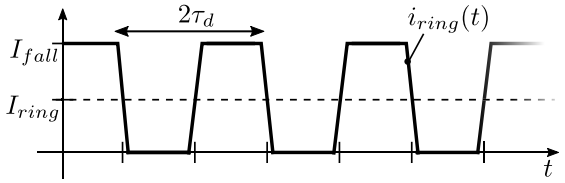

Fig. 10. Simplified sketch of the current ripple waveform $i_{\text{ring}}(t)$ corresponding to our circuit model of Fig. 9 which should be compared to the actual ripple waveform of Fig. 5(a).

A. Single-Ended Delay Cell

The goal of our analysis is to explore trends to guide design decisions. For this reason, we will use the simplest possible delay model, as was also done in other work [21]. For the single inverter unit cell, the dynamics of the threshold crossings are illustrated in Fig. 9. The falling delay τ_{df} can be described by the following expression:

$$\int_0^{\tau_{df}} \frac{I_{\text{fall}}}{C_L} = V_M \tag{8}$$

Here, τ_{df} is the time needed to toggle the next inverter and I_{fall} is the discharge current. V_M is the voltage difference between the stable state of the inverter and the toggle point of the inverter, which can be approximated as $\frac{V_{\text{ring}}}{2}$ for simplicity. Finally, C_L is the load capacitance seen by the cell and consists of the cell's output capacitance, the input capacitance of the next cell, the input capacitance of the readout buffer and finally the interconnect capacitance. If we make the (very rough) approximation that the current I_{fall} is constant during the entire switching process (remember, we go for simplicity rather than full accuracy), we obtain the fall time as:

$$\tau_{df} = \frac{V_{\text{ring}} \cdot C_L}{2 \cdot I_{\text{fall}}} \tag{9}$$

Furthermore, we will make the approximation that the MOS transistor in the inverter is in its pentode region. This is justified by the observation that at the start of the switching effect the drain source voltage of the transistor is relatively large. Hence, the current can be described by:

$$I_{\text{fall}} = \alpha_n \cdot g(V_{GS} - V_{Tn}) \quad \text{with} \quad \alpha_n = \frac{W_n}{L_n} \tag{10}$$

Here α_n stands for the ratio-metric factor and $g(\cdot)$ is a function which in weak inversion is exponential, in normal strong inversion quadratic and in velocity saturation linear.

Assuming that the devices switch abruptly, and taking the considerations above into account, the ring current $i_{\text{ring}}(t)$ in a bottom drive configuration can be modeled as displayed in Fig. 10. Here, we can observe the ripple, which has a peak-to-peak magnitude of I_{fall}, and the (quasi)-static component I_{ring} of the ring current, which is approximately equal to $I_{\text{fall}}/2$. This explains why we expect the ring's I-V characteristic of Fig. 7 to have the same shape as an NMOS diode characteristic (shown in the Appendix, Fig. 24). Comparing the ripple sketch to the simulated ripple waveform of Fig. 5(a), it is clear that the actual ripple is much smaller, affirming that our model is only an approximation. Despite this limitation, the period of the ripple is correctly predicted.

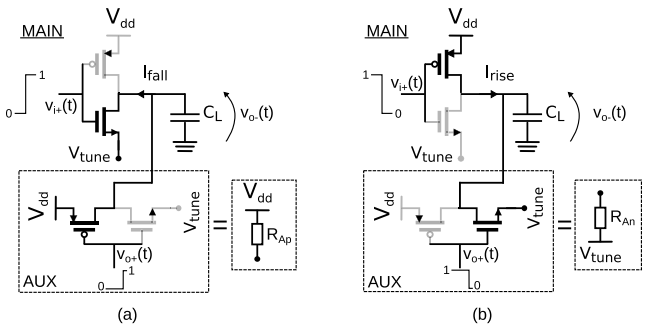

Fig. 11. Half-cell of the direct cross-coupled delay cell used in Fig 2: (a) simplified model for the falling transition and (b) simplified model for the rising transition.

B. Differential Delay Cell With Direct Cross-Coupling

To simplify the analysis for this differential circuit, we will assume that the auxiliary inverters in this delay cell ensure that the edges of the differential VCO are perfectly aligned (as intended). Consequently, this delay cell can be analyzed by studying a half-cell. To obtain the falling edge delay τ_{df+}, we will study the positive half cell shown in Fig. 11(a).

Here the cell's input waveform is simplified into an ideal square wave (with a zero rise time). This immediately switches the PMOS transistor in the main inverter off, while the NMOS transistor is switched on. Again we assume a constant current I_{fall} in the NMOS transistor biased in the pentode region. This current will start the discharge process of the load capacitor C_L. During this switching process, the gate of the auxiliary inverter is not yet switched and hence the auxiliary PMOS transistor will still be on. At the beginning of the switching process, the drain source voltage on this transistor is very small and hence this transistor will be in the triode region, such that it can be modeled by its on-resistance R_{Ap}. Considering the falling edge of the positive half cell at the output $v_{o-}(t)$, the switching process boils down to the following set of equations:

$$I_{\text{fall}} = \frac{V_{dd} - v_{o-}(t)}{R_{Ap}} - C_L \frac{dv_{o-}(t)}{dt}$$

$$\text{with} \quad \begin{cases} v_{o-}(0) = V_{dd} \\ v_{o-}(\tau_{df+}) = V_M \end{cases}$$

$$\iff \tau_{df+} = R_{Ap} C_L \cdot \ln\left(\frac{1}{1 - \frac{V_M}{I_{\text{fall}} \cdot R_{Ap}}}\right) \tag{11}$$

which can be further simplified by making the assumption:

$$\tau_{df+} \ll R_{Ap} C_L. \tag{12}$$

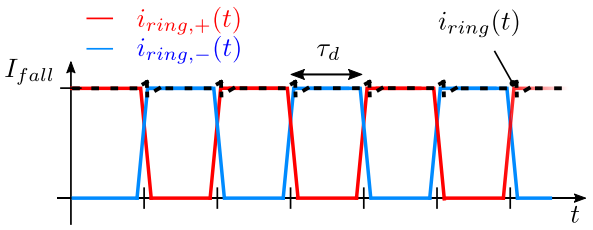

Fig. 12. Simplified sketch of the current ripple waveform $i_{\text{ring}}(t)$ of the differential delay cell with direct cross-coupling corresponding to our circuit model of Fig. 11.

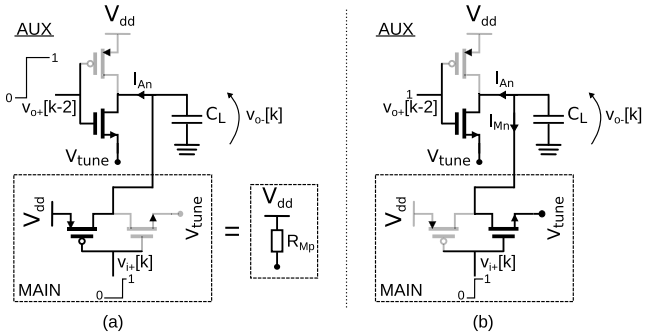

Fig. 13. Equivalent half-cell of the feed-forward coupled differential delay cell illustrating the falling edge switching mechanism. (a) Pre-discharge phase which forms the start of the actual edge. (b) Main discharging phase.

This is equivalent to stating that the auxiliary inverters should be sufficiently smaller ('weaker') than the main inverters, which is justified by the study in [14], where it is shown that increasing the size of the auxiliary inverters w.r.t. the main inverters comes at the cost of a worse performance in noise, power and frequency. As a consequence, the only sensible sizing of these auxiliary inverters is to make them relatively small w.r.t. the main inverters, which implies that in a good design Eq. (12) is always valid. Now we can make a first-order Taylor expression leading to a familiar expression for the positive half cell falling edge delay:

$$\tau_{df+} = \frac{V_{\text{ring}} \cdot C_L}{2 \cdot I_{\text{fall}}} \tag{13}$$

The half cell's rising edge delay τ_{dr+} can be analyzed based on the model in Fig. 11(b) and leads to an equivalent result:

$$\tau_{dr+} = \frac{V_{\text{ring}} \cdot C_L}{2 \cdot I_{rise}} \tag{14}$$

where I_{rise} is the current in the main PMOS transistor. Due to symmetry reasons, the same analysis is valid for the negative half cell, leading to similar expressions for τ_{df-} and τ_{dr-}. We note here that, even though the delays of the direct cross-coupled cell Eqs. (13, 14) look identical to the expression of the delay of the simple delay cell in Eq. (9), the oscillation frequencies in practice will not be identical because of the approximation of Eq. (12) and the load capacitances C_L are different for both circuits. We can now use these results for the half cells to approximate the overall falling edge delay τ_{df} and rising edge delay τ_{dr} of the differential delay cell:

$$\tau_{df} = \frac{\tau_{df+} + \tau_{dr-}}{2} \tag{15}$$

$$\tau_{dr} = = \frac{\tau_{dr+} + \tau_{df-}}{2} \tag{16}$$

In Section II-D, it was observed that the ripple on the ring current for the differential cells was smaller, and in addition, appeared at a frequency equal to f_{eff} instead of $\frac{f_{\text{eff}}}{2}$. Based on the analysis above, we sketched the waveform of the ring current corresponding to our model in Fig. 12 (assuming bottom drive). In contrast to the single-ended VCO delay cell, we now have two alternating contributions: the current pulled from the positive half cell $i_{\text{ring},+}(t)$ and from the negative half cell $i_{\text{ring},-}(t)$, which lags half period with respect to the positive half cell. As a result, the actual ring current is expected to be relatively flat, with a small residual ripple due to non-ideal switching, which is in qualitative agreement with the actual ripple waveform of Fig. 6(a). Also, the fact that the ripple frequency has shifted to f_{eff} is explained by Fig. 12.

C. Differential Delay Cell With Feed-Forward Cross-Coupling

To analyze this circuit, as in the previous subsection, we start with an equivalent half circuit (Fig. 13). To simplify the discussion, the auxiliary inverter is now placed at the top, and the main inverter at the bottom (in contrast to Fig. 11 where it is the other way). An important difference with the previous delay cells, is that now two phases must be distinguished: a pre-(dis)charging phase and the main (dis)charging phase. Another important difference is that for the kth cell now cell $k-2$ is also involved, since it drives the auxiliary inverter. To distinguish between these voltages we add the cell number as $[k]$ in the expression for the voltage. For example, $v_{o-}[k]$ refers to the negative terminal output voltage of the kth cell. The pre-discharging phase is detailed in Fig. 13(a). It occurs when the rising edge arrives at the $(k-2)$th cell, but has not yet reached the actual kth cell (on which we are focusing now). By looking at the figure we see that the behavior is almost identical to the discharging phase with the direct cross-coupled delay cell of Fig. 11. The only difference here is that the role of the main and the auxiliary inverter are interchanged in this case: now, the auxiliary NMOS is switched on due to a rising edge in $v_{o+}[k-2]$. When this occurs, the PMOS in the main inverter is still on, as the rising edge has not yet reached the input of the kth cell. As such, an identical situation as in the previous section is obtained, where now the main inverter acts as a triode resistor R_{Mp}, slowing down this pre-discharge process. The pre-discharging phase finishes when the edge has further rippled through the $(k-1)$th cell and hence reaches the input of the kth cell. This happens a delay τ_{dr+} after the begin of the pre-discharging phase. Then the main discharge phase begins, displayed in Fig. 13(b). If we set $t = 0$ at the start of the main discharge phase, this leads to:

$$\begin{aligned} -\tau_{dr+} \le t \le 0: \quad & \text{Pre-discharge phase} \\ v_{o-}[k](t) = V_{dd} - I_{An} \cdot R_{Mp} \cdot & \left(1 - e^{-\frac{t+\tau_{dr+}}{R_{Mp} C_L}}\right) \\ \text{with:} \quad & v_{o-}[k](-\tau_{dr+}) = V_{dd} \end{aligned} \tag{17}$$

In the main discharge phase, both the auxiliary and the main inverter current discharge the load capacitor. The resulting behavior is almost identical to the simple ring oscillator, only now *two* current contributions (one from the auxiliary and one from the main inverter) are integrated on the load capacitance:

$$0 < t \leq \tau_{df+}: \quad \text{Main discharge phase}$$
$$v_{o-}[k](t) = v_{o-}[k](0) - \int_0^t \frac{I_{Mn} + I_{An}}{C_L} dt$$
$$\text{with: } v_{o-}[k](\tau_{df+}) = V_M \tag{18}$$

To find the circuit's (rising and falling) delays the system of equations (17)-(18) must be solved. To obtain a simple expression for the result we will make the greatly simplifying approximation to neglect the output voltage variation during the pre-discharge. While this approximation is not *very* accurate, our simulation results later on will confirm that the resulting expression is still accurate enough for a correct interpretation of the main circuit properties. Now, based on the analysis of the previous delay cells, we get:

$$\tau_{df+} = \frac{V_{\text{ring}} \cdot C_L}{2 \cdot (I_{Mn} + I_{An})} \tag{19}$$

Similar expressions can be set up for the rising edge delay τ_{dr+} as well as for the negative half cell delays τ_{df-} and τ_{dr-}. Note that this expression again looks similar to that of the delay of the simple- and direct cross-coupled delay cell in Eqs. (9, 13, 14), but care should be taken in their comparison since the load capacitance is different for all three cases.

Finally, just as for the direct cross-coupling case, the balancing mechanism between both pseudo-differential paths, creates an averaging mechanism between the negative half-cell delays τ_{df-}, τ_{dr-} on the one hand and the positive half-cell delays τ_{df+}, τ_{dr+} on the other hand. Consequently, the overall falling edge delay τ_{df} and the overall rising edge delay τ_{dr} are obtained by the averaging Eqs. (15, 16) as well, but this time substituting Eq. (19) and the equivalent expressions for τ_{dr+} and the negative half cell delays.

IV. White Noise in VCO Delay Cells

As mentioned in the introduction, numerous publications already exist on the subject of noise in simple ring oscillators [21]–[24], providing the foundation for our work. We will expand these previous results to the differential circuits and translate them to the context of VCO ADCs by referring the phase noise expressions to the VCO input terminals. We will begin with an analysis for voltage control: *VC*.

A. Single-Ended Delay Cell

With the definition for the period T from Eq. (1), we can write the variance of the period jitter as:

$$\sigma_T^2 = N \cdot (\sigma_{\tau_{df}}^2 + \sigma_{\tau_{dr}}^2) \tag{20}$$

The VCO's output signal single-sideband phase noise spectral density $S_{\phi_{out},\text{VC}}$ for voltage control can then be calculated (see Eq. (15) and Eq. (17) in [21]), using τ_{df} from Eq. (9):

$$S_{\phi_{out},\text{VC}}(f) = \frac{4kT}{I}\left(\frac{g_m}{2I}(\gamma_N + \gamma_P) + \frac{1}{V_{\text{ring}}}\right)\left(\frac{f_0}{f}\right)^2 \tag{21}$$

Here it is assumed that the NMOS current I_{fall} is equal to the PMOS I_{rise} and represented by the symbol $I = I_{\text{fall}} = I_{\text{rise}}$. Remember that within our simple model (Fig. 10) it is also assumed that $I = 2 \cdot I_{ring}$. The NMOS and PMOS pentode transconductances, $g_{m,N}$ and $g_{m,P}$ are, for simplicity, set equal to $g_m = g_{m,N} = g_{m,P}$. The parameters γ_N and γ_P are the NMOS and the PMOS channel noise parameters. Traditionally, the value of γ is assumed to be equal to $\gamma = \frac{2}{3}$ or $\gamma = \frac{1}{2}$ when the transistor is biased in strong inversion or weak inversion respectively [35]. However, in reality the value of γ is also a function of the technology [36]. For instance, shorter channels typically result in significantly higher channel noise factors. Now, this phase noise expression can be input referred using the VCO voltage-sensitivity (or VCO gain) K_V:

$$S_{w,in,\text{VC}}(f) = S_{\phi_{out}}(f)\left(\frac{f}{K_V}\right)^2 = \frac{4kT}{I}\left(\frac{g_m}{2I}(\gamma_N + \gamma_P) + \frac{1}{V_{\text{ring}}}\right)\left(\frac{f_0}{K_V}\right)^2 \tag{22}$$

Based on the expressions for the cell delays in the previous section and Eq. (1), we can derive an expression for K_V:

$$K_V = \frac{df_0}{dV_{\text{ctrl}}} = -\frac{df_0}{dV_{\text{ring}}} = f_0 \cdot \left[\frac{1}{V_{\text{ring}}} - \frac{dI}{dV_{\text{ring}}} \cdot \frac{1}{I}\right] \tag{23}$$

As the gate-source voltage of the inverter transistors is equal to V_{ring}, we can write $g_m = \frac{dI}{dV_{\text{ring}}}$. Substituting this in the expression for the input referred phase noise gives:

$$S_{w,in,\text{VC}}(f) = \frac{4kT}{I}\frac{\frac{g_m}{2I}(\gamma_N + \gamma_P) + \frac{1}{V_{\text{ring}}}}{\left(\frac{g_m}{I} - \frac{1}{V_{\text{ring}}}\right)^2} \tag{24}$$

Note that $S_{w,in,\text{VC}}(f)$ is not dependent on f and hence corresponds to input referred white noise. In addition, the expression only depends on the transistor biasing and parameters (I, g_m, γ, V_{ring}). This has two important consequences: first, the noise is independent of the load capacitance of the delay cell (which will be confirmed by the simulations below). Consequently, the designer has the freedom to add explicit capacitance, e.g. in the form of buffer circuits, or to work with non-minimal channel lengths (e.g. to improve the $1/f$ behavior see below), since this can be done without a thermal noise penalty. However, there is a penalty in the quantization noise of the overall VCO ADC, as $f_{\text{eff}} \sim \frac{1}{C_L}$ directly impacts the quantization noise of the system, and hence increasing the inverter's load capacitance can only be done if the system is not limited by quantization noise. A second consequence is that the input referred white noise is not affected by the number of delay cells, N. This result was already known for the output phase noise [21], [24] and is also valid for the input referred noise.

B. Differential Delay Cell With Direct Cross-Coupling

For the noise calculation of the direct cross-coupled VCO delay cell from Fig. 2, we can again ignore the effect of the auxiliary inverter, as was done in Section III-B. Consequently, the noise calculations will be similar as for the

single-ended delay cell. Starting from Eq. (20) and taking into account the balancing effect due to the differential nature, see Eqs. (15, 16), a similar noise calculation can be done for the direct cross-coupled VCO delay cell:

$$S_{w,in,\mathrm{VC}}(f) = \frac{4kT}{2I}\frac{\frac{g_m}{2I}(\gamma_N+\gamma_P)+\frac{1}{V_{\mathrm{ring}}}}{\left(\frac{g_m}{I}-\frac{1}{V_{\mathrm{ring}}}\right)^2} \tag{25}$$

This expression is identical to the noise behavior of the single-ended VCO delay cell, apart from the effect of the balancing mechanism, which improves the noise performance with a factor 2. It should be observed that the ring current is twice as large as in the previous case (see Fig. 12). Hence, intuitively it makes sense that the noise is indeed a factor 2 smaller.

C. Differential Delay Cell With Feed-Forward Cross-Coupling

If the pre-charging phase is neglected, as in Section III-C, the analysis of the feed-forward cross-coupled delay cell also becomes similar to the previous cases. The most important difference is that the charging current now comes from both the main inverter as well as the auxiliary inverter. This leads to an overall current that is twice as large, but unfortunately both inverters contribute to the noise. Taking this into account as well as the balancing effect, due to the differential nature of the delay cell, the input referred white noise is obtained as:

$$S_{w,in,\mathrm{VC}}(f) = \frac{4kT}{4I}\frac{\frac{g_m}{2I}(\gamma_N+\gamma_P)+\frac{1}{2V_{\mathrm{ring}}}}{\left(\frac{g_m}{I}-\frac{1}{V_{\mathrm{ring}}}\right)^2} \tag{26}$$

The expression is again very similar to the previous expressions. The total noise improvement is now even higher, boasting more than a factor 4 improvement w.r.t. the single-ended VCO delay cell. As in the previous case, the root cause of this improvement can intuitively be understood by observing that the current has further increased: there are now 4 main inverter current components (compared to 2 for the case of a direct coupling cell and only 1 for the simple cell).

Before moving on, we refer here to the simplified noise expressions described by Eqs. (38-40) in Appendix B. These equations show that, in approximation, the voltage noise spectral density of the ring oscillator is described by $\sim \frac{kT}{g_{\mathrm{ring}}}$, just like a diode, allowing for a very simplified and intuitive noise calculation.

D. White Noise Simulations

To assess the validity of our analyses, again extensive simulations were performed. In these simulations, again all main inverters were sized according to Eq. (5). In our first batch of simulations the case of $N = 9$ was investigated and a capacitive load of 8 fF (modeling the phase readout) was used. Then for every value of the ring voltage V_{ring} the input referred white noise is obtained from PNOISE simulations according to the approach described in [37]. This was repeated for each of our three unit cells. The results are summarized in Fig. 14.

Next to the simulation results, also theoretical predictions based on Eqs. (24)–(26) are added to the figure. For simplicity,

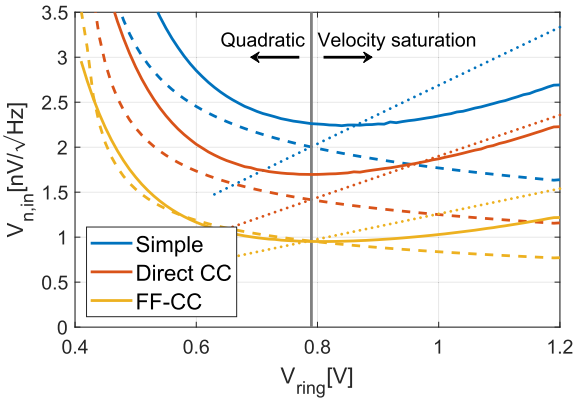

Fig. 14. Simulated input referred white noise (full lines), calculated using the quadratic formula (dashed lines) and calculated using the velocity saturation formula (dotted lines).

a fixed value of the noise factor $\gamma = \gamma_N = \gamma_P = 1.15$ was used here. This relatively large value is justified since we have short-channel devices [36], [38], [39]. First, a quadratic model for the device currents was used. As can be seen on Fig. 14, the resulting predictions match quite accurately for lower values of the ring voltage V_{ring}, but start to deviate significantly for higher values of V_{ring}. This behavior is expected as we are using short channel transistors and consequently for high overdrive voltages the transistors enter the velocity saturation region [36]. Hence, the results calculated with a velocity saturation model for the transistors are added as well and the model matches reasonably well for large values of V_{ring}. More details on the used device current equations are summarized in Appendix A. As mentioned before, Appendix B shows the simplified noise expressions, useful for quick estimates of the input referred noise.

In a second batch, all these simulations were repeated but now the load capacitance at every VCO node was increased by a factor 10 to 80 fF. As predicted by the theory, the results were found to be the same (within the accuracy of the simulator). We emphasize that this insight is only attainable when considering our input referred phase noise approach, as the effect of the VCO frequency f_0 is nullified by the VCO gain K_V in the input referred noise expression.

Finally, in a third batch, the simulations were repeated for increasing values of the number of VCO cells N, up to $N = 65$. Unfortunately, we were unable to do the simulations for higher values of N. The reason for this is the following: to obtain the phase noise we first need to do a PSS simulation followed by a PNOISE simulation [37]. However, the complexity (and simulation time) of a PSS simulation increases dramatically with an increasing number of delay cells. With a number of delay cells equal to $N = 65$, the simulations already took a very long time, and even failed to converge for some values of the ring voltage. For larger values of N (e.g. > 65), the simulator failed to converge over the entire range of V_{ring}. Nevertheless, we present our findings here. For relatively small values of the number of VCO cells up to $N = 33$, we found that the input referred white noise indeed was approximately independent of N. However, for the larger value of $N = 65$, a discrepancy was found: the input referred white noise was now about 2 dB better than expected. This

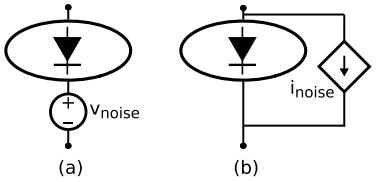

Fig. 15. Interpretation of the ring's I-V characteristic as a diode allowing to refer the ring's phase noise to its input terminal (a) as an equivalent voltage and (b) as an equivalent current.

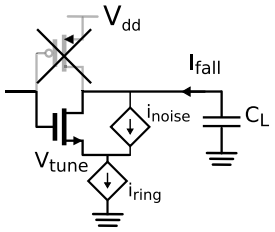

Fig. 16. Effect of NMOS noise during a falling edge.

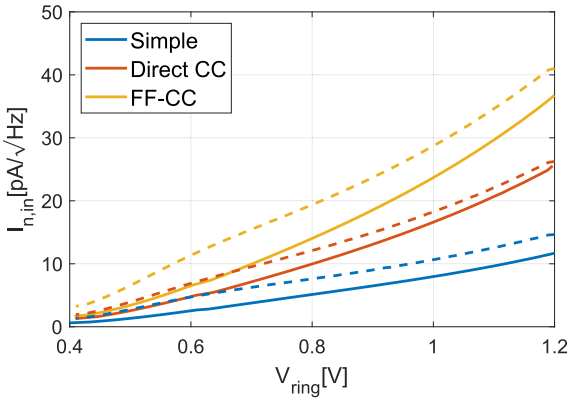

Fig. 17. Simulated input referred white noise for a current mode configuration (full lines), and calculated using Eqs. (32) (dashed lines).

effect was not observed in earlier work [21], [24] and it is not yet fully understood whether this is due to simulation artifacts or a genuine trend which is not explained by the theory.

E. Current Mode Noise

As mentioned in Section II-D, everything from that point, including the noise analysis above, is made with a voltage-mode approach. However, it is well known for conventional analog circuits that a different approach must be taken for optimizing current-mode circuits. Hence, the question how this translates to the different ring oscillators under scrutiny.

In Section II-D, it was already explained that a voltage-mode approach could be translated to a current-mode approach through the I-V characteristic of the ring (see Fig. 7). For the input referred noise sources, this is illustrated in Fig. 15, which indicates how the ring's internal noise sources can be modeled as equivalent input referred noise generators (either voltage v_{noise} or current i_{noise}). Regardless, whether the ring is driven in current or voltage control, the current and respectively voltage noise can be derived from each other through:

$$S_{w,in,I}(f) = S_{\phi_{out}}\left(\frac{f}{K_I}\right)^2 = \underbrace{S_{\phi_{out}}\left(\frac{f}{K_V}\right)^2}_{S_{w,in}(f)} \cdot g_{ring}^2 \tag{27}$$

Or simply put:

$$i_{\text{noise}} = g_{\text{ring}} v_{\text{noise}} \tag{28}$$

where the ring transconductance g_{ring} can be obtained by taking the derivative of the ring's I-V characteristic (Fig. 7). This allows to convert the input referred voltage noise into the input referred current noise.

The derivation above assumes that the phase noise at the VCO output is the same. However, we know from the discussion above that for fixed values of I_{ring} and V_{ring}, the ripple depends on the driving point impedance and thus differs between voltage and current control. Hence it could be that the phase noise is also different. Upon investigation, it turns out that this is indeed the case. To clarify this, we have to look back to the analysis of [21], where it is shown that the PMOS transistors contribute noise during the rising edge and the NMOS during the falling edge. Let us now focus on the falling edge in current control, shown in Fig. 16.

Here, we can see that if the ring is driven by an ideal current source the NMOS noise (represented by the source i_{noise}) cannot propagate to the output. Consequently the NMOS transistors do not contribute to the phase noise and only the PMOS noise is relevant. For the bottom drive configuration, as displayed in the figure, this boils down to omitting the γ_N representing the NMOS noise in Eqs. (29-31). Combining this with Eq. (28), for the case of a bottom drive configuration, we can then obtain the input referred current noise for the case of current control (*IC*) for the simple, direct CC and FF-CC ring oscillators respectively:

$$S_{w,in,I,\text{IC}}(f) = \frac{4kT}{I}\frac{\frac{g_m}{2I}\gamma_P + \frac{1}{2V_{\text{ring}}}}{\left(\frac{g_m}{I} - \frac{1}{V_{\text{ring}}}\right)^2} \cdot g_{\text{ring}}^2 \tag{29}$$

$$S_{w,in,I,\text{IC}}(f) = \frac{4kT}{2I}\frac{\frac{g_m}{2I}\gamma_P + \frac{1}{2V_{\text{ring}}}}{\left(\frac{g_m}{I} - \frac{1}{V_{\text{ring}}}\right)^2} \cdot g_{\text{ring}}^2 \tag{30}$$

$$S_{w,in,I,\text{IC}}(f) = \frac{4kT}{4I}\frac{\frac{g_m}{2I}\gamma_P + \frac{1}{4V_{\text{ring}}}}{\left(\frac{g_m}{I} - \frac{1}{V_{\text{ring}}}\right)^2} \cdot g_{\text{ring}}^2 \tag{31}$$

For the case of top drive, the reciprocal situation where only the NMOS transistors contribute to the noise, occurs. With our sizing the NMOS and the PMOS noise factors γ_N and γ_P are approximately equal. Taking this into account and by comparing the above results with Eqs. (24-26) we can generalize these results for arbitrary driving impedance as:

$$S_{w,in,I}(f) = S_{w,in,\text{VM}}(f) \cdot g_{\text{ring}}^2 \cdot \Gamma_Z, \tag{32}$$

where the driving impedance factor Γ_Z is around 0.5 for ideal current control and 1 for ideal voltage control. This equation (evaluated for $\Gamma_Z = 0.5$ and the previous results for $S_{w,in,\text{VC}}(f)$) is shown together with the simulated input referred current mode noise in Fig. 17.

V. Flicker Noise in VCO Delay Cells

Similarly as for the analysis of white noise, we can build on prior results on output phase noise and refer them to the input by using the expression of the VCO sensitivity, see Eq. (23). Through straightforward elaboration similar to the calculations above, we can translate Eqs. (15) and (45) in [21] toward input referred expressions for the flicker noise in VCO ADCs. For the case of the single ended delay cell, we obtain:

$$S_{1/f,in,\mathrm{VC}}(f)=\frac{1}{8NC_{\mathrm{ox}}}\frac{\left(\frac{g_m}{I}\right)^2\left(\frac{K_{fn}}{W_nL_n}+\frac{K_{fp}}{W_pL_p}\right)}{\left(\frac{g_m}{I}-\frac{1}{V_{\mathrm{ring}}}\right)^2}\cdot\frac{1}{f} \quad (33)$$

Here K_{fn} and K_{fp} represent the NMOS and the PMOS flicker noise constants and C_{ox} depicts the oxide capacitance. For the differential delay cell with direct coupling:

$$S_{1/f,in,\mathrm{VC}}(f)=\frac{1}{8NC_{\mathrm{ox}}}\frac{\left(\frac{g_m}{I}\right)^2\left(\frac{K_{fn}}{2\ W_nL_n}+\frac{K_{fp}}{2\ W_pL_p}\right)}{\left(\frac{g_m}{I}-\frac{1}{V_{\mathrm{ring}}}\right)^2}\cdot\frac{1}{f} \quad (34)$$

is obtained, which is a factor 2 smaller w.r.t. the previous case. Essentially, this is due to the fact that (ignoring the small auxiliary inverters) the number of inverters has doubled and hence the total gate area is a factor 2 larger. And finally for the differential delay cell with feed-forward coupling:

$$S_{1/f,in,\mathrm{VC}}(f)=\frac{1}{8NC_{\mathrm{ox}}}\frac{\left(\frac{g_m}{I}\right)^2\left(\frac{K_{fn}}{4\ W_nL_n}+\frac{K_{fp}}{4\ W_pL_p}\right)}{\left(\frac{g_m}{I}-\frac{1}{V_{\mathrm{ring}}}\right)^2}\cdot\frac{1}{f} \quad (35)$$

which again is another factor 2 smaller. This can be understood by considering that the total gate area has now further increased by another factor 2. If we examine these expressions, we see that, as expected, the $1/f$ noise improves with increasing gate area. This means that the flicker noise performance can be improved by using non-minimal length devices, which has been exploited in low frequency designs [3] where the reduced effective oscillation frequency is not an issue. Also, the flicker noise is inversely proportional with the number N of cells in the ring. This is a degree of freedom that in principle can be exploited without any penalty (ignoring the impact on the readout circuitry): i.e. all other relevant analog VCO ADC metrics (effective oscillation frequency, power, white noise) are independent of N.

To assess our analysis, similar simulations were performed as for the white noise case. The results for our reference case ($N = 9$ unit cells, main inverters sized according to Eq. (5) and 8 fF load per phase), are shown in Fig. 18. For simplicity, the flicker noise is represented as the noise density at 1 Hz. The predictions according to Eqs. (33)–(35) are superimposed. In this case only the case of the quadratic MOSFET model is shown. Here, $K_{fn} = K_{fp} = 3.2 \cdot 10^{-24}$ were used for the flicker noise constants, which is in agreement with [21], [36].

From Fig. 18 it is clear that the simulated noise significantly increases with increasing values of V_{ring}. Moreover, it is clear that the theoretical predictions do not follow this trend. Even when adding the velocity saturation MOSFET model (see Appendix A) for higher values of V_{ring} to the plot, this behavior could not be accurately explained. Upon

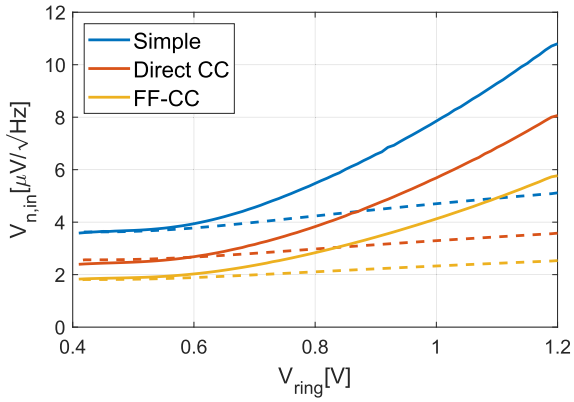

Fig. 18. Input referred flicker noise at 1 Hz: simulated (full lines) and calculated with quadratic model (dashed lines).

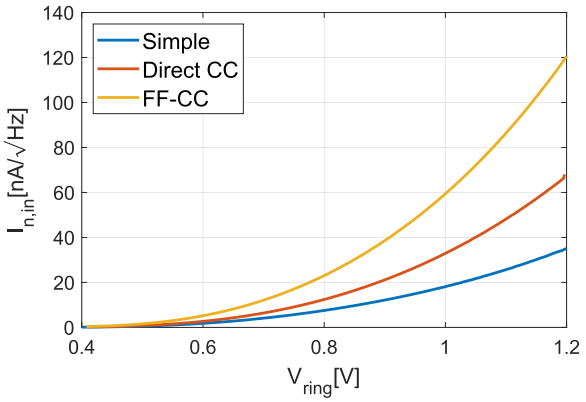

Fig. 19. Input referred current flicker noise simulated at 1 Hz.

investigation, we believe that the effect can be attributed to the strong bias-dependency of the flicker noise constant K_{fp} [36]: deep in strong inversion, increases by a factor of 2 are not uncommon for NMOS devices and for PMOS devices, increases by a factor as high as 50 have been reported [36].

Similar to the white noise simulation study, in subsequent batches, these simulations were repeated with a 10× increase of the load capacitance and for varying values of the number of cells N. Increasing the load capacitance, did not affect the flicker noise as predicted by the theory. Increasing the number N of cells lead to a $1/N$ decrease of the flicker noise, also in agreement with the theoretical predictions. Again, we emphasize here that this insight is only attainable when considering our input referred phase noise approach, as the effect of the VCO frequency f_0 is nullified by the VCO gain K_V in the input referred noise expression.

Finally, the current mode flicker noise was studied. In particular it was found that similarly as for the white noise, in bottom drive current control, the NMOS transistors do not contribute noise. Hence a similar expression as (32) with a driving impedance factor Γ_Z holds also for the flicker noise. The associate results for flicker noise simulations in a current control configuration are shown in Fig. 19.

VI. Power Efficiency

On the one hand, from the results compiled in Fig. 14 and Fig. 18, the differential delay cells seem to be the

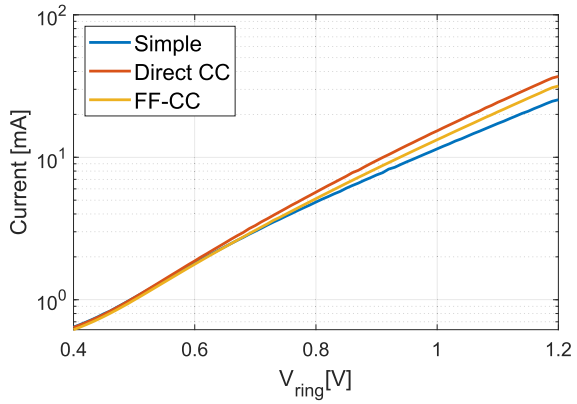

Fig. 20. Current needed for $1nV/\sqrt{Hz}$ of input referred white noise, using straight-forward impedance scaling.

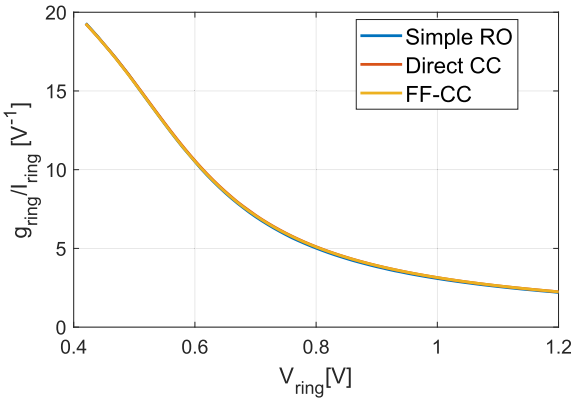

Fig. 21. $\frac{g_{ring}}{I_{ring}}$ vs. V_{ring} plot.

better option in terms of noise performance for voltage mode circuits. On the other hand, for current mode circuits, from Figs. 17 and 19, the simple delay cell seems to be the best option for current mode. In the presentation of the results above however, the common denominator is that every main inverter is sized identical. This does not take into account that the different cells have different numbers of inverters, which means that their area and even more important their current consumption, is very different (see e.g. Fig. 7). We will now take this into account for a more relevant comparison.

A. White Noise Power Efficiency

To make a fair comparison, the current consumption required to obtain an (arbitrarily chosen) input referred white noise level of $1nV/\sqrt{Hz}$ is displayed in Fig. 20. Here, the well known impedance scaling law is used that a 3dB noise voltage reduction can be obtained by increasing every transistor width as well as the current by a factor of 2. This way, every circuit can be appropriately sized for an arbitrary voltage noise level at the price of an increased current consumption, which is also reflected in the correct ADC Figure-of-Merit (FoM) [40]. This scaling law is used to obtain the plot of Fig. 20.

From the plot, two important conclusions can be drawn. First, for nearly all biasing levels of V_{ring}, the simple delay cell is the most efficient, while the conventional differential delay cell with direct cross-coupling is the worst. The improved differential delay cell with feed-forward cross-coupling is roughly in between. However, for small values of V_{ring} (starting from approximately 0.66 V) the difference between the three cells becomes negligible. In fact the differential cell with feed-forward is the best, but the difference is so small that this is almost invisible on the figure. The second conclusion is that only modest improvements with regard to the power efficiency can be obtained by choosing the right delay cell architecture. In contrast, appropriately selecting the biasing of V_{ring} has an enormous impact. E.g. reducing V_{ring} from 1 V to 800 mV almost halves the required power for a given white noise level. In general, in terms of power efficiency, the bias should be chosen to keep the ring voltage as low as possible.

There are a few practical limitations on reducing the voltage on the ring: the ring voltage should remain sufficiently high such that the oscillation (which has a peak to peak amplitude of V_{ring}) is large enough to drive the readout circuit. Additionally, at lower values of V_{ring} the VCO has an increased non-linearity, which should be dealt with. Fortunately there are plenty of techniques that can solve this [1], [2], [5], [13], [14], [19] or by employing a co-optimization, trading noise performance for linearity. Finally, a lower ring voltage results in a lower effective frequency, and thus a lower SQNR.

Without taking the SQNR into account, based on these considerations, it is beneficial to use an architecture where the signal swing around the biased ring voltage is limited, such that the bias level can be set near $V_{ring} = 0.4$ V where it is used in the most efficient way. This can be achieved by many architectures: e.g. two-stage [4], [5], feedback [6]–[12]) or even by simply using a straightforward open loop ADC without pre-amplifier such that the VCO is used with very small input signals [3], [20].

For a more intuitive understanding of the previous results, we can again use the simplified noise expressions of Eqs. (38-40), see Appendix B. Here we saw that the voltage noise spectral density was essentially $\sim kT/g_{\text{ring}}$. This implies that the optimal biasing of the ring can be found by considering $g_{\text{ring}}/I_{\text{ring}}$. This is plotted in Fig. 21 as a function of V_{ring} for the three different ring oscillators. The plot clearly confirms the previous result that the highest value of $g_{\text{ring}}/I_{\text{ring}}$ (and hence the optimal biasing) occurs for low bias levels of the ring. Moreover, the plot also shows that the differences between the three circuits are expected to be very small, which again is confirmed by the results of Fig. 20.

Let us now focus on the current mode configuration. From the simplified noise expressions of Eqs. (38-40) in Appendix B together with Eq. (28), we can derive that the current noise spectral density is essentially $\sim kTg_{\text{ring}}$. Hence, from Fig. 21, we expect that the most efficient biasing in current mode will be for a high value of V_{ring}.

To enable a fair comparison between the different delay cells, a typical current mode configuration is considered. Here the ring oscillator is driven by a transconductor where the transconductor bias current (in this case arbitrarily set to 1 mA) biases the ring, see Fig. 22. The corresponding input referred noise current plot is obtained by scaling Fig. 17, such that every point in the plot represents the same current level (in this case 1 mA). This implies that every point in the plot represents

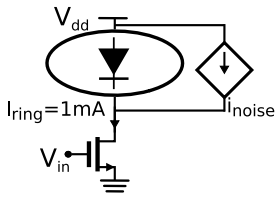

Fig. 22. Current mode operation where the ring is driven by a transconductor with a fixed bias current of 1 mA.

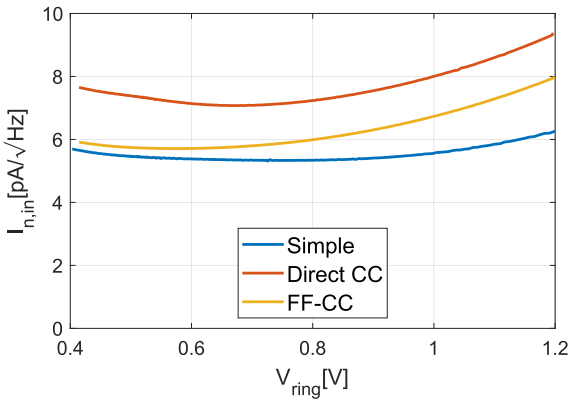

Fig. 23. Input referred white noise for a current control approach, for the case of fixed ring bias current I_{ring} of 1 mA.

a different sizing, corresponding to the desired bias value of the ring voltage V_{ring}. The corresponding noise is shown in Fig. 23 as a function of the ring biasing level V_{ring}. Here, we can see that for increasing values of V_{ring}, initially the noise decreases as expected. Hence, a larger value of the bias voltage V_{ring} is favored. But for increasingly larger values of the bias voltage V_{ring}, the noise performance deteriorates, which is contrary to the intuition from Fig. 21. Upon investigation, we found that this is mainly due to the fact that the ring enters velocity saturation, where the channel noise factor γ is worse [36]. Also, the omitted factors in the simplified expressions in the appendix worsen the noise at higher ring voltages (and even more in velocity saturation). The result of these combined effects is that current mode efficiency curve is relatively flat. Note that these effects also play in the voltage mode case, but here they all work in the same direction as the $g_{\text{ring}}/I_{\text{ring}}$ effect and hence make the curve even steeper.

B. Flicker Noise Power Efficiency

The bias dependency of the flicker noise in terms of efficiency is somewhat irrelevant, as the flicker noise can easily be designed to adhere to the specifications by increasing the number of cells, N, or by increasing the gate area at the cost of a lower effective oscillation frequency. We do remark here that the strong bias dependency of K_f could make a low bias level design attractive. Ultimately, if these techniques are not sufficient (e.g. in a low frequency design for sensor applications) chopping techniques can be used [41], [42].

VII. Conclusion and Takeaways

We believe that we have laid the foundation for a more intuitive understanding of ring oscillators to be used in VCO ADCs, which is valid for the most relevant pseudo-digital ring oscillator circuits. We advocate the following intuition:

- We can think of the electrical behavior of the VCO as a diode with the corresponding intuition on voltage headroom and power consumption.
- The simplified noise expressions (Appendix B) indicate that the voltage noise spectral density is $\sim kT/g_m\Gamma_Z$. Hence the diode interpretation is also applicable for the thermal noise, but here a driving impedance correction factor Γ_Z should be taken into account.
- The flicker noise is determined by the active area of the oscillator and can be improved either by increasing N, the number of unit elements, or the gate area used in a unit element, see Eqs. (42-44).
- Apart from flicker noise, the electrical ring properties essentially only depend on the unit cell's impedance level. In particular, they do not depend on the number of stages nor on the capacitive load of a delay cell.

The quantization noise performance is strongly affected by the effective oscillation frequency, f_{eff}:

- This f_{eff} is independent of N the number of stages.
- It is strongly dependent on the capacitive load of the stage and also on the biasing of the ring.
- Unlike most other VCO aspects, f_{eff} differs significantly for the 3 types of delay cells where the differential cell with feed-forward cross-coupling clearly performs best.

Finally, we want to remark that the actual system decision on the number of cells, the biasing of the ring and the sampling frequency should be made after an overall system level study where also the power consumption of the phase readout as well as the digital reconstruction logic is taken into account.

Appendix A
MOSFET Model

To evaluate the theoretical equations derived in Sections IV and V, a MOSFET model is needed. Particularly to relate these equations to a device sizing strategy. Unfortunately, the device equations to accurately describe the behavior of a MOSFET transistor [36] are cumbersome and not suitable for quick and simple calculations. To overcome this, some authors advocate the use of a table-based approach [43]. We went with a more pragmatic approach, based on the fact that we are operating very short channel transistors at a relatively high gate overdrive voltage. Hence, it makes sense to use a conventional strong inversion model (with a quadratic model) and a velocity saturation model (with a linear model). This leads to the following device equations for the current I_{quad} in the quadratic region and I_{vel} in the velocity saturation region:

$$\begin{aligned} I_{quad} &= \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{\text{ring}} - V_T\right)^2 \\ I_{vel} &= WC_{ox}v_{sat}(V_{\text{ring}} - V_T') \end{aligned} \tag{36}$$

As is common, here μ stands for the carrier mobility, C_{ox} for the oxide capacitance and v_{sat} for the saturation velocity.

As expected, the quadratic model is valid for smaller values of $V_{\text{ring,eff}} = V_{\text{ring}} - V_T$, while the velocity saturation model is valid for larger values of $V_{\text{ring,eff}}$. This is illustrated in Fig. 24, which shows the actual NMOS current for the sizing of Eq. (5),

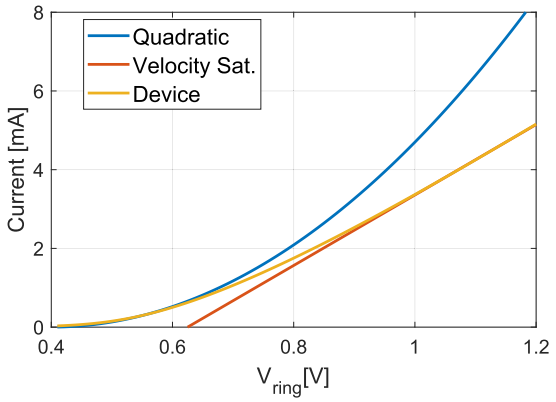

Fig. 24. I-V characteristic of an NMOS device with the corresponding quadratic and linear approximations.

as well as the approximations of Eq. (36), where the numerical values $C_{ox} = 14\ fF/\mu m^2$; $\mu = 0.014$ A/V^2 and $v_{sat} = 8 \cdot 10^4$ m/s were used. Note that a different V_T is used for the velocity saturation ($V_T = 0.4$ V, $V_T' = 0.625$ V), which was needed to obtain a good fit.

APPENDIX B
SIMPLIFIED NOISE EXPRESSIONS FOR DESIGNERS

To make quick estimations of the noise, simpler expressions than Eqs. (24)–(26), (29)–(31) and (33)–(35) are desired. We will first look at the white noise behavior.

1) White Noise: For this we start by rewriting $\frac{g_m}{I}$ based on the operating region:

$$\frac{g_m}{I} = \frac{\delta I}{\delta V_{\text{ring}}} \cdot \frac{1}{I} = \frac{\lambda}{(V_{\text{ring}} - V_T)} = \frac{\lambda}{V_{\text{ring,eff}}} \tag{37}$$

Here, $\lambda = 1$ in velocity saturation and $\lambda = 2$ in the quadratic region. From this expression we can immediately conclude that the following is always true: $\frac{g_m}{I} > \frac{1}{V_{\text{ring}}}$.

Now we can stretch this a bit and make the approximation that $\frac{g_m}{I} \gg \frac{1}{V_{\text{ring}}}$. Then the noise expressions can be simplified substantially. For the case of the simple delay cell, the direct cross-coupled and the feed-forward cross-coupled respectively we obtain:

$$S_{w,in}(f) = 4kT \cdot \frac{\gamma_N + \gamma_P}{2g_m} \cdot \Gamma_Z \tag{38}$$

$$S_{w,in}(f) = 2kT \cdot \frac{\gamma_N + \gamma_P}{2g_m} \cdot \Gamma_Z \tag{39}$$

$$S_{w,in}(f) = kT \cdot \frac{\gamma_N + \gamma_P}{2g_m} \cdot \Gamma_Z \tag{40}$$

This can be further combined with the expressions for g_m in the quadratic and velocity saturation region:

$$\begin{aligned} g_{m,quad} &= \mu C_{ox} \frac{W}{L}(V_{\text{ring}} - V_T) \\ g_{m,vel} &= W C_{ox} v_{sat} \end{aligned} \tag{41}$$

This leads to a $\left(\sim \frac{1}{V_{\text{ring}} - V_T}\right)$-noise behavior for the quadratic part of the MOS I-V characteristic, and a constant behavior for the linear part (velocity saturation).

To link this to the overall ring behavior, remark that, based on our simple models, this g_m corresponds to $2g_{ring}$ for the simple ring oscillator, g_{ring} for the differential ring oscillator with direct cross-coupling and to $\frac{g_{ring}}{2}$ for the differential ring oscillator with feed-forward cross-coupling. While these equations are very simple and useful for back-of-an-envelope calculations, we caution the reader that the result is an optimistic estimate of the actual noise level (around 50% of the actual effective noise value).

2) Flicker Noise: The same approach can be applied for the flicker noise. For the case of the simple delay cell, the direct cross-coupled and the feed-forward cross-coupled respectively we obtain for voltage control:

$$S_{1/f,in,\text{VC}}(f) = \frac{\frac{K_{fn}}{W_n L_n} + \frac{K_{fp}}{W_p L_p}}{8NC_{\text{ox}}} \cdot \frac{1}{f} \tag{42}$$

$$S_{1/f,in,\text{VC}}(f) = \frac{\frac{K_{fn}}{W_n L_n} + \frac{K_{fp}}{W_p L_p}}{16NC_{\text{ox}}} \cdot \frac{1}{f} \tag{43}$$

$$S_{1/f,in,\text{VC}}(f) = \frac{\frac{K_{fn}}{W_n L_n} + \frac{K_{fp}}{W_p L_p}}{32NC_{\text{ox}}} \cdot \frac{1}{f} \tag{44}$$

The results for current control are even simpler, because here only one transistor contributes to the noise (the PMOS for bottom drive and the NMOS for top drive), which means that one term can be removed in the above expression. For a more general driving impedance, the above equations require a driving impedance correction factor Γ_Z.

As already explained in Section V, care should be taken when using these equations due to the fact that the flicker noise "*constants*" K_{fn} and K_{fp} are not constant at all, but depend significantly on the biasing point of the transistor [36].

REFERENCES

[1] G. G. E. Gielen, L. Hernandez, and P. Rombouts, "Time-encoding analog-to-digital converters: Bridging the analog gap to advanced digital CMOS—Part 1: Basic principles," *IEEE Solid-State Circuits Mag.*, vol. 12, no. 2, pp. 47–55, Jun. 2020.

[2] G. G. E. Gielen, L. Hernandez, and P. Rombouts, "Time-encoding analog-to-digital converters: Bridging the analog gap to advanced digital CMOS—Part 2: Architectures and circuits," *IEEE Solid-State Circuits Mag.*, vol. 12, no. 3, pp. 18–27, Aug. 2020.

[3] A. Quintero *et al.*, "A coarse-fine VCO-ADC for MEMS microphones with sampling synchronization by data scrambling," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 29–32, 2020.

[4] K. Reddy *et al.*, "A 16-mW 78-dB SNDR 10-MHz BW CT delta sigma ADC using residue-cancelling VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2916–2927, Dec. 2012.

[5] X. Xing and G. G. E. Gielen, "A 42 fJ/step-FoM two-step VCO-based delta-sigma ADC in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 714–723, Mar. 2015.

[6] S. Li, A. Mukherjee, and N. Sun, "A 174.3-dB FoM VCO-based CT delta sigma modulator with a fully-digital phase extended quantizer and tri-level resistor DAC in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1940–1952, Jul. 2017.

[7] A. Jayaraj, M. Danesh, S. T. Chandrasekaran, and A. Sanyal, "Highly digital second-order $\Delta\Sigma$ VCO ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 7, pp. 2415–2425, Jul. 2019.

[8] M. Sadollahi and G. C. Temes, "A 10-MHz BW 77.9 dB SNDR DT MASH delta sigma ADC with NC-VCO-based quantizer and OPAMP sharing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 9, pp. 3384–3392, Sep. 2019.

[9] H. Maghami *et al.*, "A highly linear OTA-free VCO-based 1–1 MASH delta sigma ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 7, pp. 2440–2453, Jul. 2019.

[10] A. Jayaraj, M. Danesh, S. T. Chandrasekaran, and A. Sanyal, "76-dB DR, 48 fJ/step second-order VCO-based current-to-digital converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 4, pp. 1149–1157, Apr. 2020.

[11] H. Maghami *et al.*, "A highly linear OTA-less 1–1 MASH VCO-based $\Delta\Sigma$ ADC with an efficient phase quantization noise extraction technique," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 706–718, Mar. 2020.

[12] W. Zhao *et al.*, "A 0.025-mm^2 0.8-V 78.5-dB SNDR VCO-based sensor readout circuit in a hybrid PLL-$\Delta\Sigma$ M structure," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 666–679, Mar. 2020.

[13] A. Babaie-Fishani and P. Rombouts, "Highly linear VCO for use in VCO-ADCs," *Electron. Lett.*, vol. 52, no. 4, pp. 268–270, Feb. 2016.

[14] J. Borgmans and P. Rombouts, "Enhanced circuit for linear ring VCO-ADCs," *Electron. Lett.*, vol. 55, no. 10, pp. 583–585, May 2019.

[15] V. Nguyen, F. Schembari, and R. B. Staszewski, "A 0.2-V 30-MS/s 11b-ENOB open-loop VCO-based ADC in 28-nm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 9, pp. 190–193, Sep. 2018.

[16] G. Taylor and I. Galton, "A mostly-digital variable-rate continuous-time delta-sigma modulator ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2634–2646, Dec. 2010.

[17] G. Taylor and I. Galton, "A reconfigurable mostly-digital delta-sigma ADC with a worst-case FOM of 160 dB," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 983–995, Apr. 2013.

[18] S. Rao, K. Reddy, B. Young, and P. K. Hanumolu, "A deterministic digital background calibration technique for VCO-based ADCs," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 950–960, Apr. 2014.

[19] A. Babaie-Fishani and P. Rombouts, "A mostly digital VCO-based CT-SDM with third-order noise shaping," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2141–2153, Aug. 2017.

[20] W. Jiang, V. Hokhikyan, H. Chandrakumar, V. Karkare, and D. Markovic, "A +/−50-mV linear-input-range VCO-based neural-recording front-end with digital nonlinearity correction," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 173–184, Jan. 2017.

[21] A. A. Abidi, "Phase noise and jitter in CMOS ring oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1803–1816, Aug. 2006.

[22] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.

[23] A. Homayoun and B. Razavi, "Relation between delay line phase noise and ring oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 384–391, Nov. 2013.

[24] F. Pepe and P. Andreani, "An accurate analysis of phase noise in CMOS ring oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 8, pp. 1292–1296, Aug. 2019.

[25] B. Razavi, "The ring oscillator [a circuit for all seasons]," *IEEE Solid State-Circuits Mag.*, vol. 11, no. 4, pp. 10–81, Nov. 2019.

[26] K. M. Al-Tamimi, K. El-Sankary, and Y. Fouzar, "VCO-based ADC with built-in supply noise immunity using injection-locked ring oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 7, pp. 1089–1093, Jul. 2019.

[27] M. Baert and W. Dehaene, "A 5-GS/s 7.2-ENOB time-interleaved VCO-based ADC achieving 30.5 fJ/cs," *IEEE J. Solid-State Circuits*, vol. 55, no. 6, pp. 1577–1587, Jun. 2020.

[28] I. Kovacs and M. Neag, "New dual-loop topology for ring VCOs based on latched delay cells," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–5.

[29] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time $\Sigma\Delta$ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[30] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time $\Delta\Sigma$ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3344–3358, Dec. 2009.

[31] E. Gutierrez, L. Hernandez, F. Cardes, and P. Rombouts, "A pulse frequency modulation interpretation of VCOs enabling VCO-ADC architectures with extended noise shaping," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 2, pp. 444–457, Feb. 2018.

[32] J. Kim, T.-K. Jang, Y.-G. Yoon, and S. Cho, "Analysis and design of voltage-controlled oscillator based analog-to-digital converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 1, pp. 18–30, Jan. 2010.

[33] V. Unnikrishnan and M. Vesterbacka, "Mitigation of sampling errors in VCO-based ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 7, pp. 1730–1739, Jul. 2017.

[34] F. Cardes, E. Gutierrez, A. Quintero, C. Buffa, A. Wiesbauer, and L. Hernandez, "0.04-mm^2 103-dB-A dynamic range second-order VCO-based audio sigma delta ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1731–1742, Jun. 2018.

[35] A. Van der Ziel, *Noise in Solid State Devices and Circuits*. Hoboken, NJ, USA: Wiley, 1986.

[36] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*. London, U.K.: Oxford Univ. Press, 2011.

[37] F. Cardes, A. Quintero, E. Gutierrez, C. Buffa, A. Wiesbauer, and L. Hernandez, "SNDR limits of oscillator-based sensor readout circuits," *Sensors*, vol. 18, no. 2, p. 445, Feb. 2018.

[38] J. C. J. Paasschens, A. J. Scholten, and R. van Langevelde, "Generalizations of the Klaassen–Prins equation for calculating the noise of semiconductor devices," *IEEE Trans. Electron Devices*, vol. 52, no. 11, pp. 2463–2472, Nov. 2005.

[39] A. J. Scholten *et al.*, "The new CMC standard compact MOS model PSP: Advantages for RF applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1415–1424, May 2009.

[40] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Hoboken, NJ, USA: Wiley, 2017.

[41] C.-C. Tu, Y.-K. Wang, and T.-H. Lin, "A low-noise area-efficient chopped VCO-based CTDSM for sensor applications in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2523–2532, Oct. 2017.

[42] J. Marin, E. Sacco, J. Vergauwen, and G. Gielen, "A robust BBPLL-based 0.18-μm CMOS resistive sensor interface with high drift resilience over a −40°C–175°C temperature range," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1862–1873, Jul. 2019.

[43] P. G. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 2017.

Jonas Borgmans was born in Sint-Niklaas, Belgium, in 1994. He received the Ir. degree in electronics from Ghent University, Belgium, in 2017, where he is currently pursuing the Ph.D. degree with the Electronics and Information Systems Department. Since 2017, he has been with the Electronics and Information Systems Department, Ghent University. His main technical interest is analog circuit design, focusing on analog-to-digital converters.

Robbe Riem was born in Ypres, Belgium, in 1994. He received the Ir. degree in electronics from Ghent University, Belgium, in 2017, where he is currently pursuing the Ph.D. degree with the Electronics and Information Systems Department. Since 2017, he has been with the Electronics and Information Systems Department, Ghent University. His main technical interest is analog circuit design, focusing on sensor readout front-ends.

Pieter Rombouts (Senior Member, IEEE) received the Ir. and Ph.D. degrees from Ghent University in 1994 and 2000, respectively.

Since 1994, he has been with the Electronics and Information Systems Department, Ghent University, where he has been a Professor of analog electronics since 2005. His technical interests are signal processing, circuits and systems theory, analog circuit design, and sensor systems. He has served or is currently serving as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, and *Electronics Letters*.