A Cascaded Mode-Switching Sub-Sampling PLL With Quadrature Dual-Mode Voltage Waveform-Shaping Oscillator

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***Abstract*— A cascaded mode-switching sub-sampling PLL with quadrature dual-mode voltage waveform-shaping oscillator is proposed in this paper. The dual-mode voltage waveform-shaping oscillator is introduced to extend the tuning range and improve phase noise performance at mm-wave frequency, simultaneously. Meanwhile, the dual-mode quadrature topology is investigated to reduce the phase noise and quadrature phase error, compared to conventional quadrature oscillator. Then, the proposed oscillator is applied in a cascaded PLL with divider-less mode-switching sub-sampling loop, which can obtain the merits of high frequency-resolution, low loop noise, and wide frequency locking range. Both the dual-mode voltage waveform-shaping oscillator and the cascaded PLL are verified and fabricated in a 28-nm CMOS process. The FoM and FoM_T of the oscillator at 10 MHz offset are −188.2 dBc/Hz and −200.7 dBc/Hz respectively. The proposed PLL prototype exhibits a frequency range from 22.8 to 33.9 GHz with a typical power consumption of 41.7 mW. The phase noise across the frequency band is from −104.1 to −108.2 dBc/Hz at 1 MHz offset. The jitter FoM_j is −236.2 dB.**

***Index Terms*— Cascaded PLL, frequency synthesizer, millimeter-wave, mode-switching, oscillator, quadrature, sub-sampling, voltage waveform-shaping, wideband.**

I. Introduction

MILLIMETER-wave (mm-wave) multiple-band operations for the 5G wireless and point-to-point backhaul communication require phase-locked loops (PLLs) with wide tuning range at mm-wave frequencies. At the same time, to support the high data rates at Gb/s level, the complex modulation schemes are demanded, which put stringent requirements on the PLL integrated jitter and phase noise. At mm-wave bands, it is not easy to achieve wide tuning range and low phase noise simultaneously due to the limited quality factor of the resonator in mm-wave VCOs. Multiple oscillators can be used to relax the tuning range for each oscillator, at the expense of chip area [1]. Lately, PLLs utilizing high frequency crystal and large loop bandwidth have demonstrated low phase noise at mm-wave bands [2]–[4]. However, such crystal is expensive and would increase system cost. Another way to relax the trade-off is cascading injection-locked frequency multiplier (ILFM) after the PLL [5]–[7], then the PLL and VCO can work at lower frequency. Nevertheless, it is not easy to achieve robust operation over a wide frequency range, while multiple ILFMs would much increase the system complexity and chip area. In recent years, sub-sampling PLL (SSPLL) technique has shown promising results for achieving low in-band phase noise, which could even work without a divider [8]. Nevertheless, for a wideband sub-sampling PLL, a divider is often still used for initial frequency locking [9]. Recently, cascaded fractional-N sub-sampling mm-wave PLLs [10], [11] are reported. Such PLL architecture has the advantages of high-frequency-resolution and good in-band phase noise. However, due to the limited tuning range of mm-wave oscillator, the existing cascaded PLL can not cover a wide frequency range at mm-wave.

As the key block of mm-wave PLL, the wideband mm-wave oscillator is dramatically demanded, which determines the operation band of the PLL and phase noise out of loop bandwidth. However, due to the degrading quality factor of varactor and switch capacitor, it is a great challenge for mm-wave oscillator to achieve low phase noise and wide tuning range simultaneously. On the other hand, quadrature signals are widely used in communication systems [12]–[15]. The quadrature oscillator would introduce the trade-off between phase noise and phase error, especially at mm-wave. Recently, voltage waveform-shaping oscillators have been reported to obtain good phase noise performance by forming the square-like voltage waveform [16]–[18]. Nevertheless, the tuning range is limited by the parasitics of the complex resonator tanks. In the meantime, multi-core coupled oscillators are also reported to reduce the phase noise with relatively high power consumption [19]–[21]. To extend operation bandwidth, mode-switching oscillators are developed [22]–[26]. However, at mm-wave frequency, it is still not easy to achieve the wide tuning range and low phase noise simultaneously.

To address the challenges of wideband mm-wave PLL and oscillator design, this paper presents a cascaded

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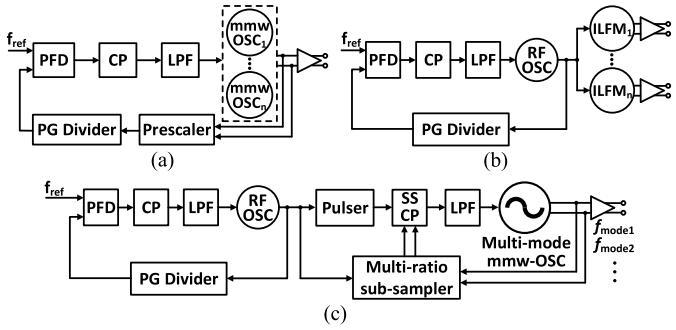

Fig. 1. (a) Multiple-oscillator mm-wave PLL. (b) PLL with injection-locked multipliers. (c) Proposed cascaded mode-switching PLL.

mode-switching sub-sampling PLL with a quadrature dual-mode voltage waveform-shaping oscillator. Fig. 1 compares the simplified architectures of multiple-oscillator PLL, PLL with ILFMs, and the proposed cascaded mode-switching sub-sampling PLL. The proposed PLL consists of a type-II PLL cascaded with a divider-less mode-switching sub-sampling loop. Thus, the structure has the merits of robust frequency control and low loop noise. Moreover, the mode-switching mechanism can support the wide frequency locking range without divider in the sub-sampling loop. A quadrature dual-mode voltage waveform-shaping oscillator is utilized in the mode-switching sub-sampling loop to achieve the low phase noise and wide tuning range, simultaneously. The dual-mode voltage waveform-shaping resonator generates four reconfigurable resonances to achieve voltage waveform-shaping in dual-mode, which much extends the tuning range at mm-wave frequency. Meanwhile, compared with conventional quadrature oscillator, the dual-mode quadrature topology can achieve lower phase noise and phase error. Finally, the dual-mode voltage waveform-shaping oscillator and the cascaded mode-switching PLL are implemented in a conventional 28-nm CMOS technology, respectively. The oscillator [27] achieves a 42.3% tuning range and a FoM_T of -200.7 dBc/Hz at 10 MHz offset. The proposed PLL exhibits a frequency range from 22.8 to 33.9 GHz. The phase noise across the frequency band is from -104.1 to -108.2 dBc/Hz at 1 MHz offset. The measured quadrature phase error is 0.5° to 1.2°. With a reference of 52 MHz, the jitter FoM_j is -236.2 dB.

The rest of the paper is organized as follows. Section II discusses the principle of dual-mode voltage waveform-shaping and the dual-mode quadrature topology. In Section III, the implementation and measurement of dual-mode waveform-shaping oscillator is introduced. Section IV presents the implementation and measurement of the cascaded PLL. Finally, a conclusion is drawn in Section V.

II. Principle of Quadrature Dual-Mode Voltage Waveform-Shaping Oscillator

A. Dual-Mode Voltage Waveform-Shaping

The voltage waveform-shaping oscillator or class-F oscillator utilizes odd harmonic voltage to resemble a square-wave voltage at the drain node, thus reducing the voltage across the transistor when it is conducting. Then, lower root-mean-square (rms) value of the impulse sensitivity function (ISF) can be achieved. A transformer based resonator is usually used to ensure the third harmonic by realizing two resonance peaks at the fundamental and third-harmonic frequencies. To overcome the bandwidth limitation of conventional voltage waveform-shaping oscillator and achieve the voltage waveform-shaping in dual-mode frequency range, two critical challenges are the reconfigurable multi-resonance resonator and the method of mode-switching.

Fig. 2(a) shows the transformer-coupled and capacitor-coupled resonators, both of which generate two resonances. For the transformer-coupled resonator, $\omega_1 = [LC(1 + k_m)]^{-1/2}$, $\omega_2 = [LC(1 - k_m)]^{-1/2}$ [28]. For the capacitor-coupled resonator, $\omega_1 = (LC)^{-1/2}$, $\omega_2 = [L(C + C_m)]^{-1/2}$ [22]. Dual-resonance resonator can be implemented to achieve waveform-shaping or mode-switching oscillator. To obtain multiple resonances, one approach is using multi-stage transformer coupled resonator [7]. However, the reconfiguration method is complex, while the implementation of layout meets great challenge. Another approach is to introduce transformer coupling and capacitor coupling together. As shown in Fig. 2(b), the multi-stage resonator is formed by two transformer-coupled resonators coupled by the capacitors C_{mp}. There are two possible coupling directions between the two transformer-coupled resonators, then an additional resonance of $\omega_3 = [L(C + C_{mp})(1 + k_m)]^{-1/2}$ is generated. Fig. 2(c) shows the proposed dual-mode voltage waveform-shaping resonator. The primary and secondary stages of the transformers are connected together by two pairs of capacitors (i.e., C_{mp} and C_{ms}), respectively. Thus, both stages have two possible coupling directions. Meanwhile, four resonances can be observed from the input impedance (i.e., ω_{e1}, ω_{e2}, ω_{o1}, and ω_{o2}) which can be expressed by (1) and (2), as shown at the bottom of the next page.

As shown in Fig. 3, to obtain the mode-switching mechanism, two switch-networks connect the primary and secondary stages of the two transformers, respectively. Each of the switch-network contains two pairs of switches (i.e., S_e for even mode and S_o for odd mode). The oscillator can operate in even or odd modes when the corresponding switch turns on and the other switch turns off. Fig. 4 shows the equivalent circuit of the resonator in even and odd modes. R_e and R_o are the turn-on resistance of S_e and S_o, respectively. As shown in Fig. 4(a), S_e turns on and S_o turns off in even mode. The two transformer based resonators are coupled in-phase. C_{ms} and C_{mp} are shorted by R_e. Then, such capacitors can be removed. On the other hand, when S_o turns on and S_e turns off, odd mode is selected. In such mode, the waveforms on the two ends of C_{ms} and C_{mp} are differential. Note that there is a virtual ground at the center of both C_{ms} and C_{mp}. Therefore, the capacitors can be reconnected at the virtual ground, which are equivalent to the parallel connected in the primary and secondary staged of transformers, respectively. The equivalent circuit in odd mode is shown in Fig. 4(b). It is notable that there is no current flowing through the turn-on switches in the proposed dual-mode voltage waveform-shaping oscillator, since the voltage waveforms at the two nodes of each switch have the same amplitude and phase [22].

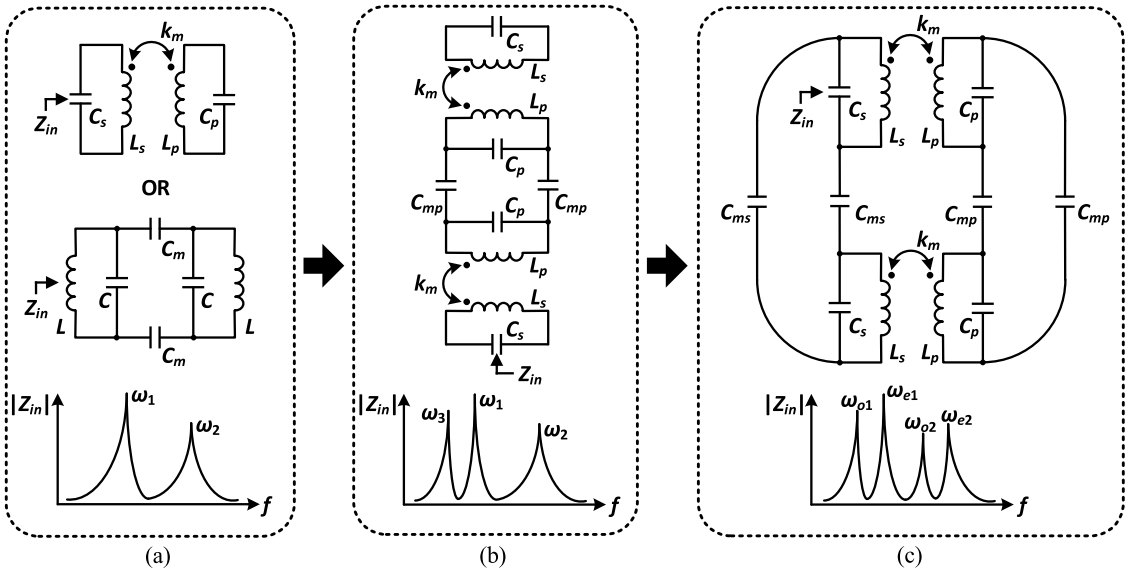

Fig. 2. (a) Transformer-coupled resonator and capacitor-coupled resonator. (b) Two transformer-coupled resonator with the primary stages coupled by capacitors. (c) Proposed dual-mode voltage waveform-shaping resonator.

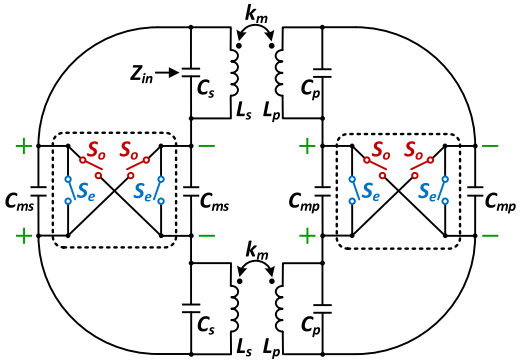

Fig. 3. Dual-mode voltage waveform-shaping resonator with mode switches.

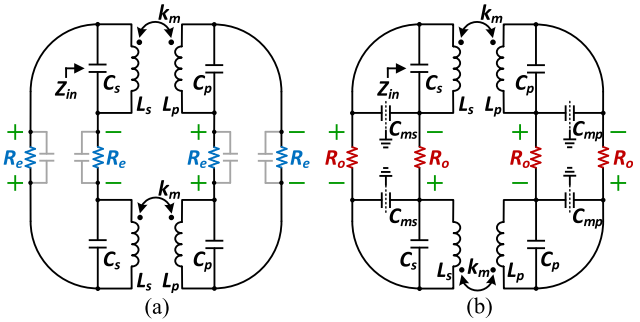

Fig. 4. Equivalent circuits of the resonator in (a) even mode and (b) odd mode.

Therefore, the switches are used to select the oscillation mode and would not degrade the performance of the desired mode even when they have non-zero turn-on resistance. Fig. 5 shows the simulated resonator input impedance in even and odd modes. As shown in Fig. 5(a), in the even mode, resonances at ω_{o1} and ω_{o2} damp with the decreasing of R_e, while resonances at ω_{e1} and ω_{e2} are almost unaffected. On the contrary, in the odd mode, resonances at ω_{e1} and ω_{e2} are suppressed, while resonances at ω_{o1} and ω_{o2} are constant. The resonances ω_{e1} and ω_{e2} are same as the transformer-coupled resonator, while the ω_{o1} and ω_{o2} are adjusted by C_{mp} and C_{ms}. Therefore, once designing the four resonances to meet the relationship of $\omega_{e2} = 3\omega_{e1}$ and $\omega_{o2} = 3\omega_{o1}$, the resonator can support the dual-mode voltage waveform-shaping at the fundamental frequency of ω_{e1} and ω_{o1}, respectively.

Simplified schematic of the proposed dual-mode voltage waveform-shaping oscillator is shown in Fig. 6. In each oscillator core, a tail current source is utilized to control the oscillator current. Both gates and drains of the two oscillator cores are connected by the mode switches and capacitors. The simulated square-like voltage waveforms in the even and odd modes are depicted in Fig. 7(a) and (b), respectively. The calculated ISF of the proposed oscillator is shown in Fig. 8. Compared to conventional class-B oscillator, lower rms of ISF (i.e., enhanced flatness in a period) is obtained in both even and odd modes, which leads to lower phase noise over wide frequency range.

$$\omega_{e1,e2}^2 = \frac{1 + \left(\frac{L_s C_s}{L_p C_p}\right) \pm \sqrt{1 + \left(\frac{L_s C_s}{L_p C_p}\right)^2 + \left(\frac{L_s C_s}{L_p C_p}\right)(4k_m^2 - 2)}}{2L_s C_s (1 - k_m^2)} \tag{1}$$

$$\omega_{o1,o2}^2 = \frac{1 + \frac{L_s(C_s + C_{ms})}{L_p(C_p + C_{mp})} \pm \sqrt{1 + \left[\frac{L_s(C_s + C_{ms})}{L_p(C_p + C_{mp})}\right]^2 + \frac{L_s(C_s + C_{ms})(4k_m^2 - 2)}{L_p(C_p + C_{mp})}}}{2L_s(C_s + C_{ms})(1 - k_m^2)} \tag{2}$$

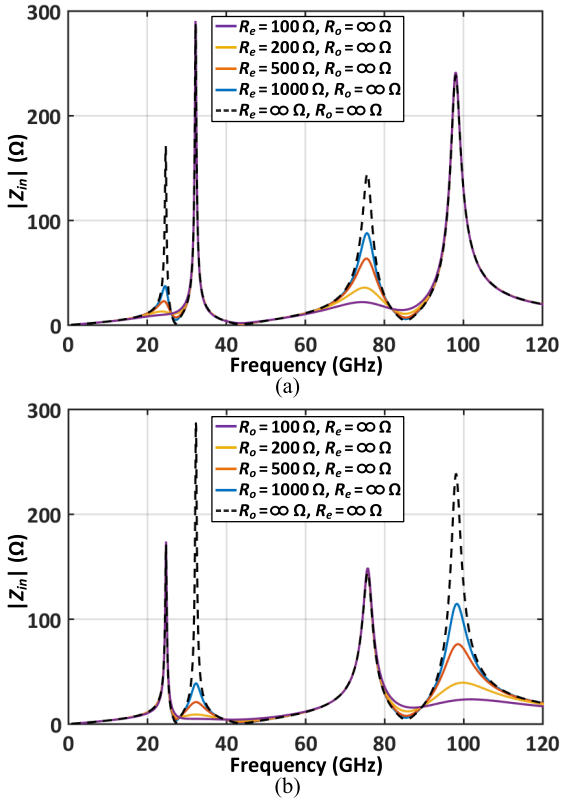

Fig. 5. Input-impedance of dual-mode voltage waveform-shaping resonator in (a) even mode (i.e., R_e changes, while R_o is $\infty\,\Omega$) and (b) odd mode (i.e., R_o changes, while R_e is $\infty\,\Omega$).

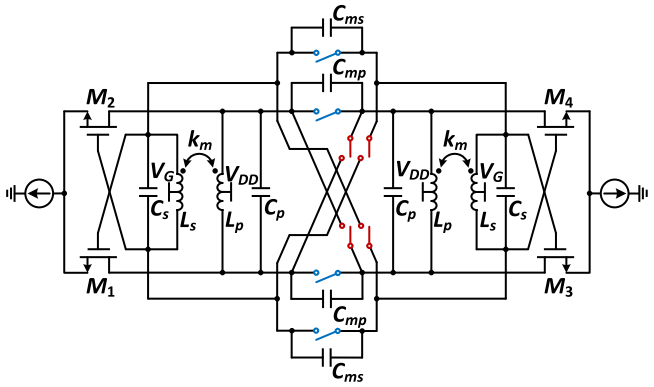

Fig. 6. Schematic of the dual-mode voltage waveform-shaping oscillator.

B. Dual-Mode Quadrature Oscillator

The deterioration of phase noise and quadrature phase error is a well-known trade-off in QVCO design [12], [13]. In this work, the dual-mode quadrature topology is proposed to achieve the quadrature signal in a wide frequency range. Compared with conventional QVCO, the proposed dual-mode quadrature oscillator can reduce not only the deterioration of phase noise, but also the quadrature phase error. The simplified configuration and dual-mode operation of the dual-mode quadrature oscillator is shown in Fig. 9(a) and (b), which consists of two pairs of oscillator cores, mode switching circuits, and quadrature coupling buffers. Mode switches and capacitors are implemented to couple each oscillator pair operating in-phase (even mode) or out-of-phase (odd mode),

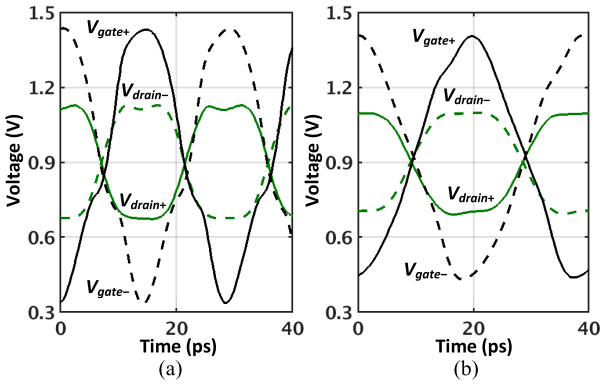

Fig. 7. Simulated voltage waveforms in (a) even mode and (b) odd mode.

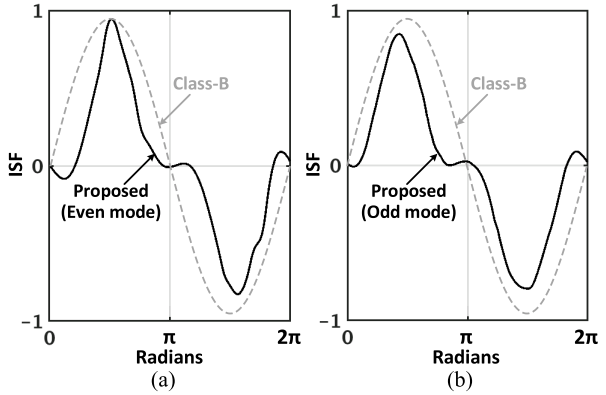

Fig. 8. Calculated ISF in (a) even mode and (b) odd mode.

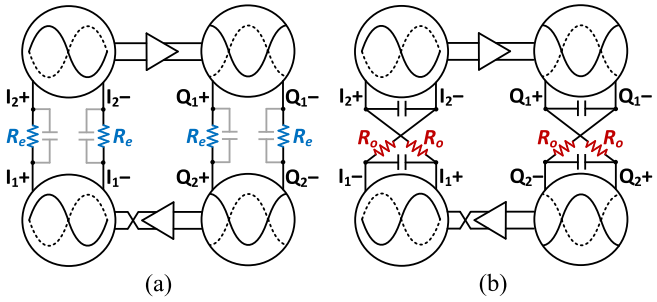

Fig. 9. (a) Even mode in-phase coupled quadrature ring. (b) Odd mode out-of-phase coupled quadrature ring.

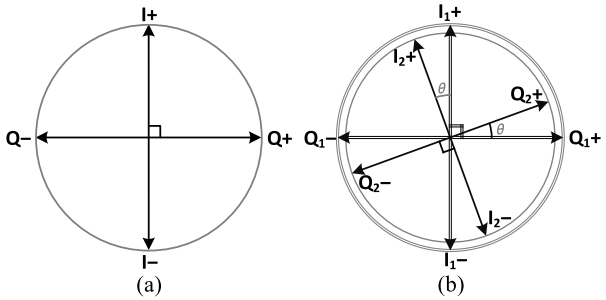

Fig. 10. Phase of (a) conventional QVCO and (b) proposed dual-mode quadrature oscillator.

generating the dual-mode operation frequency. To obtain the dual-mode quadrature signal, the coupling buffers couple the two oscillator pairs as a twisted ring. Differing from conventional QVCO, where each oscillator core injects the current to the other through the coupling buffer, the proposed dual-mode

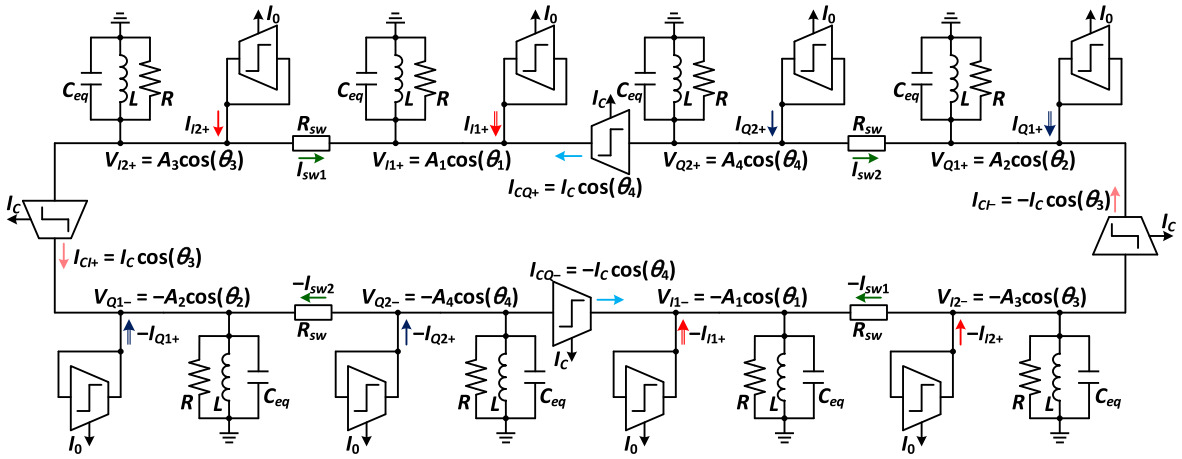

Fig. 11. Model of proposed dual-mode quadrature oscillator.

quadrature oscillator has two types of coupling conditions. Two oscillator cores get both the injection current from the coupling buffers and the coupling current from the turn-on switches, while the other two cores only have the reverse coupling current from the switches. The phase of conventional QVCO and proposed dual-mode quadrature oscillator is compared in Fig. 10. Due to the different coupling conditions, there is a phase shifting of θ between the two oscillator cores in each dual-mode oscillator pair, while the phase between the two pairs of oscillator is in quadrature, as shown in Fig. 10(b). Later, the analysis of phase noise and phase error will show that θ is helpful to reduce the deterioration of phase noise and phase error. It can be obtained from Fig. 9, except the value of equivalent capacitance, the coupling relationship of the four oscillator cores in even and odd mode is equivalent to be same. Therefore, the quadrature signal can be generated in dual-mode, and a uniform model can be utilized to analyze the operation condition in dual-mode.

As shown in Fig. 11, the model based on simplified LC cores is introduced to discuss the dual-mode quadrature topology, which consists of eight single-ended LC oscillators, four quadrature coupling transconductors, and four resistors of the coupling switches. In each LC resonator, C_{eq} presents the equivalent capacitance in even mode or odd mode. In the even mode, a smaller C_{eq} is used for a high operation frequency, while a larger C_{eq} leads to a low frequency in the odd mode. I_C and I_0 denote the amplitude of coupling current (i.e., $I_{CI\pm}$ and $I_{CQ\pm}$) and $-G_m$ current (i.e., $I_{I1\pm}$, $I_{I2\pm}$, $I_{Q1\pm}$, and $I_{Q2\pm}$), respectively. θ_1, θ_2, θ_3, and θ_4 are the phase of the output signal in each oscillator core. Note that $\theta = \theta_3 - \theta_1 = \theta_4 - \theta_2$. I_{sw1} and I_{sw2} are the currents flowing through the switches, which are generated from the voltage difference between two ends of each switch and expressed as follows:

$$I_{sw1} = (A_3\cos\theta_3 - A_1\cos\theta_1)/R_{sw} \quad (3)$$

$$I_{sw2} = (A_4\cos\theta_4 - A_2\cos\theta_2)/R_{sw}. \quad (4)$$

To intuitively analyze the principle of dual-mode quadrature oscillator, the current phasor and tank impedance of conventional QVCO and proposed type are compared in Fig. 12.

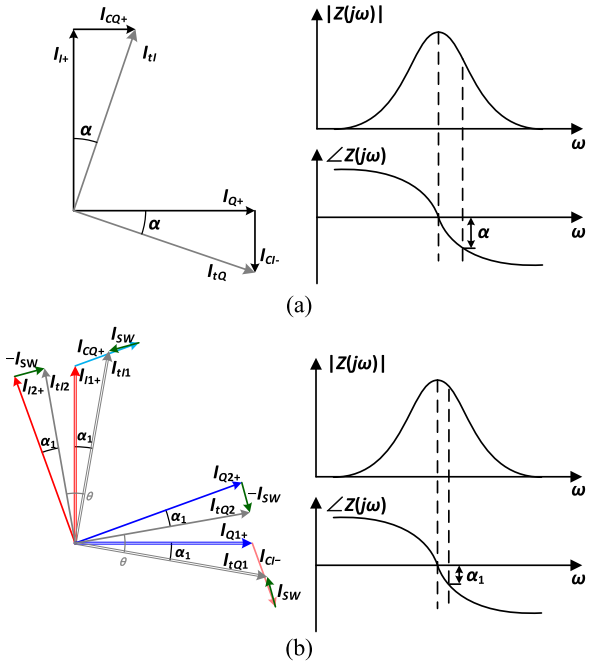

Fig. 12. Current phasor and tank impedance of (a) conventional QVCO and (b) proposed dual-mode quadrature oscillator.

For conventional QVCO, the current in each LC tank is formed by the oscillation current from cross-coupled pair and injected current from quadrature coupling network. Thus, a phase-shift α exists between the combined current I_t and self-oscillation current, which is expressed as $\alpha = arctan(I_C/I_0)$, as shown in Fig. 12(a). To support the steady state with α, there is a frequency deviation between oscillation frequency and tank resonance, which would cause the degradation of quality factor and phase noise. For the dual-mode quadrature type shown in Fig. 12(b), the injection current I_{CQ+} is in phase with I_{Q2+}, which is orthogonal to I_{I2+}. Due to the phase shifting θ between I_{1+} and I_{2+}, the phase between I_{CQ+} and I_{1+} is $\pi/2 - \theta$. Thus, the phase between the combined current and I_{I1+} is reduced. Moreover, the coupling current I_{sw} through R_{sw} has the effect of pulling the current of two oscillator cores together, resulting in a further reduced phase shifting

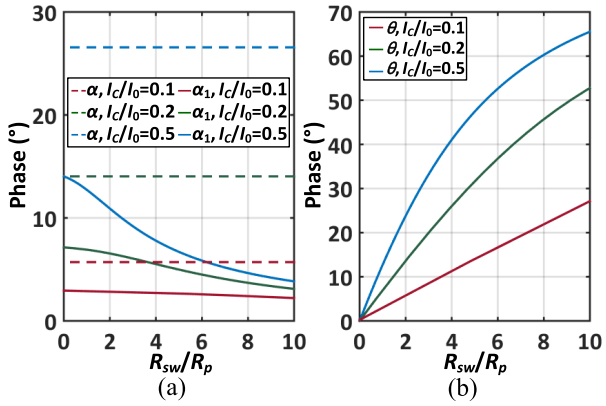

Fig. 13. (a) Simulated α and α_1.(b) Simulated θ.

between I_{I1+} and I_{tI1} (i.e., α_1). In the steady state, the four cores oscillate at the same frequency, thus the same phase shifting of α_1 is formed in each tank, as shown in Fig. 12(b). Considering θ is small in actual circuit, I_{sw} is approximately orthogonal to I_{I2+}. Then, α_1 and I_{sw} is expressed as:

$$\tan(\alpha_1) = \frac{(I_C - I_{sw})\cos\theta}{(I_C - I_{sw})\sin\theta + I_0} = \frac{I_{sw}}{I_0} \tag{5}$$

$$I_{sw} = (I_0 \sin\theta + I_C - 2I_{sw})R_p/R_{sw}. \tag{6}$$

Reorganizing (10), I_{sw} can be derived as:

$$I_{sw} = \frac{I_0 \sin\theta + I_C}{2 + R_{sw}/R_p}. \tag{7}$$

Therefore, α_1 and θ can be calculated once the parameters are determined. Fig. 13(a) depicts α and α_1 with the change of R_{sw}/R_p. It is clear to find that α_1 of the proposed topology is much lower than α in conventional QVCO. Meanwhile, α_1 is reduced with the increasing of R_{sw}/R_p. On the other hand, θ increases with the increasing of R_{sw}/R_p, as shown in Fig. 13(b). In practical implementation, the quadrature phase error is caused by the mismatches from asymmetric layout or process variation. To quantify and clarify the influence of the mismatches, each switch-coupled oscillator pair is considered as a whole oscillator. Applying the injection and coupling conditions to the generalized Adler's equation in [12] equations (8)-(11) can be obtained:

$$\frac{d\theta_1}{dt} = \omega_{01} + \frac{\omega_{01}}{2Q}\frac{(I_{C1} - I_{sw1})\sin(\theta_4 - \theta_1)}{I_{01} + (I_{C1} - I_{sw1})\cos(\theta_4 - \theta_1)} \tag{8}$$

$$\frac{d\theta_2}{dt} = \omega_{02} - \frac{\omega_{02}}{2Q}\frac{(I_{C2} - I_{sw2})\sin(\theta_3 - \theta_2)}{I_{02} + (I_{C2} - I_{sw2})\cos(\theta_3 - \theta_2)} \tag{9}$$

$$\frac{d\theta_3}{dt} = \omega_{01} + \frac{\omega_{01}}{2Q}\frac{I_{sw1}\sin(\theta_4 - \theta_3)}{I_{01} + I_{sw1}\cos(\theta_4 - \theta_3)} \tag{10}$$

$$\frac{d\theta_4}{dt} = \omega_{02} - \frac{\omega_{02}}{2Q}\frac{I_{sw2}\sin(\theta_3 - \theta_4)}{I_{02} - I_{sw2}\cos(\theta_3 - \theta_4)} \tag{11}$$

where the mismatches from coupling current, switches, G_m current, and LC tank resonant frequency are considered as:

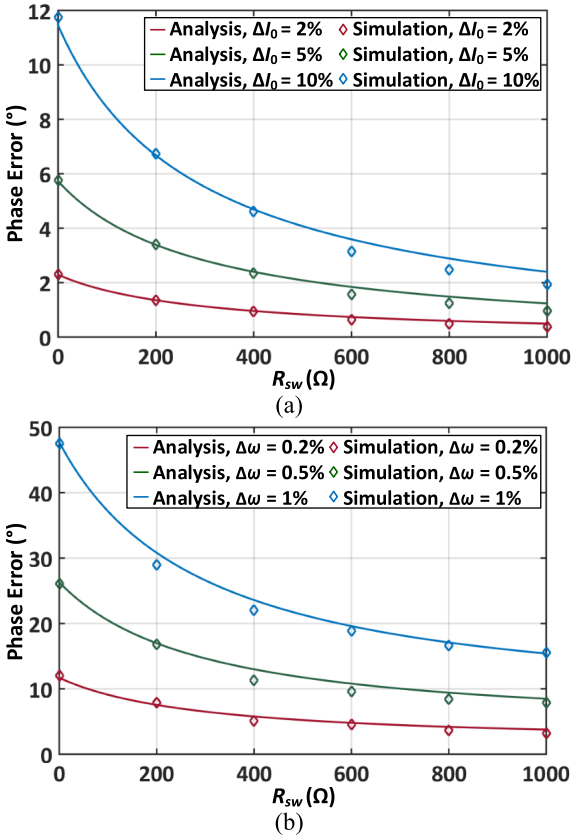

Fig. 14. Predicted and simulated phase error with different (a) ΔI_0 and (b) $\Delta\omega$ (I_0 = 2 mA, I_C = 1 mA, R_p = 300 Ω, Q = 10).

$I_{C1} = I_C + \Delta I_C/2$, $I_{C2} = I_C - \Delta I_C/2$, $I_{01} = I_0 + \Delta I_0/2$, $I_{02} = I_0 - \Delta I_0/2$, $I_{sw1} = I_{sw} + \Delta I_{sw}/2$, $I_{sw}2 = I_{sw} - \Delta I_{sw}/2$, $\omega_{01} = \omega_0 + \Delta\omega_0/2$, and $\omega_{02} = \omega_0 - \Delta\omega_0/2$. The resonant frequency $\omega_0 = 1/\sqrt{LC_{eq}}$ and $Q = RC_{eq}\omega_0$. Then, the quadrature phase error $\Delta\varphi$ compared to ideal state $\varphi = \pi/2$ is derived as (12), shown at the bottom of the page, where $m = I_C/I_0$ and $n = I_{sw}/I_0$. One interesting thing is found that the expression of phase error is similar to $\Delta\varphi$ in QVCO using phase-shifting coupling technique, and the effect of θ is same as phase-shifting in [12]. The large θ is, the less sensitive the quadrature phase is to the mismatch of each kind of currents and the resonant frequency. As discussed above, by appropriately choosing the switch's size, θ can be controlled by R_{sw}. Moreover, θ is independent on frequency. Thus, the proposed dual-mode quadrature topology is suitable for the generation of wideband quadrature signal. Fig. 14(a) shows the calculated and simulated quadrature phase error for 2%, 5%, and 10% mismatch of I_0 with the growing of R_{sw}, while the states for mismatch between resonance frequencies are compared in Fig. 14(b). As expected, the quadrature phase error is rapidly decreased with the increasing of R_{sw}. Note that the calculation and simulation match well when $R_{sw} < 400\Omega$. For a large R_{sw} corresponding to large θ, the I_{sw} is no

$$\Delta\varphi = \frac{\cos\theta}{\sin\theta + m - n}\frac{\Delta I_0}{2I_0} - \frac{\cos\theta}{\sin\theta + m - n}\frac{\Delta I_C - \Delta I_{sw}}{2(I_C - I_{sw})} - Q\frac{1 + (m-n)^2 + 2(m-n)\sin\theta}{(m-n)(\sin\theta + m - n)}\frac{\Delta\omega}{\omega_0} \tag{12}$$

longer orthogonal to I_{I2+}. With the increasing of θ, the phase between I_{I1+} and the whole current injected to I_{I1+} (i.e., $I_{CQ+} + I_{sw}$) is lower than $\pi/2 - \theta$, which corresponds to a larger effective θ in (12). Thus, the simulated quadrature phase error decreases faster than the calculation with the increasing of R_{sw}.

In order to find effects of resonator parameters on phase noise performance, it's necessary to quantify the effect of design parameters. Following the steps in [11], the phase noise of quadrature oscillator can be expressed by the modified Leeson equation [29]:

$$L(\Delta\omega) = 10\log\left[\frac{kTR_p}{2V_{\text{eff}}^2 Q_{\text{eff}}^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{13}$$

where k is the Boltzmann's constant, T is the absolute temperature, V_{eff} is the effective output amplitude, and Q_{eff} is the effective Q-factor caused by the frequency shifting. Regarding $V_{I1\pm}$ and $V_{Q1\pm}$ as the quadrature output, the effective output voltage is $V_{\text{eff}} = V_0[1 + (m-n)sin\theta]$. And Q_{eff} is

$$Q_{\text{eff}} = Q \Bigg/ \sqrt{1 + \left[\frac{(m-n)\cos\theta}{1 + (m-n)\sin\theta}\right]^2}. \tag{14}$$

As above-discussed, the turn-on resistance would not influence the resonances in demanded mode. However, for a switch-coupled dual-core oscillator, the influence of the switch's on-resistance on the phase noise is non-negligible. For a dual-core oscillator, the equivalent impedance of the LC tanks with the coupling switch at $\Delta\omega$ offset is expressed as [30]

$$\left|Z_{\text{eq}}(\Delta\omega)\right|^2 = \frac{|Z_{\text{tank}}|^2}{2}\frac{2R_{sw}^2 + |Z_{\text{tank}}|^2}{R_{sw}^2 + |Z_{\text{tank}}|^2} \tag{15}$$

where R_{sw} represents the turn-on resistance of mode switches. Z_{tank} is the impedance of a LC tank. Once the two oscillator cores are ideal coupled (i.e., $R_{sw} = 0$), the phase noise can be improved by 3 dB compared with single core oscillator. However, if R_{sw} is large enough (i.e., $R_{sw} \gg Z_{\text{tank}}$), Z_{eq} is approximately equal to Z_{tank}, which leads to a phase noise same as single core oscillator. Then, the expression of phase noise can be rewritten as:

$$L(\Delta\omega) = 10\log\left[\frac{2kTR_p}{V_{\text{eff}}^2}\left(\frac{|Z_{\text{eq}}|}{R_p}\cdot\frac{Q}{Q_{\text{eff}}}\right)^2\right]. \tag{16}$$

Fig. 15 shows the calculated and simulated suppression of phase noise compared with ideal-coupled case (i.e., $R_{sw} = 0$). It's notable that, phase noise is reduced with the increasing of R_{sw}. When $R_{sw} > 800\ \Omega$, the phase noise's reduction is not obvious. It can also be concluded from (16): when R_{sw} increases, the increased Q_{eff} reduces the phase noise, while the increased Z_{eq} increases the phase noise. Thus, when R_{sw} is too large, the dual-core oscillator will be decoupled, which will neutralize the effect of the increased Q_{eff} and cause the deterioration of phase noise. Meanwhile, according to the implementation, if R_{sw} is too large, the dual-mode operation could not be sustained sufficiently. With the asymmetry introduced by quadrature coupling transistors, there will be current

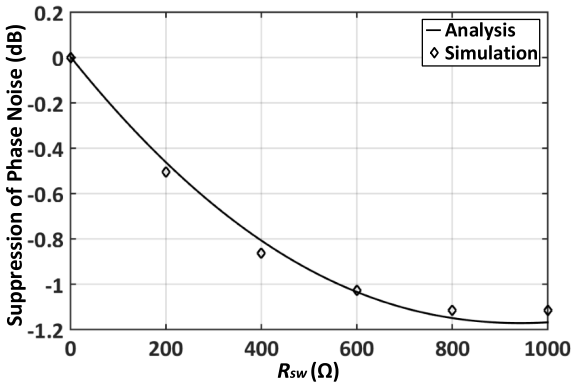

Fig. 15. Predicted and simulated change of phase noise with the increasing of R_{sw}.

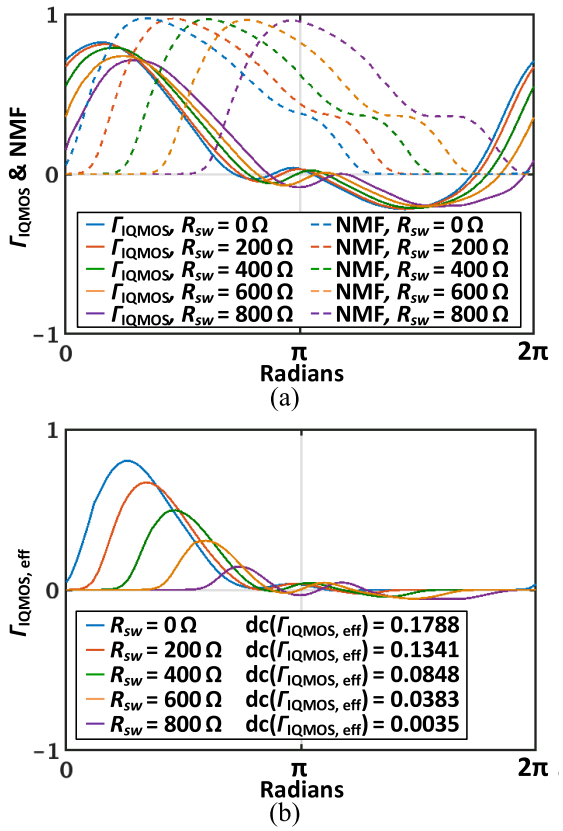

Fig. 16. Simulated (a) ISF, NMF, and (b) ISF_{eff} of the quadrature coupling transistor.

flowing through R_{sw} as mentioned above. For a R_{sw} of 500 Ω, the simulated noise contributions from R_{sw} at 1 MHz and 10 MHz offset are 0.6% and 0.68%, respectively.

In the design of quadrature oscillator, the flicker noise contributed from the coupling devices is usually non-negligible. According to [31], the flicker noise up-conversion is related to the dc value of effective ISF. The effective ISF is defined as $\Gamma_{\text{eff}}(\omega_0 t) = \Gamma(\omega_0 t)\cdot\alpha(\omega_0 t)$, where $\Gamma(\omega_0 t)$ and $\alpha(\omega_0 t)$ are the functions of ISF and noise modulation function (NMF). Fig. 16(a) shows the simulate ISF and NMF of the quadrature coupling transistor. With R_{sw} increasing from 0 to 800 Ω, the phase shift of θ is increased from 0° to 17.5°, while the phase difference between ISF and NMF is much increased. As shown in Fig. 16(b), with the increasing of R_{sw}, rms of

TABLE I
OSCILLATOR'S SUMMARY AND COMPARISON WITH STATE-OF-THE-ARTS

		This Work	ISSCC13 [33]	ISSCC16 [5]	JSSC17 [19]	ISSCC18 [20]	JSSC18 [24]	JSSC18 [34]	ISSCC19 [26]
Technology		**CMOS 28-nm**	SiGe 130-nm	CMOS 130-nm	SiGe 55-nm	SiGe 130-nm	CMOS 65-nm	CMOS 28-nm	CMOS 65-nm
Supply Voltage (V)		**0.9**	1.5	1.3	1.2	3	0.9	1	0.65
Frequency (GHz)		**20.7∼31.8**	28∼37.8	26.5∼29.7	17.4∼20.3	13.2∼15.4**	42.9∼50.6	27.3∼31.2	25∼38
Tuning Range (%)		**42.3**	29.8	11.4	15.4	16	16.5	14	41.2
Power (mW)		**5.5**	10.5	38.6*	36	72	21.5	22	21.6
Phase Noise (dBc/Hz)	@1 MHz	**−102.5**	−103.6	−106.8	−118.5	−124	−106.1	−106	−108.8**
	@10 MHz	**−127.4**	−127**	−118.9	−139.5**	−143**	−122**	−126	−130**
FoM (dBc/Hz)	@1 MHz	**−183.3**	−183.9	−179.4	−188.7	−189	−186.6	−181	−184.3
	@10 MHz	**−188.2**	−185.7	−171.5	−189.7	−188	−182.0	−181	−185.5
FoM_T (dBc/Hz)	@1 MHz	**−195.8**	−193.5	−180.5	−192.5	−193	−190.8	−184	−196.6
	@10 MHz	**−200.7**	−195.3	−172.6	−193.5	−192	−186.4	−184	−197.8

*Low frequency oscillator + injection-locked oscillator **Estimated from the figures in references

$$\text{FoM} = L(\triangle f) - 20\log_{10}\left(\frac{f_0}{\triangle f}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\text{mW}}\right) \quad \text{FoM}_\text{T} = L(\triangle f) - 20\log_{10}\left(\frac{f_0}{\triangle f}\cdot\frac{TR}{10}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\text{mW}}\right)$$

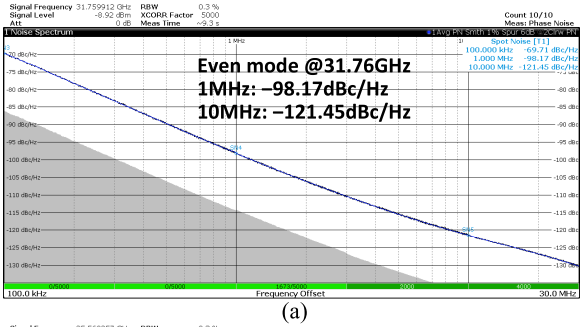

Fig. 17. Measured phase noise of the oscillator in (a) even mode and (b) odd mode.

Γ_{eff} is obviously reduced, while the symmetry of Γ_{eff} is much improved. The dc value of Γ_{eff} is reduced from 0.1788 to 0.0035, which leads to a reduced flicker noise up-conversion of the quadrature coupling transistor.

III. IMPLEMENTATION AND MEASUREMENT OF DUAL-MODE WAVEFORM-SHAPING OSCILLATOR

To verify the mechanism mentioned above, the dual-mode voltage waveform-shaping oscillator [27] is designed and fabricated in a conventional 28-nm CMOS technology. In each oscillator core, a resistor loaded tail current source is utilized to control the oscillator current and suppress the flicker noise up-conversion. Three switch capacitors (i.e., 2 binary control bits, $B_0 \sim B_1$) across the secondary winding form the coarse tune. Fifteen switch capacitors (i.e., 4 binary control bits, $B_2 \sim B_5$) and one pair of varactors are used to introduce the mid-coarse tune and fine tune, respectively. One bit B_{mode} is set to control the switch-mode. According to (1) and (2), the primary and secondary capacitance need to be tuned simultaneously to sustain the demanded ratio of resonances. Thus, the overlaps of adjacent coarse tune bands are designed to be high enough. For a certain required frequency, there are several capacitor settings with different capacitor ratio. Then, there are more chances to get an optimized voltage waveform-shaping effect.

Frequency and phase noise of the oscillator are measured by R&S FSW43 and FSWP50, respectively. The measurement results show a dual-band frequency tuning from 23.5 to 31.8 GHz (i.e., 30% tuning range) in even mode and 20.7 to 25.6 GHz (i.e., 21.2% tuning range) in odd mode, respectively. Thus, a dual-mode wide tuning range of 42% is achieved at the center frequency of 26.25 GHz. The overlap of two modes is 2 GHz, while the overlap of adjacent coarse tune bands is larger than 40%. Measured phase noise of two modes are shown in Fig. 17. In the even mode, the phase noise is −98.17 dBc/Hz at 1 MHz and −121.45 dBc/Hz at 10 MHz with a carrier of 31.76 GHz. In the odd mode, the phase noise is −102.46 dBc/Hz at 1 MHz and −127.40 dBc/Hz at 10 MHz with a carrier of 25.56 GHz. The measured power consumption is 5.5 mW with a supply voltage of 0.9 V. Measured results are summarized and compared with the relevant state-of-the-art oscillators in Table I. Quad-core coupled oscillator [20] shows the lowest phase noise at a lower frequency. However, it costs around 13 times power consumption comparing to this work. It is notable that the proposed oscillator exhibits a FoM of −183.3 dBc/Hz at 1 MHz and −188.2 dBc/Hz at 10 MHz with a carrier frequency of 25.56 GHz. Meanwhile, the corresponding FoM_T of −195.8 dBc/Hz at 1 MHz and −200.7 dBc/Hz at 10 MHz is the state-of-the-art around 30 GHz.

IV. IMPLEMENTATION AND MEASUREMENT OF PLL

A. Configuration of Cascaded Mode-Switching PLL

Fig. 18 shows the block diagram of the proposed cascaded mode-switching sub-sampling PLL. The first loop in the

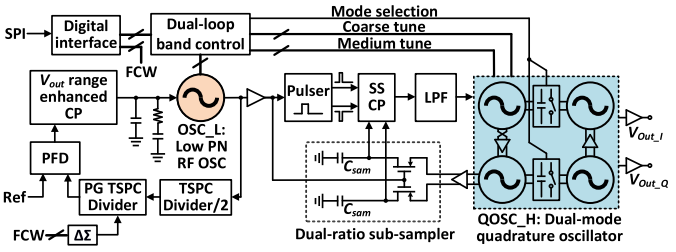

Fig. 18. Architecture of the cascaded mode-switching sub-sampling PLL.

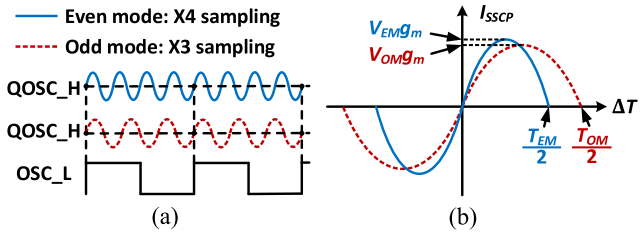

Fig. 19. Waveforms (a) and sub-sampling characteristic (b) of even mode (EM) and odd mode (OM) operation.

proposed PLL generates low phase noise signal at single-GHz bands. The low frequency oscillator (OSC_L) is designed with a high quality factor resonator and large voltage swing to achieve low phase noise. A general 52 MHz temperature compensated crystal oscillator (TCXO) is chosen to provide the first loop's reference clock rather than high-frequency low-phase-noise crystal. A 20-bit MASH-111 delta-sigma modulator is used to achieve 100 Hz frequency resolution of the first loop. The sub-sampling loop uses a quadrature dual-mode voltage waveform-shaping oscillator (QOSC_H) to generate the wideband IQ signal at mm-wave. The triple and quadruple sub-sampling locking range fully covers the dual-mode frequency range of QOSC_H (i.e., odd mode and even mode), respectively. Fig. 19(a) illustrates the waveforms of dual-ratio sub-sampling, while Fig. 19(b) shows the sub-sampling phase detector's characteristic. Due to the high reference frequency (i.e., the output of first PLL loop), the loop bandwidth of the sub-sampling loop can be much larger than the first loop, which helps to reduce the loop filter area. In each mode, phase noise of the cascaded PLL for even and odd modes can be expressed as equations (17) and (18), respectively, where L_{loop1} is the in-band phase noise of the first loop. The f_{loop1} and f_{loop2} are the loop bandwidths of the first loop and second SSPLL loop, respectively.

$$L_{\text{EM}} \cong \begin{cases} 16L_{\text{loop1}}, & \Delta f < f_{\text{loop1}} \\ 16L_{\text{VCO\_L}}, & f_{\text{loop1}} \le \Delta f \le f_{\text{loop2}} \\ L_{\text{VCO\_H,EM}}, & \Delta f > f_{\text{loop2}} \end{cases} \tag{17}$$

$$L_{\text{OM}} \cong \begin{cases} 9L_{\text{loop1}}, & \Delta f < f_{\text{loop1}} \\ 9L_{\text{VCO\_L}}, & f_{\text{loop1}} \le \Delta f \le f_{\text{loop2}} \\ L_{\text{VCO\_H,OM}}, & \Delta f > f_{\text{loop2}} \end{cases} \tag{18}$$

When the offset frequency is lower than f_{loop1}, the phase noise is determined by the in-band phase noise of the first loop and the multiplication ratio in each mode.

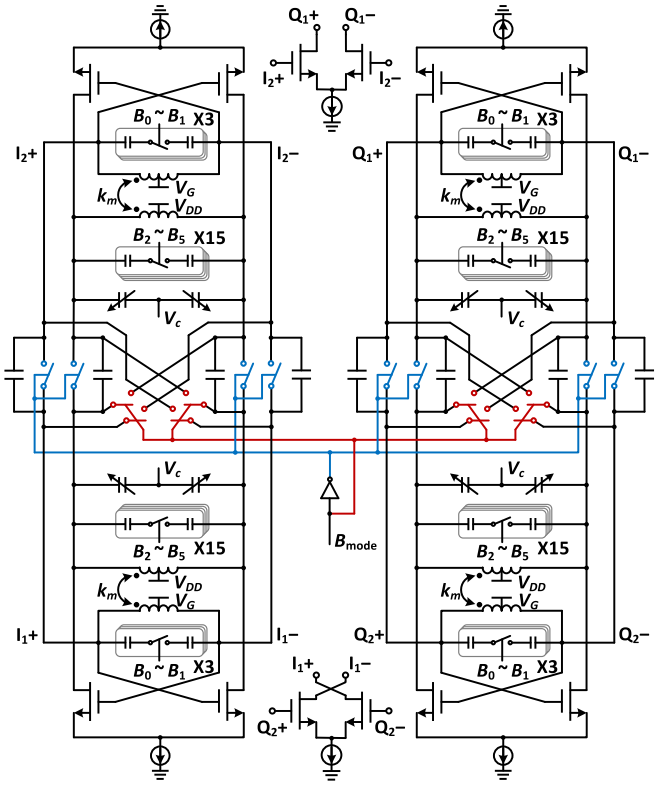

Fig. 20. Schematic of the quadrature dual-mode voltage waveform-shaping oscillator.

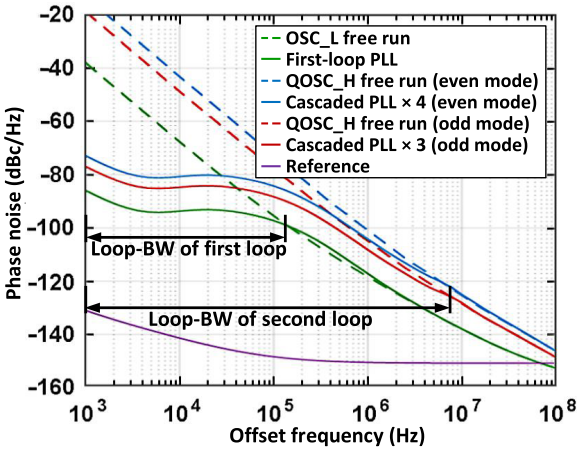

Fig. 21. Simulated PLL phase noise.

For $f_{\text{loop1}} < \Delta f < f_{\text{loop2}}$, the PLL's phase noise is approximated as the phase noise of low frequency oscillator multiplied by the square of sub-sampling ratio in each mode. Then, for the offset frequency higher than f_{loop2}, the PLL has the same phase noise as the dual-mode quadrature oscillator. Therefore, the phase noise performance of the two oscillators and the frequency range of the dual-mode quadrature oscillator are the key factor for the proposed PLL architecture.

B. Implementation of QOSC_H and OSC_L

Circuit implementation of the proposed quadrature dual-mode voltage waveform-shaping oscillator is shown

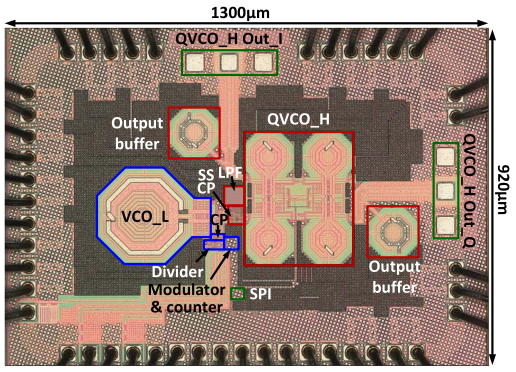

Fig. 22. Chip micrograph of the PLL.

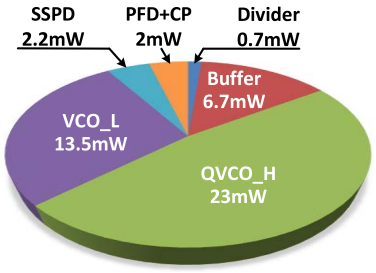

Fig. 23. Power consumption of each key blocks.

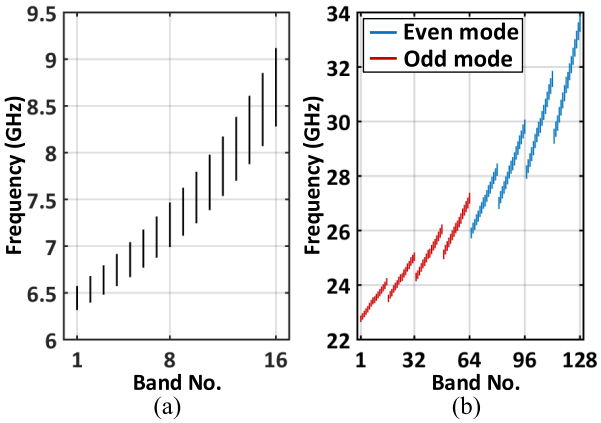

Fig. 24. Measured frequency range of the (a) OSC_L and (b) QOSC_H.

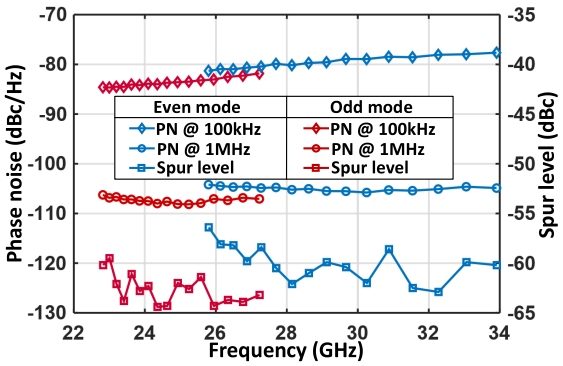

Fig. 25. Measured phase noise and spur level.

in Fig. 20, which consists of two dual-mode voltage waveform-shaping oscillator, and quadrature coupling buffers. The circuit implementation of each oscillator core is same as section III. Note that the turn-on resistance of the mode-switch PMOS is about 500 Ω to balance the quadrature phase error, phase noise, and select the required mode effectively. Meanwhile, the common source buffer pairs are employed to couple the drains of each oscillator cores to form the quadrature operation. Tail current source is used in each buffer pair to control the coupling current. The quadrature signal is output through the inductor-biased buffer.

The RF oscillator OSC_L is designed as the class-B type. Thick-oxide MOSFETs and a supply of 2.5 V are introduced to increase the maximum oscillation voltage swing and improve the phase noise. Meanwhile, the stepped-impedance (SI) inductor can achieve higher quality-factor by using stepped-width and stacked top thick metal [32]. Simulation results show that the quality-factor of inductor is increased from 21 to 25 at 8 GHz. To achieve a small K_{vco} and reduce the flicker noise up-conversion, 4-binary-bit switch-capacitor array is employed for coarse frequency tuning while a pair of varactors is used to achieve continuous frequency tuning. The oscillator is designed to completely cover the frequency from 6.5 to 9 GHz, which has the corresponding triple and quadruple sub-sampling locking range from 19.5 to 36 GHz.

C. Fabrication and Experimental Results

The cascaded mode-switching PLL is designed and fabricated in a conventional 28-nm CMOS technology. The simulated phase noise of the low-phase-noise RF oscillator (OSC_L), quadrature dual-mode voltage waveform-shaping oscillator (QOSC_H), and cascaded PLL output are illustrated and compared in Fig. 21. The loop bandwidth of the sub-sampling PLL is around 7 MHz. It can be seen that, in both modes, the cascaded PLL's phase noise is significantly reduced within the loop bandwidth. The chip micrograph of the cascaded PLL is shown in Fig. 22. The chip size including pad ring is 1.19 mm^2. The typical power consumption is 41.7 mW, as shown in Fig. 23.

Fig. 24 (a) and (b) depict the measured frequency range of the OSC_L and QOSC_H, respectively. The OSC_L has a frequency range of 6.4 to 9.1 GHz, while the dual-mode quadrature oscillator's frequency range covers 25.8 to 33.9 GHz in the even mode and 22.8 to 27.2 GHz in the odd mode. Thus, the cascaded PLL can lock over a wideband frequency range from 22.8 to 33.9 GHz. The phase noise and spur level over the frequency are depicted in Fig. 25. Fig. 26 shows the measured spectrum and phase noise at 33.9 GHz (even mode) and 25.4 GHz (odd mode). For integer-N mode, the measured output integrated jitters are 378.05 fs in the even mode and 298.67 fs in the odd mode. For fractional-N mode, the measured output integrated jitters are 382.05 fs in the even mode and 306.18 fs in the odd mode. The measured spectrums in the two modes are shown in Fig. 27. The reference spurious levels are −61.73 dBc in even mode and −65.41 dBc in odd mode, while the fractional spurious levels are −60.12 dBc in even mode and −65.41 dBc in odd mode. Fig. 28 provides the measured fractional spur as function of the fractional

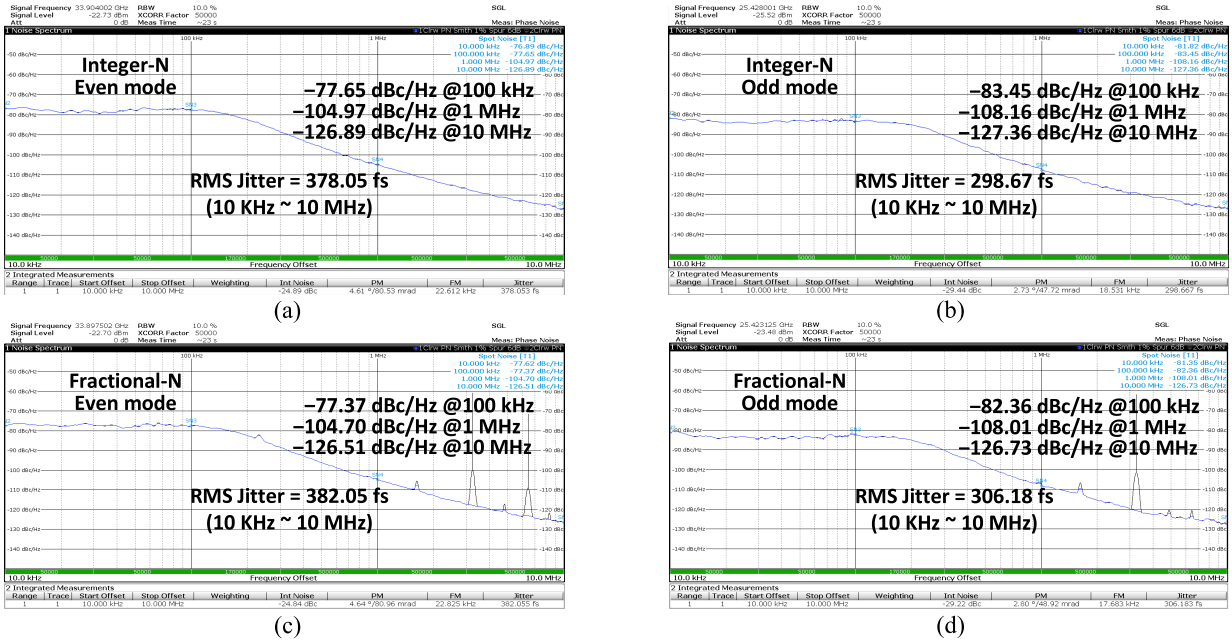

Fig. 26. Measured phase noise of the cascaded PLL in (a) integer-N even mode, (b) integer-N odd mode, (c) fractional-N even mode, and (d) fractional-N odd mode.

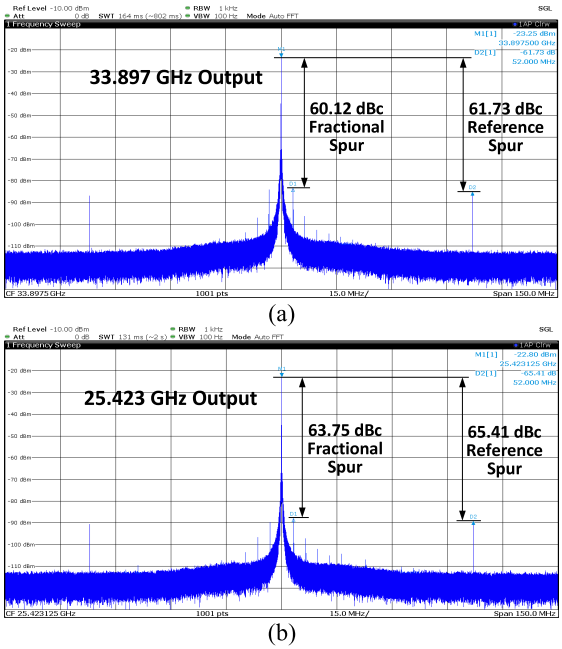

Fig. 27. Measured spectrum in (a) even mode and (b) odd mode.

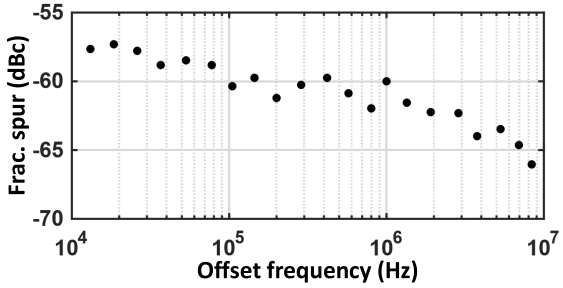

Fig. 28. Measured fractional spur as function of the fractional frequency offset from the carrier.

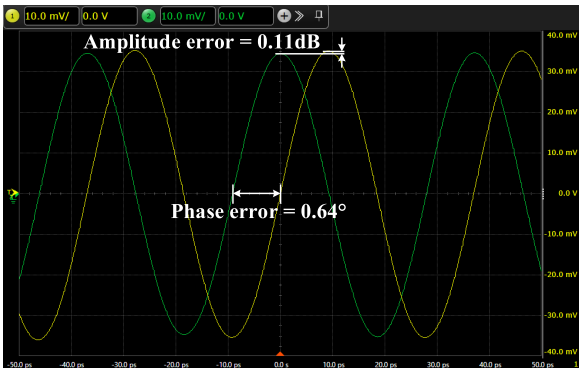

Fig. 29. Measured quadrature output.

frequency offset from the carrier of 489 $\times f_{\text{ref}}$. Fig. 29 shows the measured quadrature output. The measured quadrature phase error is from 0.5° to 1.2°.

As shown in Table II, the proposed cascaded mode-switching PLL is compared with state-of-the-art mm-wave PLLs. With the lowest f_{ref}, the proposed cascaded PLL demonstrates a wide frequency range of competitive frequency range of 39.2% with competitive phase noise and jitter performance. Ref. [1] performs the widest frequency range using two oscillators. However, the phase noise is much worse than our work. For a fair comparison with the proposed PLL, the cost and frequency of the reference crystal should be considered for the estimation of system performance and cost. FoM_{r} is the FoM_{j} normalized to 52 MHz f_{ref}. It can be seen that the proposed PLL not only achieves the wide frequency range at mm-wave and high overall performance of FoM_{r}, but also much decreases the system cost.

TABLE II
PLL'S SUMMARY AND COMPARISON WITH STATE-OF-THE-ARTS

		This Work	ISSCC15 [1]	JSSC15 [2]	ISSCC16 [35]	JSSC17 [36]	ISSCC18 [6]	ISSCC18 [3]	ISSCC19 [37]
Technology		**CMOS 28-nm**	SOI 32-nm	CMOS 40-nm	CMOS 65-nm	CMOS 65-nm	CMOS 65-nm	CMOS 40-nm	CMOS 65-nm
Frequency (GHz)		**22.8∼33.9**	13∼28	21.4∼25.1	25.3∼30.4	50.2∼66.5	25∼30	33.6∼38.2	30.6∼34.2
Tuning Range (%)		**39.2**	72.5	15.9	18	28	18.2	4.2	13
Ref. Frequency (MHz)		**52**	104.5	390	3500	100	120	120	100
Power (mW)		**41.7**	31	64	261	46	36.4	68	35
PN$^{\triangle}$ (dBc/Hz)	@100 kHz	**−82.6**	−80*	−97*	−98*	−88.9	−90.8	−89	−89.6
	@1 MHz	**−108.2**	−81.2	−102.5	−107*	−100.7	−103.3	−77.3	−101.3
	@10 MHz	**−126.8**	−115.8	−98.3	−118*	−128.7	−120.1	−115.9	−119.6
RMS jitter (fs)		**306.2**	1030*	394	103.9	962	206	577	197.6
Jitter integ. Range (Hz)		**10k∼10M**	10k∼100M	100k∼100M	100k∼100M	1k∼40M	1k∼100M	10k∼1M	30k∼10M
FoM$_{\rm j}$ (dB)		**−236.2**	−224.8	−230.0	−235.5	−235.1	−238.1	−226.5	−238.6
FoM$_{\rm r}$ (dB)		**−236.2**	−221.8	−221.3	−214.0	−232.3	−234.5	−222.9	−235.7
FoM @1 MHz (dBc/Hz)		**−179.9**	−154.2	−172.4	−170.9	−172.0	−175.7	−147.0	−173.8
Fractional Spur (dBc)		**–55.6**	N/A	N/A	N/A	–52.2	N/A	–55	–42.2
Type		**Frac.-N**	Frac.-N	Int.-N	Int.-N	Frac.-N	Frac.-N	Frac.-N	Frac.-N
Phase		**Quad.**	Diff.	Eight	Diff.	Diff.	Quad.	Diff.	Diff.
Chip Size (mm^2)		**1.19**	1.12	N/A	2.4	2.89	1.6**	1.2	0.79**

$^{\triangle}$Normalized to 25 GHz *Estimated from the figures in references **Excluding pads

$$\text{FoM} = L(\triangle f) - 20\log_{10}\left(\frac{f_0}{\triangle f}\right) + 10\log_{10}\left(\frac{P_{DC}}{1\text{mW}}\right) \quad \text{FoM}_{\rm j} = 10\log\left[(\frac{\sigma_t}{1\text{s}})^2 \cdot \frac{P_{DC}}{1\text{mW}}\right] \quad \text{FoM}_{\rm r} = 10\log\left[(\frac{\sigma_t}{1\text{s}})^2 \cdot \frac{P_{DC}}{1\text{mW}} \cdot \frac{f_{\rm ref}}{52\text{MHz}}\right]$$

V. CONCLUSION

A cascaded mode-switching sub-sampling PLL with quadrature dual-mode voltage waveform-shaping oscillator is proposed in this paper. The fractional-N PLL achieves low phase noise RF signal with high frequency-resolution, while the mode-switching sub-sampling loop multiplies the RF signal to mm-wave frequency and extends the frequency locking range. Dual-mode voltage waveform-shaping oscillator is introduced to obtain wide tuning range and low phase noise at mm-wave bands. The dual-mode quadrature topology is investigated to reduce the phase noise and quadrature phase error. The dual-mode voltage waveform-shaping oscillator and the cascaded mode-switching PLL are fabricated in a conventional 28-nm CMOS process, respectively. The oscillator achieves a state-of-the-art FoM$_{\rm T}$ of −200.7 dBc/Hz at 10 MHz offset. With a conventional 52 MHz reference crystal, the proposed PLL exhibits a wideband frequency range from 22.8 to 33.9 GHz with competitive phase noise performance.

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