A Compact Transformer-Based Fractional-N ADPLL in 10-nm FinFET CMOS

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***Abstract*— In this article, we introduce a fractional-N all-digital phase-locked loop (ADPLL) architecture based on a single LC-tank, featuring an ultra-wide tuning range (TR) and optimized for ultra-low area in 10-nm FinFET CMOS. Underpinned by excellent switches in the FinFET technology, a high turn-on/off capacitance ratio of LC-tank switched capacitors, in addition to an adjustable magnetic coupling technique, yields almost an octave TR from 10.8 to 19.3 GHz. A new method to compensate for the tracking-bank resolution can maintain its quantization noise level over this wide TR. A new scheme is adopted to overcome the metastability resolution problem in a fractional-N ADPLL operation. A low-complexity TDC gain estimator reduces the digital core area by progressive averaging and time-division multiplexing. Among the published fractional-N PLLs with an area smaller than 0.1 mm^2, this work achieves an rms jitter of 725 fs in an internal fractional-N mode of ADPLL's phase detector (2.7–4.825 GHz) yielding the best overall jitter figure-of-merit (FOM) of −232 dB. This topology features small area (0.034 mm^2), wide TR (56.5%) and good supply noise rejection (1.8%/V), resulting in FOMs with normalized TR (FOM_T) of −247 dB, and normalized TR and area (FOM_{TA}) of −262 dB.**

***Index Terms*— All-digital phase-locked loop (ADPLL), transformer, metastability, time-to-digital converter (TDC), TDC gain estimator, FinFET, compact area, fractional-N, wide tuning range (TR).**

I. Introduction

FREQUENCY synthesizers are widely used in mainstream SoC applications, which range from RF wireless to wireline communications, such as high-speed SERDES ([1]). They are further used in processor and memory clock generation [2], with high performance computing (HPC) growing rapidly due to the recent emergence of artificial intelligence (AI) [3]. The wireline and clock generation applications simultaneously require low jitter, small area, wide tuning range, and supply noise rejection.

TABLE I
COMPARISON OF RING-BASED AND LC-TANK ADPLLS

	Ring	Conventional LC Tank	Design Goal
Supply Noise Rejection	Poor	Good	**Good**
Tuning Range	Wide	Narrow	**Wide**
Area	Small	Large	**Small**
Jitter	Poor	Good	**Medium**

There are two general types of oscillators: ring-based and conventional LC tanks, as indicated in Table I. An inverter-based ring oscillator (RO) is the most common solution for wireline communications due to its wide tuning range and small area. However, it exhibits poor jitter and supply noise rejection, especially in advanced CMOS [4], [5]. A recent trend of injection locking a RO to a reference clock requires the clocking source and its distribution to be of very high purity [6], which is not readily available in a highly integrated SoC environment. An LC tank oscillator could solve these two drawbacks, but it suffers from a narrow tuning range and large area due to the LC-tank inductor [7], [8].

In state-of-the-art ROs, a high current is needed to achieve reasonable phase noise. In [4], the phase noise is enhanced by increasing the current drawn by the RO. Three identical ROs are connected in parallel to achieve the best phase noise. For less demanding applications, two out of the three cores could be shut down to reduce the power consumption 3× while degrading the phase noise by 5 dB. The RO-based phase-locked loop (PLL) typically needs a low drop-out (LDO) regulator to address its poor power supply rejection (PSR) of noise and ripple [9], [10]. The supply sensitivity is usually several MHz per mV [14]. However, an LDO with a high PSR over a wide bandwidth is extremely challenging in advanced CMOS due to the decreasing dynamic resistance r_{out} and increasing parasitic capacitance of (long channel) devices.

On the other hand, the major issue of LC-PLLs is a narrow tuning range (e.g. 15–30%) and large occupied area.

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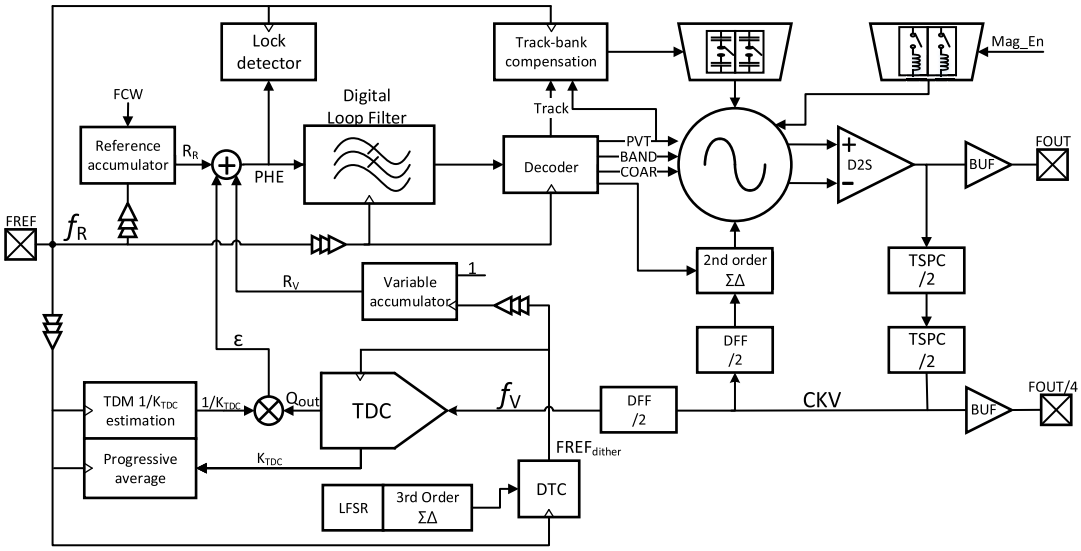


Fig. 1. Block diagram of the proposed ADPLL.

To increase the tuning range, multiple oscillator cores are usually employed [7], [11], [12]. However, the large resulting area is usually cost prohibitive.

All-digital PLLs (ADPLL) are widely used in advanced CMOS, where they exploit the naturally fine conversion resolution of time-to-digital converters (TDC) and digitally controlled oscillators (DCO), thus further reducing the area and power dissipation over analog PLLs [4]–[6], [8], [12]–[18]. FinFET technology provides an especially good solution due to its faster switching transistors with lower propagational speed and lower power consumption, all in a much smaller area than in the coplanar technology [19]. In this article, we present an ADPLL fabricated in 10-nm FinFET technology to achieve a good supply noise rejection, wide tuning range, and reasonable jitter performance within a very limited area for clock generation and wireline communications SoCs [20].

Block diagram of the proposed ADPLL is shown in Fig. 1. The key innovation is a compact transformer-based DCO described in Section III. Four further innovations are introduced: 1) an adjustable magnetic coupling technique to extend the DCO tuning range to near octave (Section III-B); 2) a compensation of tracking bank gain for the reduced quantization noise floor (Section III-D); 3) a new metastability clock scheme in the TDC (Section IV); and 4) a low complexity K_{TDC} estimator to minimize the digital area (Section V).

II. ADPLL Architecture

At the heart of this ADPLL lies the differential LC-tank DCO, as shown in Fig. 1. To save the power consumed by the clock distribution network, a D2S block transforms the differential oscillator output waveform into a single-ended clock, which goes to the main output as FOUT at $f_{\mathrm{out}} \approx 10$–$20\,\mathrm{GHz}$. FOUT is further divided by two stages of $\div 2$ dividers going to the secondary output, FOUT/4, and is also fed back to the TDC-based phase detector through another $\div 2$ divider.

In this RF synthesizer of wide tuning range, the divider selection is quite important due to its trade-off between consumed power and the capability of wide operational frequency. An injection-locked divider, which is widely adopted in mm-wave/RF wireless applications, is not in consideration here due to the narrow tuning range and large area. Most designers will use a D-flip-flop (DFF) based divider, TSPC divider, or CML divider in wireline applications for the wide tuning range operation. Current-mode logic (CML) divider could handle very high input frequency due to its fast response time. Since the static current is required, the power consumption is quite large. True single-phase clock (TSPC) divider is an alternative solution for medium frequency due to its requirement of full swing. In the first two $\div 2$ divider stages after the $\sim$10–20 GHz DCO, the operational frequency band is $>5\,\mathrm{GHz}$, so TSPC appears suitable. For the third-stage divider feeding the DCO $\Sigma\Delta$ modulator, the TSPC and static dividers could both meet the specification, so the DFF $\Sigma\Delta$ to save power.

The 2^{nd}-order $\Sigma\Delta$ modulator provides dithering to the DCO to minimize the quantization noise with a sampling rate of $f_{\mathrm{out}}/8$ frequency. A digital-to-time converter (DTC) is inserted before the TDC to dither its FREF input in order to reduce the reference spurs and improve the in-band noise [16]. To achieve a compact implementation of a short dither sequence generator, a linear feedback shift register (LFSR) is used for DTC control.

III. Design of Compact-Transformer DCO

A. Transformer-Based Oscillator

As stated above, the RO would burn excessive power just to produce a relatively mediocre level of jitter performance. Furthermore, an RO-based PLL usually requires a wide bandwidth and high PSR LDO to decrease its high sensitivity to noise and perturbations on the power supply lines coupling from the rest of the SoC, especially switching digital circuitry.

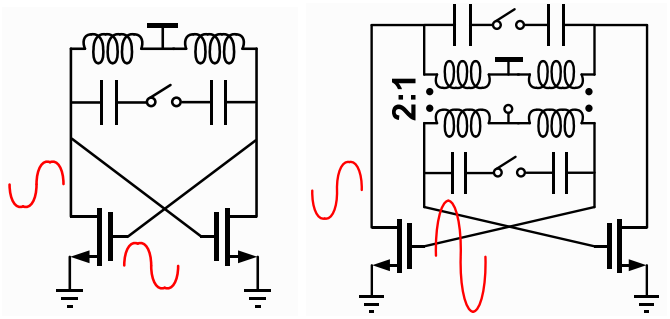


Fig. 2. (a) Conventional inductor-based oscillators. (b) Transformer-based LC-tank oscillators.

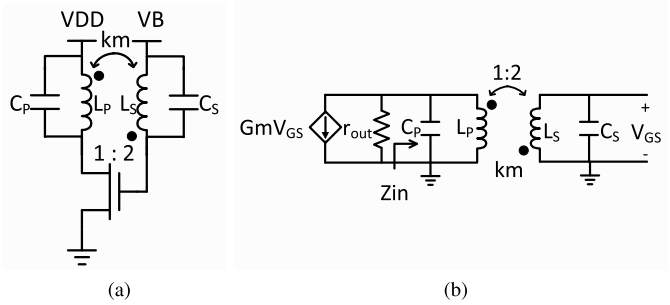


Fig. 3. (a) Transformer's half-circuit. (b) Small-signal models.

As an alternative, an LC-tank oscillator could easily improve the Q-factor 5–20×, thus resulting in a much better jitter performance. For the immunity to power supply noise, the LC tank oscillator usually features 100× better frequency pushing than the RO-based oscillator due to its resonating frequency being established by the product of the inductor (L) and capacitor (C) values only. If the single-coil inductor is replaced with a multi-coil inductor (i.e. transformer), a larger loop gain can be achieved to bring up a more reliable start-up condition at a low power consumption [21].

As mentioned in Section I, the LC-based oscillator usually occupies an excessive area due to the required high-Q of inductor which needs to be physically large. Since the inductor needs to be minimized here, its Q-factor will be inevitably degraded [8]. Hence the need for a transformer with a passive voltage gain which also helps with an oscillation start-up in low-Q conditions, as shown in Fig. 2. In Fig. 3, if we put the primary coil on the drain side and the secondary coil on the gate side, then the voltage loop gain could be enhanced by the product of the coupling coefficient k_m and turns ratio N, as in (1).

$$H(s) \simeq G_m(r_{\text{out}}||Z_{in}(s))k_m N \tag{1}$$

where G_m and r_{out} are the large-signal transconductance and output impedance of cross-coupled MOS, respectively. Z_{in} is the input impedance of the transformer seen from the primary side, as shown in (2):

$$Z_{\text{in}}(s) = \frac{s^3(L_P L_S C_S)(1-k_m^2) + sL_P}{s^4(L_P L_S C_P C_S(1-k_m^2)) + s^2(L_P C_P + L_S C_S) + 1} \tag{2}$$

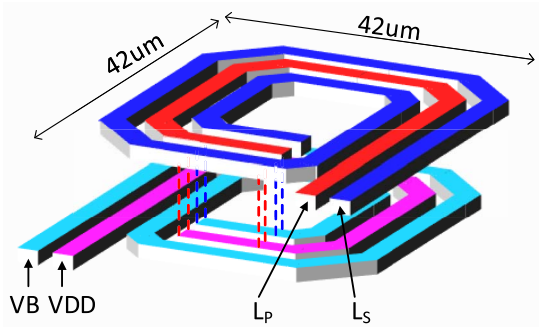


Fig. 4. 3D layout of the transformer.

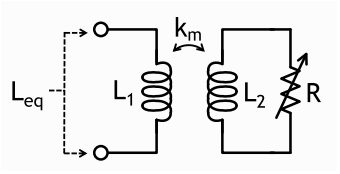


Fig. 5. Magnetic coupling technique.

Components L_P (L_S) and C_P (C_S) represent the inductor and capacitor in the primary (secondary) side. In this topology, we set k_m and N to 0.707 and 2, respectively. Consequently, the enhancing factor voltage gain is 141%. The extra 41% in the enhanced voltage gain helps the oscillation start-up in the low-Q condition.

We minimize the inductor area by using a compact multi-turn stacked transformer [8]. The 3D view layout is shown in Fig. 4. The transformer is designed as a stacked topology in two thick metal layers utilizing interconnecting vias. No ultra-thick metal is needed. Primary inductor L_p has two turns as the red winding at the top and pink at the bottom. It is connected to the drain side and the supply voltage (VDD). Secondary inductor L_s has four turns marked as the blue winding at the top and the light blue winding at the bottom. It is connected to the gate side and the bias voltage (V_B). There are floating dummy metals between the bottom winding and substrate. The spacing between the primary and secondary windings is optimized to a proper coupling coefficient k_m of 0.707 for the proper class-F operation [21]. The dotted lines represent vias to connect the upper and lower metal layers. The transformer has a turns ratio of 1:2. Its size is only $42 \times 42\,\text{um}^2$. The two metal layers shown in Fig. 4 are the uppermost thick layers. To simplify the transformer arrangement and for easy design reuse, the AP layer, which is widely used for high Q-factor inductor/transformer designs, is not adopted here. To compare with the conventional LC tank oscillator, the Q-factor is $\sim 4\times$ smaller but the area is also $\sim 4\times$ smaller because the area is roughly proportional to the Q-factor.

B. Magnetic Coupling Technique for Wide Tuning Range

Having addressed the area compactness of LC-tank, the next challenge is to extend the narrow tuning range inherent in the general LC-tank oscillators. The tuning range (f_{max}:f_{min})

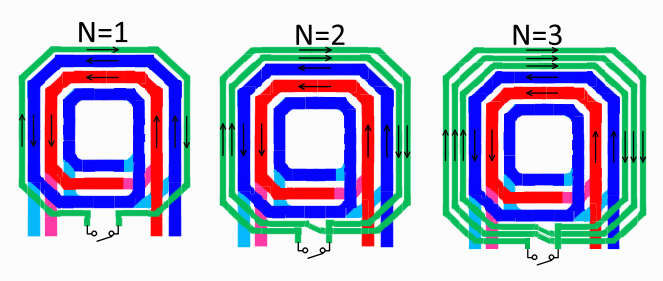


Fig. 6. Layout of the magnetic coupling technique.

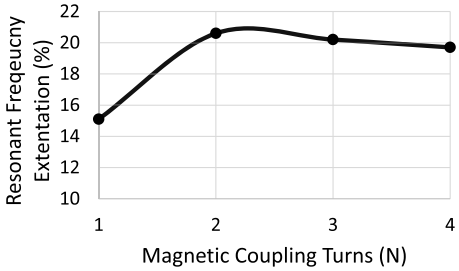


Fig. 7. Enhancement of resonant frequency by magnetic coupling of different turns.

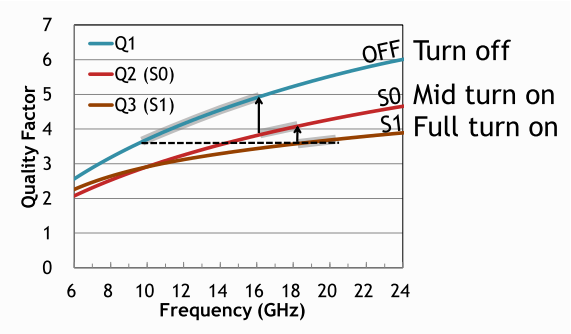


Fig. 8. Quality factor in adjustable magnetic coupling technique.

could be represented as (3):

$$\frac{f_{max}}{f_{min}} = \sqrt{\frac{C_{max}}{C_{min}}} \tag{3}$$

An octave 2:1 tuning range requires the ratio of C_{max} to C_{min} to be greater than 4 [25]. The switched capacitor (sw-cap) network is typically built with an array of metal-oxide-metal (MOM) capacitors, each connected in series with a MOS switch [17], [26]. C_{max} results when all switches are turned on. Likewise, C_{min} is reached when all switches are turned off and is established by the source/drain capacitances of the switch transistors and parasitics of interconnect wires [27]. The switch transistors must be large enough to ensure a high Q-factor of the sw-cap at low frequencies, but not too large as that would prevent C_{min} from going low enough to reach high frequencies. Hence, due to this conflicting requirement on the switch size, it is hard to enlarge the C_{max}/C_{min} ratio in the sw-cap. Practically, C_{max}/C_{min} could at best be 3 in advanced technology, which results in a tuning range of 1.7.

Consequently, we must resort to an alternative, such as magnetic tuning. Figure 5 shows the concept. The secondary coil of inductance L_2, coupled to the primary coil L_1 (here representing the transformer's equivalent winding [21]) with a coupling coefficient k_m, is loaded by a variable resistor R. The impedance seen from the primary side is:

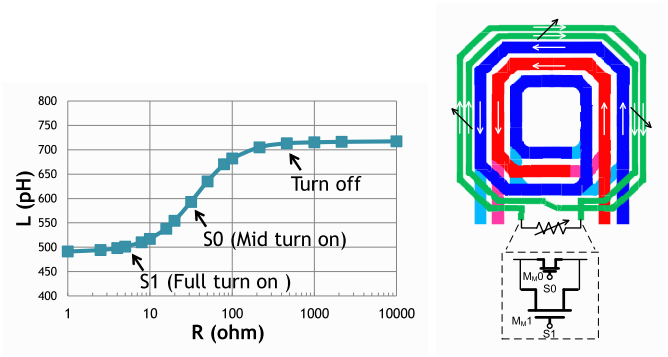
$$Z_{eq}(s) = sL_1\frac{s(1-k_m^2)L_2 + R}{sL_2 + R} \tag{4}$$

By inspection, if k_m is 0, the equivalent inductance ($L_{eq} = Z_{eq}/s$) naturally falls back to L_1. The same happens if R becomes very large. If R is close to 0, L_{eq} is equal to $L_1(1-k_m^2)$. For all other cases, the equivalent impedance will show both real (resistive) and imaginary (inductive) components. This has been studied in [31], [32] for mm-wave oscillators. Our goal is to increase k_m to minimize the equivalent inductance when $R \to 0$ such that the ratio $L_{eq}(R \to \infty)/L_{eq}(R \to 0) = 1/(1-k_m^2)$ is maximized, as demonstrated later in Fig. 9(a). This allows to further extent the maximum resonant frequency to a much higher value.

Figure 6 shows the layout of transformers employing the magnetic coupling technique. The red and blue traces represent the original 2-winding transformer, as shown earlier in the 3D view layout in Figure 4. The green trace represents the magnetic coupling coil. The switch lies on the South side of the green turn. Once the switch turns on, the opposite magnetic field will try to cancel the main one according to the Lenz's law, thus decreasing the equivalent inductance seen by the transformer and increasing its resonant frequency. In $N = 1$, the resonant frequency will be enhanced by 15%, as shown in Figure 7, but it is still not high enough. We further need an extra 20% enhancement to reach the octave tuning range. Hence, we start to increase the number of magnetic coupling turns and enhance the coupling coefficient. However, the resonant frequency enhancement becomes saturated after $N = 2$ due to the parasitic capacitance. More turns simply result in a larger parasitic capacitance. This parasitic capacitance cancels the opposite magnetic field and degrades the frequency enhancement. Hence, we have chosen $N = 2$ to obtain the largest tuning range extension of 20.6%. Although the main task of the magnetic coupling winding is to produce an opposite magnetic field for the cancellation, the resistance in this coil will be seen at the transformer's primary via magnetic coupling. The width of the magnetic coupling coil needs to be traded off between the resonant frequency boost and Q-factor degradation. In this design, the width is set to 1/2 of the original transformer winding to help with the inter-winding spacing.

The strong magnetic coupling technique will inevitably degrade the transformer's Q-factor. In (5), which assumes the series resistance losses are dominant, if the inductance L is reduced by the Lenz's law and the effective series resistance r_s is increased due to the turn-on resistance of MOS switches, the Q-factor could degrade heavily.

$$Q = \frac{\omega L}{r_s} \tag{5}$$



(a) (b)

Fig. 9. (a) Effective inductance versus the loading switch resistance R. (b) Layout of the adjustable magnetic coupling.

As shown in Figure 8, as the resonant frequency goes up, the Q-factor increases in the original turn-off state of extra magnetic coupling. Then, at the 16 GHz switch-over point, Q-factor goes down when the magnetic coupling turns on. Fully turning on the switch would induce a worse quality factor than in the case of softly turning it on. The Q-factor will drop 33% from 5.3 to 3.5 while fully turned on. It could even brake the oscillation. Hence, we need to add a softer mid turn-on state (engage M_{M0} in Fig. 9(b)) to provide a medium inductance and a lighter quality factor degradation of only 20%. The Q-factor then increases with the frequency increase from 16 to 18 GHz. This way, the quality factor will always stay above the lower bound (dotted segment) and so the oscillator start-up condition could be safe across the entire tuning range.

The relationship between R and L_{eq} is shown in Fig. 9(a). The effective inductance gets saturated at the lower bound when the resistance is smaller than 10 Ω. Thus, we could set different switch sizes for the magnetic-coupling tuning. A middle turn-on state could be set by the M_{M0} switch which has a 25× smaller W/L ratio than in M_{M1}, as shown in Fig. 9(b). Since the 10 Ω value requires a large MOS switch, the metal routing is done in such a way that it prevents from horizontal and vertical coupling of the source and drain sides of the MOS switch.

C. Oscillator Design

Figure 10 shows a complete schematic of the DCO and its buffers. The primary tank is drawn in blue color. It is connected to the coarse and fine tuning capacitors. The secondary tank is in red. The turns ratio is set to 1:2 for the class-F operation. PVT and BAND banks contain the coarse tuning capacitors and TRACK bank contains the fine tuning capacitors. The magnetic coupling is in green with two switchable MOS transistors. M1–M2 comprise the cross-coupled G_m device providing negative resistance to start up and sustain the oscillation.

M3–M6 comprise the NMOS-only buffer with dc-coupling [8], shifting the dc level from V_{DD} to half of V_{DD}. In the conventional AC-coupling technique, the dc-blocking capacitor would occupy a large area and the resistor would inject its noise back into the tank. Using a dc-coupled buffer can

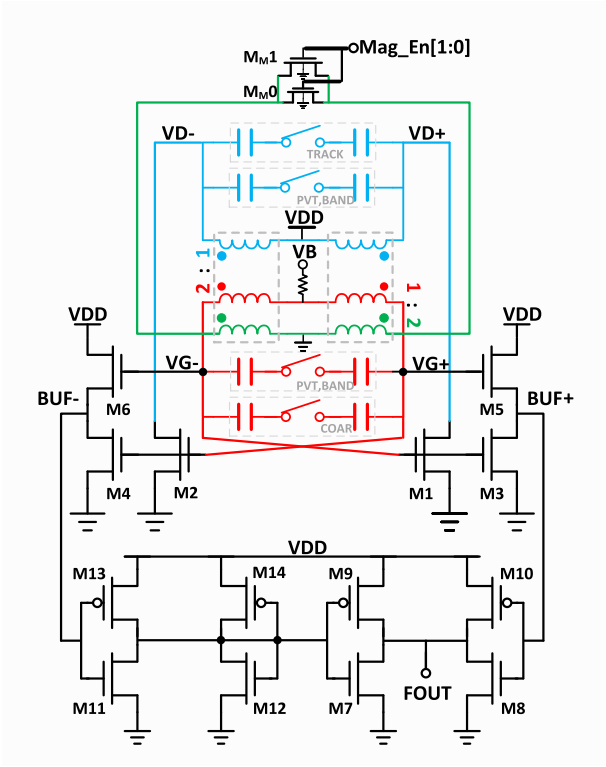


Fig. 10. Schematic of transformer-based oscillator with magnetic coupling and DC-coupled buffer with differential-to-single-ended conversion (D2S).

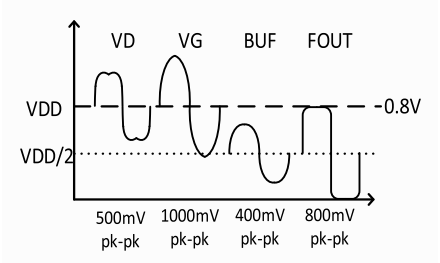


Fig. 11. Time-domain waveforms at major nodes of Fig. 10 oscillator.

prevent these issues. However, the DCO outputs at a dc level of V_B, at which it is difficult to design an effective dc buffer. Using the NMOS-only buffer could solve these problems. M5–M6 have a 4× larger W/L ratio than M3–M4 do in order to maintain the duty cycle and DC level of the output signal. M7–M14 feature the same W/L ratio for PMOS and NMOS transistors and form a high-speed differential-to-signal-ended buffer (D2S) to provide the single-ended full-swing clock to the true single-phase clock (TSPC) divider in the following stage. Using a single-ended buffer helps to reduce power consumption in the divider chain. An oscillation waveform with a dc level of V_{DD} might cause reliability issues. Since the oscillation amplitude is proportional to the quality factor, the oscillation amplitude in this low-Q design is not excessively large as in the conventional LC-tank oscillators. We only need to ensure that the peak of oscillation amplitude would not exceed V_{MAX} of the process.

Figure 11 illustrates the corresponding time-domain waveforms at each stage. V_D lies at the dc level of V_{DD} (0.8 V). V_D shape exhibits a square-like wave due to the third harmonic tone present in this class-F oscillator [21]. V_G is a 2× larger

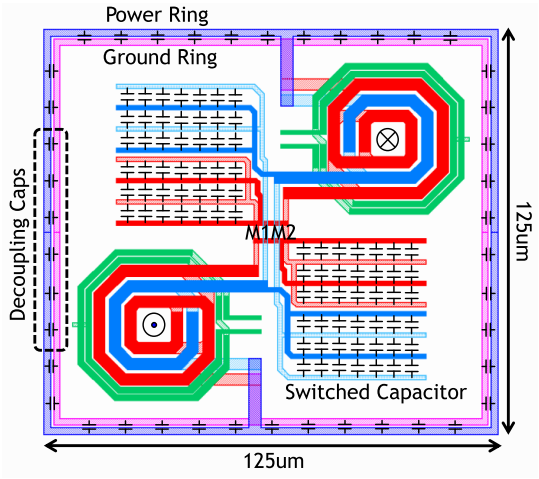


Fig. 12. Point-symmetric pseduo-differential layout of compact transformer-based oscillator.

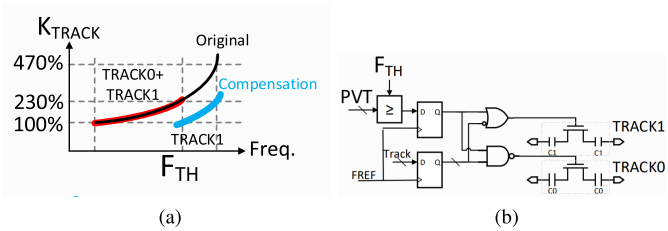


Fig. 13. Nonlinear DCO gain compensation: (a) compensation technique; (b) compensation design implementation.

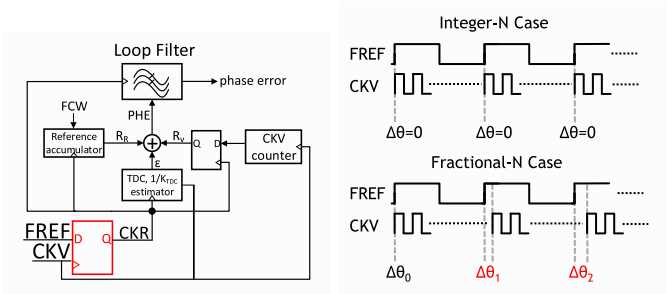


Fig. 14. Metastability issue in fractional-N phase-domain ADPLLs: (a) block diagram; (b) timing diagram.

waveform than V_D due to the transformer's 1:2 turns ratio. After the NMOS-only buffer, BUF DC level is down to half of VDD (0.4 V). Since the oscillator buffer BUF produces a differential signal which might not be rail-to-rail, D2S circuit helps to transform it to a single-ended clock with a rail-to-rail swing for the following TSPC and CMOS clock buffers.

The coarse PVT bank is a binary-weighted switched-capacitor array split into the transformer's primary and secondary to achieve the maximum Q-factor enhancement [21]. To improve the fine-tune resolution without degrading the total tank's Q-factor, TRACK bank is connected to the primary coil to benefit from the capacitance transformation of $1/N^2$. The PVT bank provides large steps of 140 MHz/LSB and dominates the DCO tuning range [29]. The COAR and TRACK banks have a resolution of 15 MHz/LSB and 1.2 MHz/LSB, respectively. The COAR bank is 4 bits in binary code and the TRACK banks is 5 bits in thermometer code. A time-averaged resolution of 37.5 kHz is achieved by 5 fractional tuning bits undergoing a 2nd-order ΣΔ dithering [29], feeding a 3-bit unit-weighted capacitor bank at the transformer's primary.

Figure 12 shows the DCO layout. There are two pseudo-differential transformers. The G_m transistors M1 and M2 lie at the center of this layout plan. The power and ground ring with the decoupling capacitors provide the AC ground for each transformer. The transformers are laid out as point-symmetric to the center. Blue and light blue lines represent the primary winding in the differential mode. Red and light red lines represent the secondary coil. They connect the gates/drains of MOS transistors and the power ring. This floorplan allows for the magnetic field cancellation. The transformer in the top right produces a magnetic field in one direction, but the opposite direction is produced by the transformer in the bottom left. Once the magnetic field is substantially canceled, the field's interference within the SoC will also be reduced. The switched-capacitor bank could occupy the remaining 50% of area without any area being further wasting. In the conventional LC tank oscillators, the differential inductors usually dominate the occupied area. The total DCO size is only $125 \times 125\,\mu\text{m}^2$ and so the core area is only $0.016\,\text{mm}^2$.

D. Nonlinearity of DCO Gain

Having achieved the small area and wide tuning range, we still see yet another drawback naturally existing in wide tuning-range LC DCOs—the step size non-linearity. In (6), the gain K_{track} variation due to a fixed capacitive step ΔC is a cubic rule of resonant frequency ($f = \frac{1}{2\pi\sqrt{LC}}$) [28].

$$K_{\text{track}} = 2\pi^2 (L\Delta C) f^3 \tag{6}$$

In this design, if the frequency tuning ratio is 2×, the gain variation will be 8×. Because the quantization noise is proportional to the fine-tuning DCO gain, K_{track}, we need to compensate the tracking steps at high frequencies to prevent the ADPLL phase degradation there.

As a solution, we use two MOM tracking capacitors stacked together and selected for different bands. In the lower band, track0 and track1 are both used. The capacitance of track0 and track1 is roughly the same. Thus, K_{track} can select between two non-zero values of 4.1 MHz and 8.2 MHz with 2× ratio. With the original K_{track} shown in red in Fig. 13(a), there might be 470% variation of the DCO gain from f_{min} to f_{max} [28]. To minimize the gain variation, we set a threshold frequency to f_{th} for the compensation to be triggered. Since the oscillation frequency is highly related to the coarse tuning bank (PVT) [29], the PVT control code is fixed after locking. We set a PVT code as a threshold to judge whether the oscillation frequency is higher or lower than f_{th}. The circuit implementation is shown in Fig. 13(b). The comparator is triggered at every frequency reference cycle and lets the tracking bank to use either track1 only or both track0 and track1. Once the PLL is locked, the PVT code should be fixed and the tracking bank compensation completed. With this technique, the variation of K_{track} will reduce from 470% to 230%.

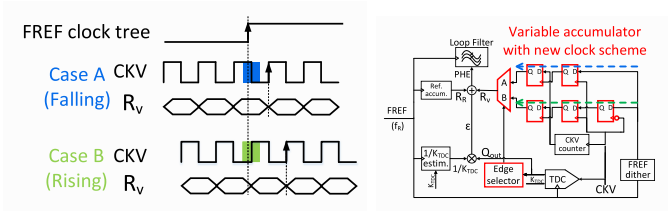


Fig. 15. Solution of metastability issue in fractional-N phase-domain ADPLL: (a) timing diagram, (b) block diagram.

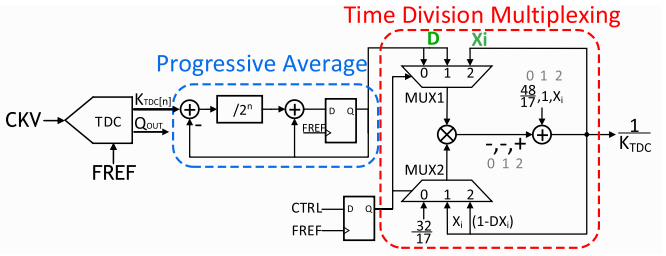


Fig. 16. Proposed method for $1/K_{\mathrm{TDC}}$ estimation with progressive averaging and time-division multiplexing.

IV. Metastability in Fractional PLLs

Having solved the key issues of the wide-tuning-range DCO, the next two techniques are related to the system level. Figure 14(a) shows a block diagram of the conventional ADPLL [13], [15]. It has two independent clock domains, namely FREF and CKV, thus it could experience metastability, for example, in the resampling FF for the CKV counter. This is prevented by employing the red-colored D flip-flop (DFF) which aligns the clock edges of FREF to CKV, and the resulting retimed clock (CKR) is adopted by all the lower-speed digital blocks. The ADPLL works now correctly in the integer-N case since the phase error is usually a small constant after locking,[1] as shown at the top of Figure 14(b). In a fractional-N ADPLL, there might be a metastability issue in the red DFF itself, as shown in 14(b). The DCO phase (i.e. edge positions) versus FREF will vary in accordance with FCW and so $\Delta\theta_n$ constantly changes. In the fractional-N mode, the red DFF could likely encounter the metastable timing alignment between CKV and FREF. The metastability issue can have a detrimental effect in increasing the fractional spurs.

Figure 15 shows a new metastability resolution scheme. The main idea is using the edge selector from the TDC to select the safe edge of CKV (rising or falling) for the FREF sampling and thus to prevent the metastability risk. In "case A" of Figure 15(a), if the FREF rising edge is close to the CKV falling edge, we use the rising edge of CKV for reclocking. R_V will be selected as path A (blue dotted line) in Figure 15(b). In "case B" of Figure 15(a), the CKV falling edge is chosen for the reclocking. The edge selector will set R_V to select path B in the MUX where CKV will use an extra DFF with the inverted CKV clock. The edge selector judges the phase relationship by the TDC data output bit Qout. We monitor the first transition of $0 \rightarrow 1$ or $1 \rightarrow 0$ to judge the CKV–FREF relationship. For example, if the first transition is $0 \rightarrow 1$, i.e. the region within the 1/4-th of CKV cycle, the edge selector will determine it is too close to the CKV's rising edge and use case B to get the correct result.

V. TDC Gain Normalization Method

To have a compact ADPLL, a simplified digital design is also important. In this section, we try to minimize the digital core area of a circuit that is potentially of high complexity if not properly optimized. The TDC output with a gain ($K_{\mathrm{TDC}} = T_V / t_{\mathrm{inv}}$) needs to be normalized by its inverse, $1/K_{\mathrm{TDC}}$, where T_V and t_{inv} are the DCO clock period and inverter delay (TDC resolution), respectively [13]. We present a low-complexity adaptive estimator of $1/K_{\mathrm{TDC}}$ with progressive averaging and time-division multiplexing, as shown in Fig. 16.

A progressive-average (PA) calculator smoothens the TDC output roughness due to the quantization noise and is preferred over the straightforward moving-average implementation for cost reasons. It could be represented as:

$$K_{\mathrm{TDC,PA}} = \frac{\Sigma_{i=0}^{n-1} K_{\mathrm{TDC},i}}{n} \tag{7}$$

where, $K_{\mathrm{TDC},i}$ represents the ith sampled data that is accumulated over n samples. The sampling clock is FREF. As shown in Fig. 16, the circuit implementation of progressive averaging is quite simple. It only requires two adders and one shift register. For an alternative moving average method, the system would need to save n data values within a certain period, which costs significant hardware to implement. The progressive-average method only saves one data value each cycle. The area cost benefits are $n-1$ times better. Generally speaking, the number of n would usually be larger than 10.

In [22], a least-mean-squared (LMS) calibration based on phase error is applied to estimate the reciprocal of K_{TDC}, but that might suffer from a non-convergence problem in the fractional-N mode, especially when it is close to integer-N [17]. A Newton-Raphson method is proposed here to provide a reciprocal of K_{TDC} with a recursive equation and guarantee absolute convergence taking max 3–4 iterations even in face of a large step input. The Newton-Raphson equation for the reciprocal [30] is represented in (8), which recursively calculates the inverse of $D = K_{\mathrm{TDC}}$ over internal steps of i.

$$X_{i+1} = X_i + X_i \cdot (1 - D \cdot X_i) \tag{8}$$

After 3–4 iterations, X_{i+1} will approach $1/D$, where $0.5 \leq D \leq 1$. The initial value of X_i is represented as $X_{i=0}$. To minimize the peak of the approximation error, $X_{i=0}$ is represented as [30]:

$$X_{i=0} = \frac{48}{17} - \frac{32}{17} \cdot D \tag{9}$$

The above coefficients of the linear approximation are determined by Chebyshev equioscillation theorem. Using this approximation, the absolute error of the initial value is less than 1/17. Thus, three multipliers are required to get the reciprocal of $1/K_{\mathrm{TDC}}$ by employing (8) and (9). Multipliers cost a huge area and power penalty due to the digital complexity.

[1] In a type-II PLL, CKV will be substantially aligned with FREF but one can add a small offset to avoid the metastability in the red DFF itself.

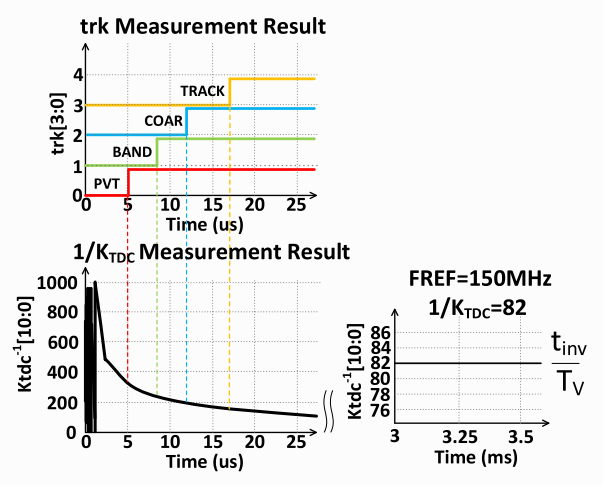


Fig. 17. Measurements of K_{TDC} estimator.

In this design, one multiplier needs a 19-bit output (6b + 13b). The high input word-length further makes it area/power expensive. A time-division multiplexing technique is proposed here to reduce the number of multipliers from 3 to 1 while getting the same result. In MUX1 and MUX2, they execute the 0, 1 and 2 MUX input paths serially with each FREF cycle. Consequently, the digital core size is substantially minimized.

Fig. 17 shows the measurement results of the new estimator. The calculation starts as early as the PVT acquisition. The trk[3:0] bus signal controls the acquisition kick-off time in each bank. For example, the PVT bank starts the acquisition at 5 μs, as shown by the rising edge of the red line. The vertical red dotted line indicates some early settling of the $1/K_{\mathrm{TDC}}$ signal starting to reveal the progressive average behavior. After 3 ms, $1/K_{\mathrm{TDC}}$ is well settled and its curve is flat without any further changes. The value of $1/K_{\mathrm{TDC}}$ is 82 in this case under $f_R = 150$ MHz and $f_V = 1.5$ GHz, where f_R and f_V are the reference and variable frequencies seen by the TDC. From this, the inverter delay can be calculated as $t_{\mathrm{inv}} = T_V/K_{TDC} = 8.2$ ps, in which $T_V = 1/f_V$. There are different digitally controlled settings for fast/slow settling modes of $1/K_{\mathrm{TDC}}$ estimation. In Fig. 17, the slow settling mode with accurate adaptation results is demonstrated. For the fast settling mode, the settling time could be less than 6.4 μs with $\leq 1.1\%$ error. In practice, the trade-off between the accuracy and speed of the adaptation loop is addressed by a dynamic switch-over of its loop bandwidth from wide to narrow, as typically done in ADPLLs [15].

VI. Measurements

Figure 18 shows the chip micrograph of the ADPLL. It is fabricated in TSMC 10-nm FinFET CMOS. The DCO core occupies merely 0.016 mm^2. The clock output is on the North side of the DCO core, so the divider chain lies nearby. The buffer line on the West side passes the divided output clock to the TDC at the South-West. The TDC with a 128-stage delay line and its metal routing output bus occupies 0.004 mm^2. The digital core occupies 0.01 mm^2 at the South-East side. The active ADPLL region is only 0.034 mm^2. The total area is smaller than the published RO-based frequency synthesizers

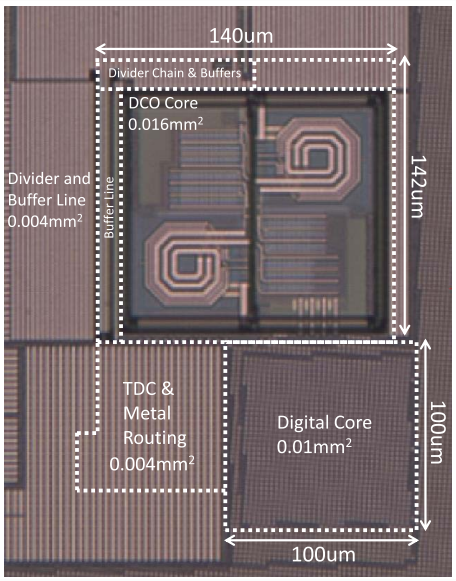


Fig. 18. Chip micrograph of the ADPLL.

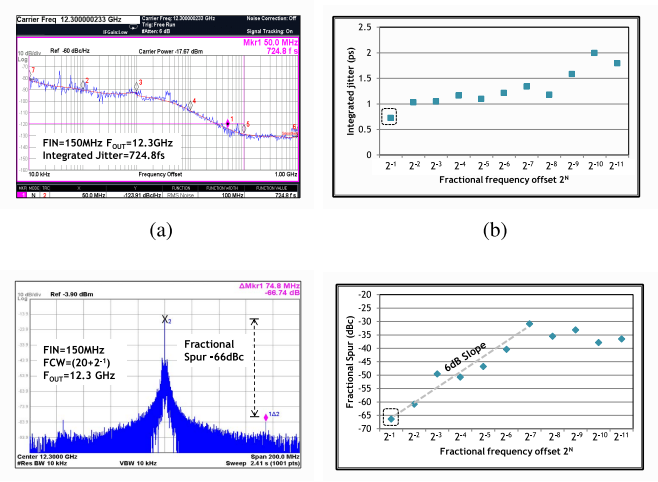
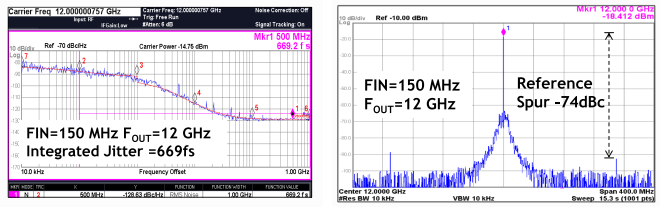


Fig. 19. Measured fractional-N mode: (a) phase noise profile; (b) phase jitter at different fractional frequency offsets; (c) wide spectrum plot; (d) fractional spurs at different fractional frequency offsets at 12.3 GHz.

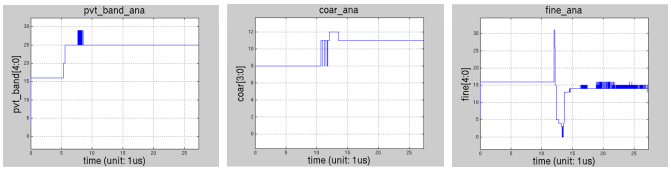
that include the necessary LDOs. The DCO, divider and buffers consume 9 mW. The TDC, $\Sigma\Delta$ modulator and variable accumulator consume 1.6 mW. The digital core consumes 1.3 mW. The total power consumption P_{DC} is 11.9 mW and the frequency range is from 10.8 GHz to 19.3 GHz, which is almost an octave.

Fig. 19 shows the measurements of integrated jitter and spurious tones in an internal fractional-N mode of ADPLL's phase detector (i.e. f_V/f_R in Fig. 1). In Fig. 19(a), the sub-ps phase jitter of 725 fs is achieved while f_R is 150 MHz and f_{out} is 12.3 GHz. The overall fractional division ratio in this case is $20.5 \times 4 = 82$, but because of the DCO's $\div 8$ divider, the TDC sees FCW = 20.5. The fractional part is 2^{-1} in this case, which shows the lowest phase jitter among all the fractional frequency offsets in Fig. 19(b). In Fig. 19(c), the fractional-N spurs are -66 dBc outside of the loop bandwidth and they increase going into the inband with a 6 dB slope, as shown in Fig. 19(d). As the fractional-N spurs go inside the loop



(a) (b)

Fig. 20. Measured integer-N operation plots: (a) phase noise; (b) wide spectrum.



(a) (b) (c)

Fig. 21. Measured acquisition behavior of (a) PVT_BAND, (b) COAR and (c) TRACK (fine) banks.

band, the integrated jitter is consequently increased to $\sim$1 ps, except for the very small fractional FCW of $\leq 2^{-9}$, where it reaches 1.5–2 ps. Techniques to reduce such fractional spurs were presented, among others, in [16], [17].

Figure 20(a) shows the phase jitter in integer-N mode at 12 GHz output with the 150 MHz reference. This mode could reach smaller integrated jitter 669 fs without the fractional spurs. Figure 20(b) shows the spectrum plot. The reference spurs can reach -74 dBc at 12.15 GHz (150 MHz $\times$ 81), which is a fairly low level.

Figure 21 shows the measured ADPLL loop settling behavior of the the three DCO tuning banks by means of *capturing* the DCO tuning input signals into the SRAM memory during the actual operation. This case corresponds to the locking frequency of 14.4 GHz with 150 MHz FREF. The default PVT code is close to the target frequency and no acquisition is required. The start-up time is within 5 μs and the lock time is 22 μs.

Table II shows the performance summary and comparison with state-of-the-art in PLLs featuring a small area in advanced technology. Our operational frequency is the highest among all LC tank oscillators. The core area is compatible with the RO ADPLL and as little as half of the analog LC PLL [7]. The phase jitter could achieve sub-ps due to the transformer-based DCO. The frequency pushing of 1.8%/V is hundreds of times smaller than in the RO-based frequency synthesizers (without any LDO) [4].

For an overall performance assessment of a PLL, the jitter (σ_t) figure-of-merit (FoM) was defined in [23] as:

$$\mathrm{FoM} = 20\log_{10}\left(\frac{\sigma_t}{1s}\right) + 10\log_{10}\left(\frac{P_{\mathrm{dc}}}{1\mathrm{mW}}\right) \quad (10)$$

An extension, $\mathrm{FoM_T}$, normalizes it to the tuning range, TR:

$$\mathrm{FoM_T} = \mathrm{FoM} - 20\log_{10}\left(\frac{\mathrm{TR}[\%]}{10}\right) \quad (11)$$

The area cost is essential in advanced technology and the LC tank oscillators usually require huge area due to the inductor. Consequently, $\mathrm{FoM_{TA}}$ is defined to further normalize it to the occupied silicon area:

$$\mathrm{FoM_{TA}} = \mathrm{FoM} - 20\log_{10}\left(\frac{\mathrm{TR}[\%]}{10}\right) + \log_{10}\left(\frac{\mathrm{Area}}{1\mathrm{mm}^2}\right) \quad (12)$$

FoM, FoM_T and $\mathrm{FoM_{TA}}$ of the proposed ADPLL are -232, -247, and -262 dB, respectively. Our best reported $\mathrm{FOM_{TA}}$ signifies achieving the adequate state-of-the-art performance for the intended application but at the near-octave tuning range and the lowest possible occupied area.

TABLE II
PERFORMANCE SUMMARY OF FRACTIONAL-N PLLS

	This work	Ximenes[8] MTT'17	Wu[12] JSSC'17	Raczkowski[24] JSSC'15	Lee[7] JSSC'15
Process	10nm	40nm	28nm	28nm	28nm
PLL Type	ADPLL TDC-based	ADPLL TDC-based	ADPLL TDC-based	PLL Sub-sampling	PLL Charge-pump
Osc. Type	LC DCO	LC DCO	LC DCO	LC VCO	LC VCO (Dual Core)
Frequency (GHz)	10.8-19.3	9.4-14.8	3.5-6.8	9.2-12.7	2.7-4.5 4.0-7.0
Power (mW)	11.9	12-20	10.7	13	14
Supply (V)	0.8	1.0 – 1.1	1.1	1.8	1.8
Core Size (mm^2)	0.034	0.063	0.5	0.59	0.07
Phase Jitter(ps)	0.725	0.74	0.42	0.28	1.1
Frequency Pushing (%/V)	1.8	0.8	--	1.8	--
FOM(dB)	-232	-230	-237	-240	-229
$\mathrm{FOM_T}$ (dB)	-247	-243	-253	-250	-247*
$\mathrm{FOM_{TA}}$(dB)	-262	-255	-256	-252	-259*

*TR is capped at octal due to dual core

VII. CONCLUSION

In this article, we have proposed a new fractional-N ADPLL architecture with the following features: Nearly one octave tuning range with a single LC tank oscillator, which does not require ultra-thick metal layers, thus could be universally used in all CMOS flavors. The DCO is assisted by an adjustable magnetic coupling technique that increases the tuning range by 17.2%. The compensation of tracking bank resolution can keep the DCO gain K_{track} roughly constant over this wide tuning range, thus maintaining the quantization level. A new metastability resolution scheme is adopted to overcome the fractional-N problem. The low complexity TDC gain estimator, $1/K_{\mathrm{TDC}}$, reduces the digital core area by the progressive average and time division multiplexing. Among all the fractional-N PLLs with an area smaller than 0.1mm^2, this work achieves a rms jitter of 725 fs in an internal fractional-N mode of ADPLL's phase detector (i.e. f_V/f_R). This topology featuring small area, wide tuning range, and good supply noise rejection shows the potential to replace ROs which necessarily require wide bandwidth LDOs, which is currently the most common solution for wireline communications.

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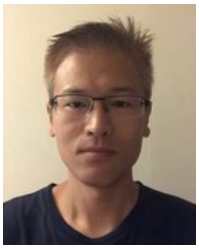

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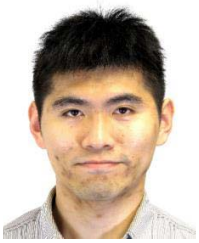

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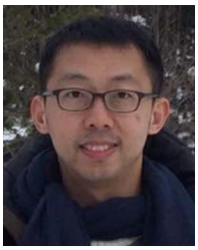

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